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AS PER : R18 B.TECH. ECE SYLLABUS
EC 404 PC : LINEAR IC APPLICATIONS B.Tech. II YEAR II SEM
ANSWERS TO QUESTIONS APPEARED IN PREVIOUS JNTUH EXAMINATIONS

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LINEAR INTEGRATED CIRCUIT APPLICATIONS
(ECE 404 PC)
UNIT – 1

INTEGRATED CIRCUITS: Classification, chip size and circuit complexity, basic information of operational amplifiers, ideal and practical op-amps, internal circuitry, op-amp characteristics, DC and AC characteristics, 741 op-amp and its features, modes of operation, inverting, non inverting, differential

Text books :

1. Linear integrated circuit by D.Roy chowdhary New Age International(P) Ltd
2. Op=Amps & linear ICs Ramakanth, A,Gayakwad , PHI

Q 1A . State the characteristics of an ideal Op-Amp

- **1. Open loop voltage gain :** infinite ($G \rightarrow \infty$)
- **2. Input impedance** : The equivalent resistance measured at either of the two input terminals by grounding the other terminal is called input impedance. It is **infinite** for an ideal Op-Amp. **($R_{in} \rightarrow \infty$)** Because of this the two input terminals does not draw any current

  3. Output impedance : The equivalent impedance measured between the output terminal and ground is **zero. ($R_0 \rightarrow 0$)** .Because of this, the output voltage is independent of the current drawn from the output.
- **4. Input Offset voltage** : When both the input terminals are connected to ground the output voltage must be zero. To make the output voltage zero a small voltage is applied to one of the terminals, the other being grounded. This small voltage is called the Input Offset voltage. (V_{ios}) . For an ideal Op-Amp V_{ios} is **zero**

Q 1B . Discuss the characteristics of a practical Op-Amp

- **1. Open loop gain** : This also called large signal voltage gain

  $A_{OL} = \frac{V_0}{V_d}$ where A_{OL} is open loop gain, V_0 is output voltage and V_d is voltage difference between input terminals

  For IC 741 A_{OL} = 200,000
- **2. Input Offset voltage** : When both the input terminals are connected to ground the output voltage must be zero. To make the output voltage zero a small voltage is applied to one of the terminals, the other being grounded. This small voltage is called the Input Offset voltage. (V_{ios})

  For IC 741 V_{ios} = 2 mV
- **3. Input Bias Current :** The small current that flows into each of the input terminals to bias the first differential pair of transistors is called bias current.

  The average input bias current $I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$

  For IC 741 I_b =80 nA

- **4. Input Offset current :** The magnitude difference between I_{b1} and I_{b2} is called the Input offset current $I_{IOS} = |I_{b1} - I_{b2}|$

  For IC 741 = I_{IOS} = 20 to 60 nA
- **5. Input impedance** : This is also called differential input resistance. It is the equivalent resistance measured at either of the two input terminals by grounding the other terminal (R_i)

  For IC 741 R_i = 2 MΩ
- **6. Common Mode Rejection Ratio :** It is normally expressed in dB. It is the ratio of Differential voltage gain A_d to the common mode gain A_c

  CMRR = $\frac{A_d}{A_c}$

  For IC 741 CMRR = 90 dB
- **7. Slew Rate** : It is the maximum rate of change of output voltage with time (V/μs)

  $S = \left|\frac{d V_0}{dt}\right|_{max}$

  For IC 741 S= 0.5 V/ μs
- **8. Gain Band width product** : It is the band width when the voltage gain is unity

  For IC 741 it is 1 MHz

Q 1B What is an ideal op-amp ? Define differential gain, common mode gain and CMRR

- An "Operational amplifier" is a direct coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and output stage.
- An ideal operational amplifier amplifies the difference between its two input terminals. The difference between the two input terminals is called differential voltage $V_d = V_1 - V_2$
- **COMMON MODE VOLTAGE:** The average level of V_1 and V_2 is called the common mode voltage

$$V_c = \frac{V_1 + V_2}{2}$$

- **DIFFERENTIAL GAIN:** The amplification gain of differential voltage V_d is called the differential gain and is denoted by A_d

$$A_d = \frac{V_0}{V_d}$$

- **COMMON MODE VOLTAGE GAIN**: The gain with which the differential amplifier amplifies the common mode signal is called Common mode gain and is denoted as A_C

$$A_C = \frac{V_0}{V_C}$$

- **COMMON MODE REJECTION RATIO**: It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C

  CMRR= $\left|\frac{A_d}{A_C}\right|$

  CMRR in dB = 20 log $\left|\frac{A_d}{A_C}\right|$
- For an ideal Op-Amp A_C should be zero. So CMRR → ∞
- Higher the value of CMRR , better will be the Op-Amp performance and it approaches ideal Op-Amp characteristics.

PROBLEM 1. : Determine the output voltage of the differential amplifier having input voltages V1 = 1 mV and V2 = 2 mv. The amplifier has a differential gain of 5000 and CMRR 1000

- V1 =1 X 10^{-3} V and V2 =2 X 10^{-3} V
- CMRR = $\frac{A_d}{A_C}$ ∴ 1000 = $\frac{5000}{A_C}$; So $A_C = \frac{5000}{1000} = 5$

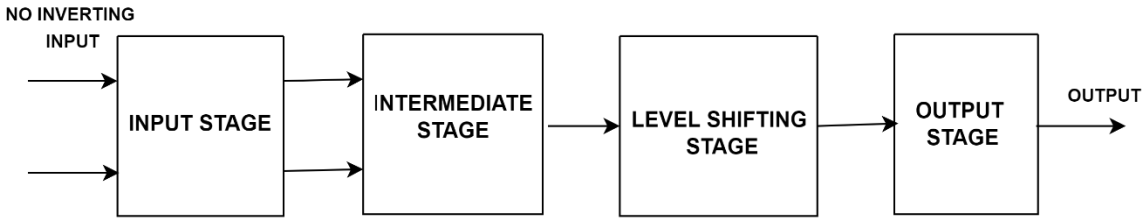
  $V_d = V_1 - V_2 = (1-2) \times 10^{-3} = -1$ mV

  $V_C = \frac{V_1 + V_2}{2} = \frac{1+2}{2} = 1.5\ mV$

  $V_0 = A_d V_d + A_C V_C = 5000\ (-1)(10^{-3}) + 5\ (1.5)(\ 10^{-3})$

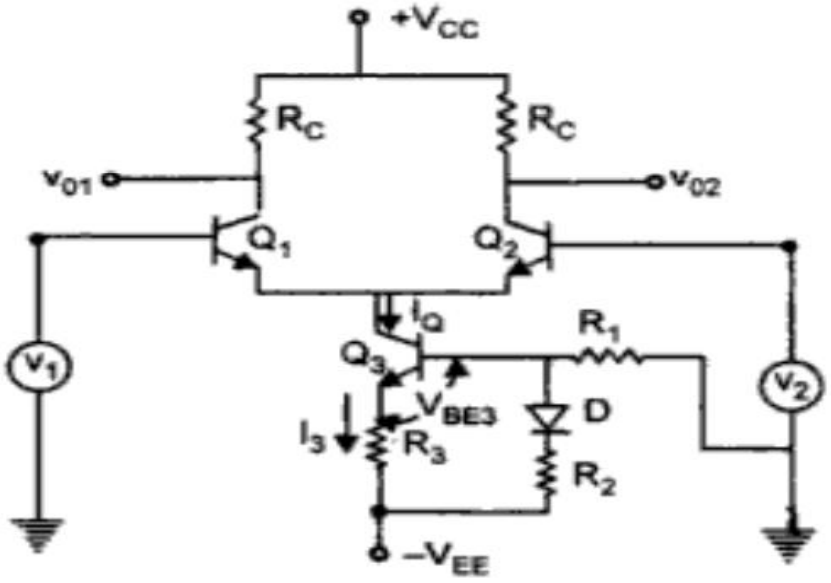
  $= -4.9925$ V

Q 2. Draw the internal block schematic of Op-Amp and mention the role of each stage



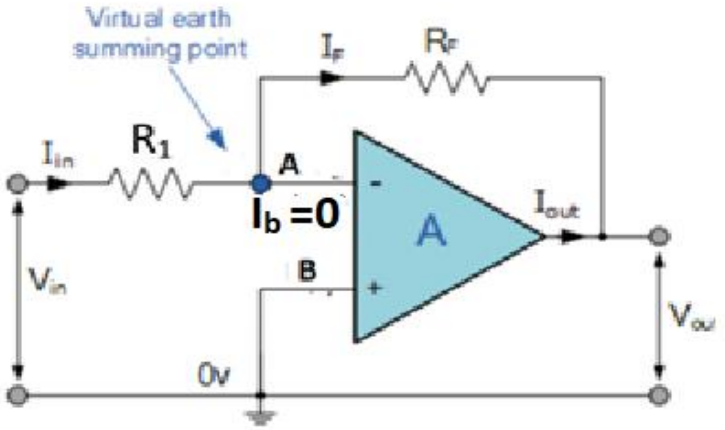
- **1. INPUT STAGE :**
- The input stage is a dual-input, balanced output differential amplifier. The two inputs are inverting and non-inverting input terminals. This stage provides most of the voltage gain of the OP-AMP and decides the input resistance value Ri.
- **2. INTERMEDIATE STAGE :**
- This is usually another differential amplifier. It is driven by the output of the input stage. This stage is a dual-input unbalanced output (single ended output) differential amplifier.
- **3. LEVEL SHIFTING STAGE :**

- Due to the direct coupling between the first two stages, the input of level of shifting stage is an amplified signal with some non-zero dc level. Level shifting stage is used to bring this dc level to zero volts with respect to ground.
- **4. OUTPUT STAGE :**
- This stage is normally a complementary output stage. It increases the magnitude of the voltage and raises the current supplying capability of OP-AMP.it also provides a low output resistance.



Q 3. Derive the expression for the output voltage of an ideal inverting amplifier

Node A is at virtual (ground) zero volts since Node B is at ground



$I_{in} = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1}$ (since V_A =0)

The Op-Amp does not draw any current ie I_b = 0

So all current I_{in} flows through the feedback resistance

$\therefore I_{in} = I_f$ So $I_{in} = -I_f$

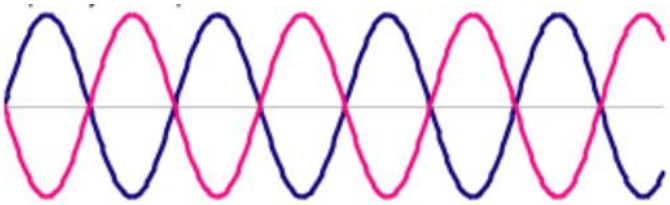
But $I_f = \frac{V_A - V_0}{R_f} = -\frac{V_0}{R_f}$

$I_{in} = I_f$

$\frac{V_{in}}{R_1} = -\frac{V_0}{R_f}$

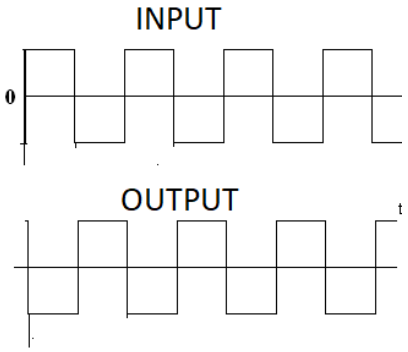
$$V_0 = -\frac{R_f}{R_1} V_{in}$$

$\frac{R_f}{R_1}$ is the gain of Inverting Amplifier and –ve indicates that the output has opposite polarity of input signal

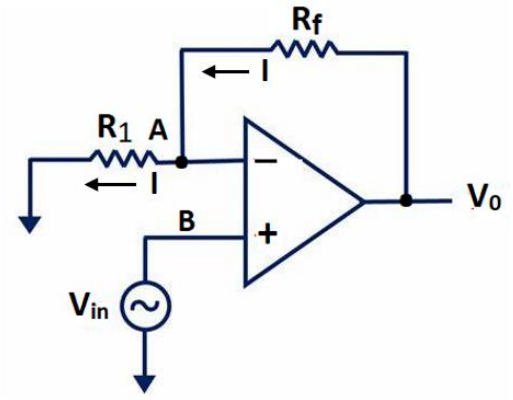


Q 4. Draw and explain the output waveform of ideal inverter circuit when the input is a square wave

- Ideal inverter has a gain depending on Rf (feedback resistor and Rin input resistor) The gain is given by the equation $-\frac{R_f}{R_1}$. The output will be 180^0 out of phase of input signal. If $R_f = R_1$, Gain = —1



Q 5. Derive the expression for the output voltage of an ideal Non- Inverting amplifier



The input is applied to the Noninverting input terminal of the Op-Amp

At node B voltage = V_{in} But $V_A = V_B = V_{in}$. This because of virtual ground concept

$$I = \frac{V_0 - V_A}{R_f} = \frac{V_0 - V_{in}}{R_f}$$

At node A $I = \frac{V_A - 0}{R_1} = \frac{V_{in}}{R_1}$ (since $V_A = V_{in}$)

Equating above two equations

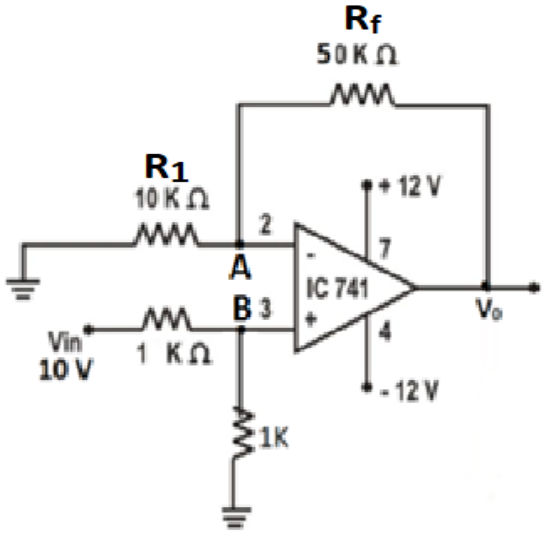
$$\frac{V_0 - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_0}{R_f} = V_{in}\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = V_{in}\left[\frac{R_f + R_1}{R_f\, R_1}\right]$$

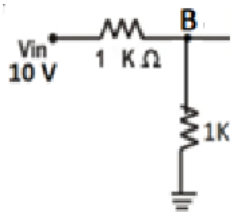
$$A_v = \frac{V_0}{V_i} = R_f\left[\frac{R_f + R_1}{R_f\, R_1}\right] = \left[\frac{R_f + R_1}{R_f\, R_1}\right] = 1 + \frac{R_f}{R_1}$$

So the gain is given by $\left[1 + \frac{R_f}{R_1}\right]$ and there is no change in polarity

PROBLEM 2: Find V_O for the circuit shown in the figure



This is the Noninverting amplifier. As such the gain $= 1+\frac{R_f}{R_i}$

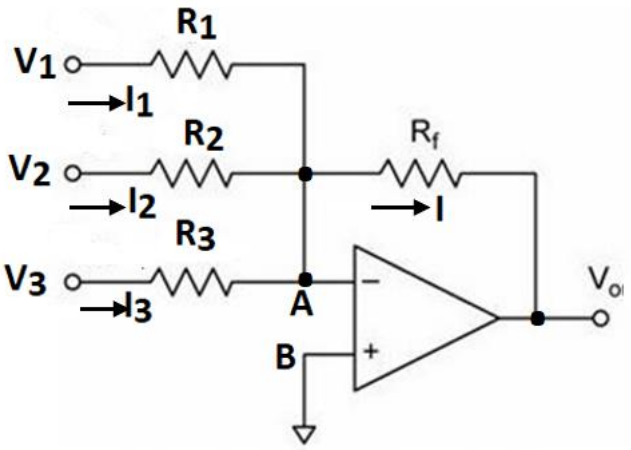


$$V_B = \frac{V_{in}}{1K + 1K} \times 1K = \frac{10}{(2)(10^3)} \times (1)(10^3) = 5\ V$$

$$V_0 = \left[1 + \frac{R_f}{R_1}\right] V_B = \left[1 + \frac{(50)(10^3)}{(10)(10^3)}\right] 5 = 30\ V$$

SUMMING AMPLIFIER INVERTING

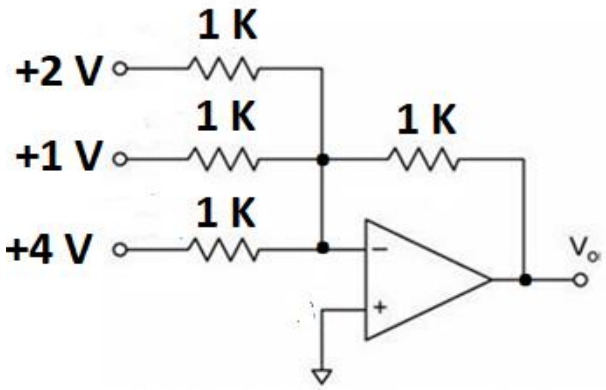
Q 6. Draw an Inverting summing amplifier with three inputs. Derive an expression for its output voltage



The Summing Amplifier Circuit Diagram

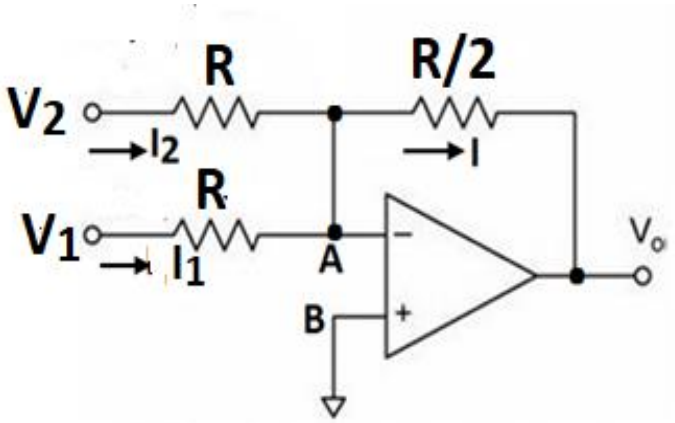
- Point B and point A are at the same potential (because of virtual short between A and B)
- But $V_B = 0$
- $\therefore V_B = V_A = 0$
- $I_1 = \frac{V_a}{R_1}$
- $I_2 = \frac{V_b}{R_2}$
- $I_3 = \frac{V_c}{R_3}$
- Using KCL at node A ,
- $I = I_1 + I_2 + I_3$
- I passes through R_f (since Op- Amp does not draw any current from node A)
- But $I = \frac{V_A - V_0}{R_f} = -\frac{V_0}{R_f}$
- $I = I_1 + I_2 + I_3$
- $-\frac{V_0}{R_f} = \frac{V_a}{R_1} + \frac{V_b}{R_2} + \frac{V_c}{R_3}$
- $V_0 = -[R_f \frac{V_a}{R_1} + R_f \frac{V_b}{R_2} + R_f \frac{V_c}{R_3}]$
- Make $R_1 = R_2 = R_3 = R$
- $V_0 = -\frac{R_f}{R} [V_a + V_b + V_c]$
- If $R_f = R$
- $V_0 = -[V_a + V_b + V_c]$
- Thus the output voltage is the sum of input voltages with polarity change

PROBLEM 3. Determine the output voltage for the configuration shown



- The circuit is inverting adder circuit
- $R_1 = R_2 = R_3 = 1\ K\Omega$
- $Rf = 1\ K\Omega$
- $V_0 = -\frac{R_f}{R}\ [V_a + V_b + V_c]$
- $V_0 = -\frac{1 \times 10^3}{1 \times 10^3}\ [2 + 1 + 4] = -7\ V$

PROBLEM 4. How summing amplifier can be used as an average. Describe

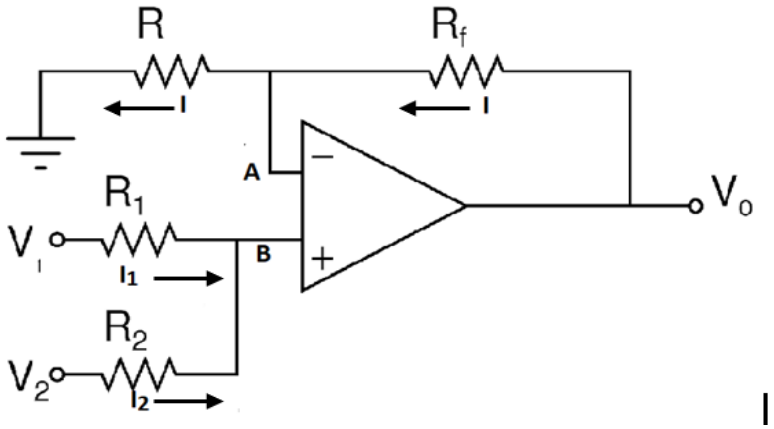


- VB =0 but VA = VB = 0 (because of Virtual ground concept)
- $I_1 = \frac{V_1}{R}$
- $I_2 = \frac{V_2}{R}$
- $I = -\frac{V_0}{R/2} = \frac{2\,V_0}{R}$

- $I = I_1 + I_2$
- $-\frac{2V_0}{R} = \frac{V_1}{R} + \frac{V_2}{R}$
- $-2V_0 = V_1 + V_2$
- $V_0 = -\frac{V_1+V_2}{2}$
- ∴ output voltage is average of two voltages with a 180^0 phase shift

SUMMING AMPLIFIER NON-INVERTING

Q 7. Draw a neat diagram of two input Non-inverting summing amplifier using Op-Amp and obtain the expression for its output voltage



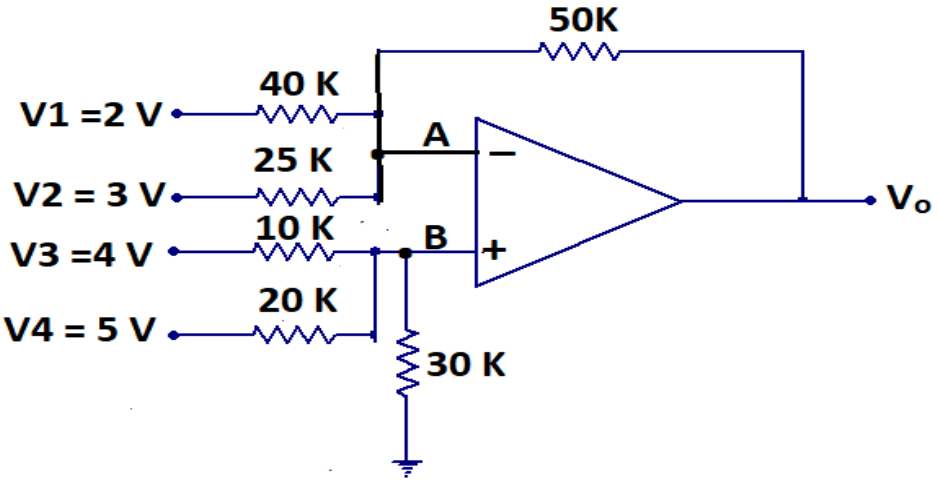
I

- $V_A = V_B$ (since node A and B are at same potential ie virtual ground)
- $I_1 = \frac{V_1 - V_B}{R_1}$
- $I_2 = \frac{V_2 - V_B}{R_2}$
- $I_1 + I_2 = 0$ (since the Op-Amp does not draw any current)
- $\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0$
- $\frac{V_1}{R_1} + \frac{V_2}{R_2} = V_B\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$
- $\frac{V_1 R_2 + V_2 R_1}{\cancel{R_1 R_2}} = V_B\left(\frac{R_2 + R_1}{\cancel{R_1 R_2}}\right)$
- $V_B = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}$

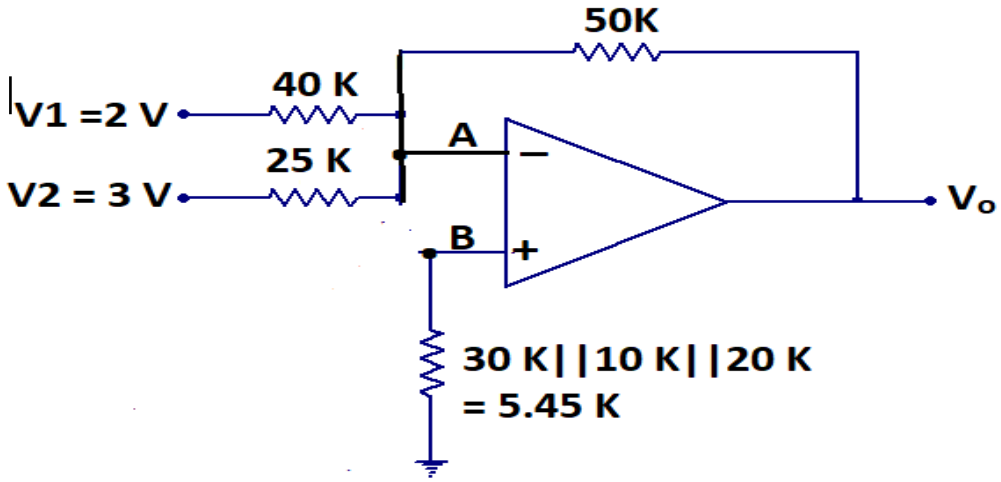
  Because of Non-inverting conflguration
- $V_0 = V_B\left[1 + \frac{R_f}{R}\right]$
- $V_0 = \left[\frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}\right] \times \left[1 + \frac{R_f}{R}\right]$
- $V_0 = \left[\frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}\right] \times \left[\frac{R + R_f}{R}\right]$

- $V_0 = [\frac{V_1 R_2}{R_1+R_2}] \ [\frac{R+R_f}{R}] + [\frac{V_2 R_1}{R_1+R_2}] \ [\frac{R+R_f}{R}]$
- If $R_1 = R_2 = R = R_f$
- $V_0 = [\frac{V_1 R}{R+R}] \ [\frac{R+R}{R}] + [\frac{V_2 R}{R+R}] \ [\frac{R+R}{R}]$
- $V_0 = V1 + V2$
- The output voltage is sum of V1 and V2 and there is no polarity change ie no phase shift

PROBLEM 5. Find V_0 for the circuit shown

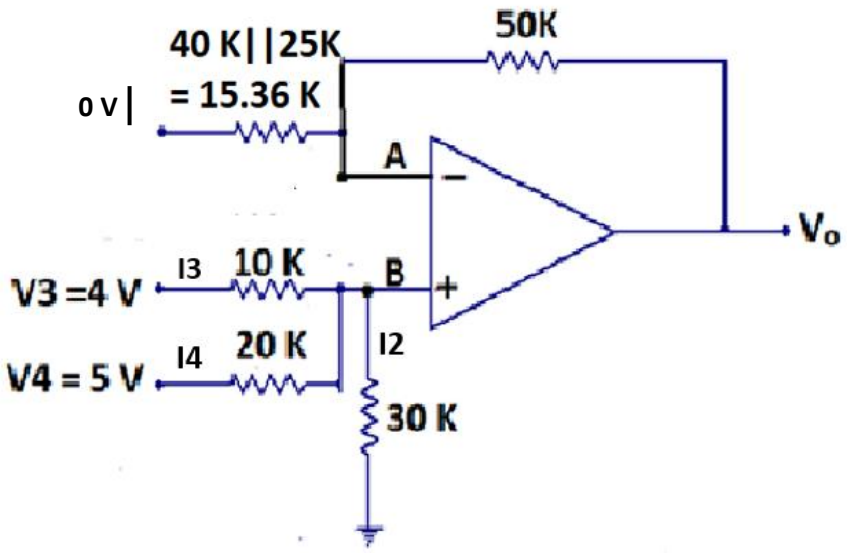


- Use Super position theorem
- 1. Make $V_3 = V_4 = 0$ V and find the value of V_{01}
- 2. Make $V_1 = V_2 = 0$ V and find the value of V_{02}
- 3. $V_0 = V_{01} + V_{02}$



I. Make V_3 and V_4=0

- V3 = V4 = 0 V
- The circuit is equivalent to Inverting configuration
- $V01 = -[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2]$
- $V01 = -[\frac{50\ K}{40\ K}\ 2 + \frac{50\ K}{25\ K}\ 3] = -8.5V$



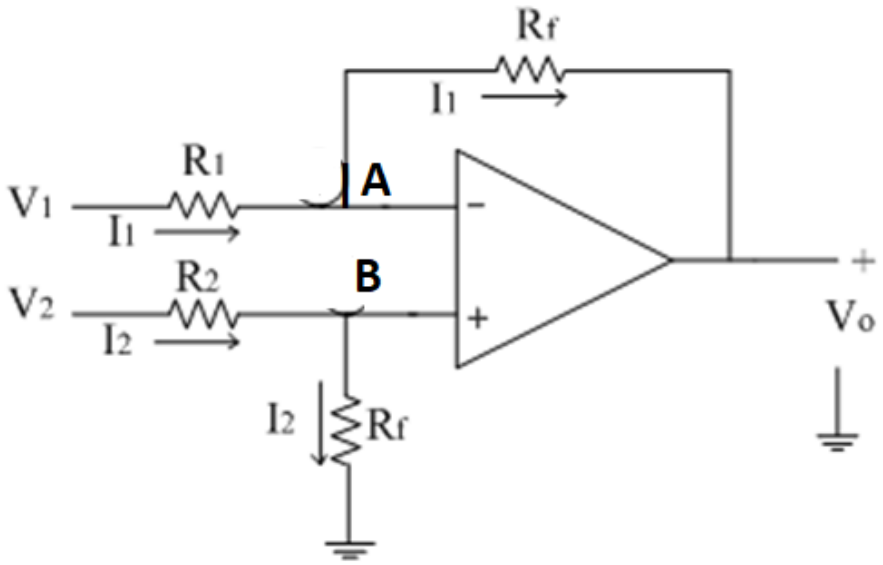
II. Make V1 and V2 =0

- V1 = V2 = 0 V
- $I3 = \frac{V_3 - V_B}{10\ K}$
- $I4 = \frac{V_4 - V_B}{20\ K}$
- $I2 = \frac{0 - V_B}{30\ K}$
- I3 + I4 + I2 = 0
- $\frac{V_3 - V_B}{10\ K} + \frac{V_4 - V_B}{20\ K} + \frac{0 - V_B}{30\ K} = 0$
- $\frac{V_3}{10K} + \frac{V_4}{20K} = \frac{V_B}{10K} + \frac{V_B}{20K} + \frac{V_B}{30K}$
- $\frac{4}{10K} + \frac{5}{20K} = V_B(0.1 + 0.05 + 0.333)10^{-3}$
- V_B = 3.54 V
- $V02 = [1 + \frac{R_f}{R}]\ V_B$
- But R is the parallel combination of 40 K and 25 K

- R = $\frac{40\ K \times 25\ K}{40\ K + 25\ K}$ = 15.36 K
- V02 = [1 + $\frac{50\ K}{15.36\ K}$] V_B = 4.25 ×3.54 = 15.08 V
- $V_0 = V_{02} + V_{01}$ = 15.08 –8.55 = 6.53 V

DIFFERENCE AMPLIFIER / SUBTRACTOR

Q 8. Draw and explain the circuit of subtractor using Op-Amp



- Use super position theorem
- **1**. Make V2 =0 . Calculate the value of Output. Let it be denoted as V01
- **2**. Make V1 =0. Calculate the value of output. Let it be denoted as V02
- **3**. Resultant Output V0 = V01 + V02

I. Make V2 =0

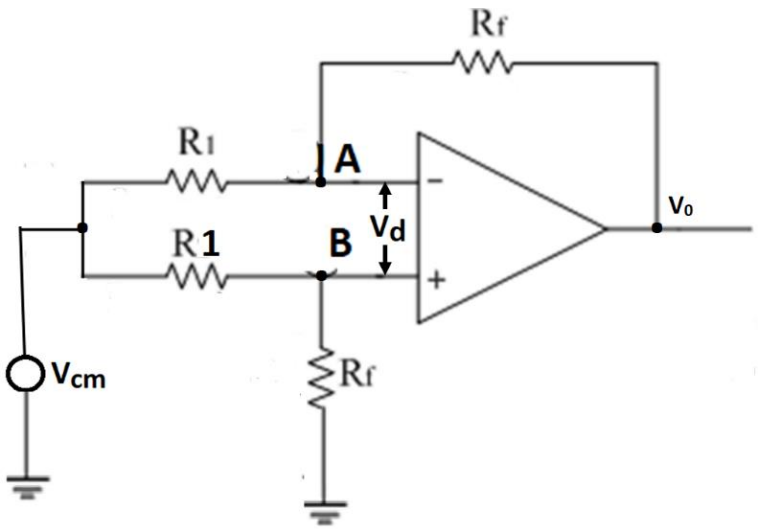
- V2 = 0
- V01 = – $\frac{R_f}{R_1}$ V_1

II.

- V1 =0
- V02 = VB [1 + $\frac{R_f}{R_1}$]
- VB = $\frac{R_f}{R_2 + R_f}$ V2 (potential divider action)

- V02 = $\frac{R_f}{R_2+R_f}$ V2 [1 + $\frac{R_f}{R_1}$]
- But V0 = V01 + V02
- V0 = – $\frac{R_f}{R_1}$ V_1 + $\frac{R_f}{R_2+R_f}$ V2 [1 + $\frac{R_f}{R_1}$]
- If R1 = R2 = R_f = R
- V0 = – $\frac{R}{R}$ V_1 + $\frac{R}{R+R}$ V2 [1 + $\frac{R}{R}$]
- V0 = – V_1 + $\frac{1}{2}$ V2 [1 +1] = V2 –V1
- So the output voltage is difference between the two input voltages

PROBLEM 6. In the circuit shown below R_1 = 100 Ω , R_f = 4.7 KΩ, CMRR =90 dB. If the amplitude of the induced 60 Hz noise at the output is 5 mV (r.m.s). Calculate the amplitude of the Common mode input voltage V_{cm}.



- **Steps to be followed:**
- **1**. We need to find out the value of Vcm
- **2**. Ac = Common mode Gain = $\frac{V_0}{V_{cm}}$

  V_0 is the output voltage and value is given in the problem
- **3**. We need to find out Ac

  CMRR = $\frac{A_d}{A_c}$ where A_d is the Differential gain

  So Ac = $\frac{A_d}{CMRR}$

  Now we need to find A_d Value of CMRR is given in the problem

- **4**. $A_d = \frac{V_0}{V_d}$

  now V_d need to be found out

- **5.** $V_d = V_B - V_A$

  $V_B = \frac{V_{cm}}{R_1+R_f} R_f$ (potential divider action)

  Now we need to find out V_A

- **6**. V_A is because of two voltages V_{cm} and V_0

  Use super position theorem

  a) Make $Vcm = 0$ and find out V_{A1}

  b) Make $V_o = 0$ and find out V_{A2}

  c) $V_o = V_{A1} + V_{A2}$

  7. Find out $V_d = V_B - V_A$

  8. Use $Ad = \frac{V_0}{V_d}$

  9. Get $A_c = \frac{A_d}{CMRR}$

  10. Use $Ac = \frac{V_0}{V_{cm}}$

  11. Find V_{cm}

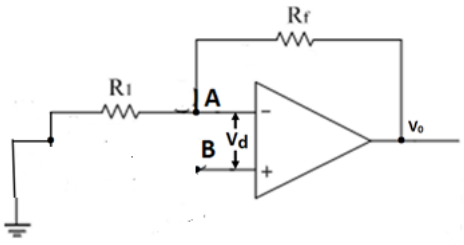
  SOLUTION:

  1. Find out V_B

  $V_B = \frac{V_{cm}\ R_f}{R_1+R_f}$

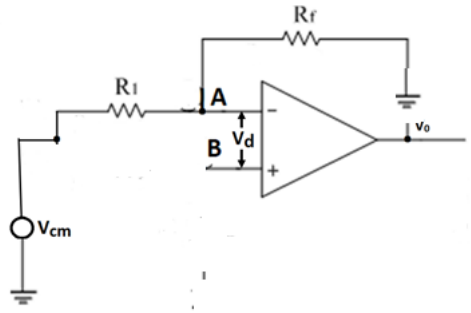
  2. Find out V_A . Use Super position theorem

  Make $V_{cm} = 0$



  $V_{A1} = \frac{V_0\ R_1}{R_1+R_f}$

3. Make V_0 =0



$V_{A2} = \frac{V_{cm}\ R_f}{R_1+R_f}$

4. $V_A = V_{A1} + V_{A2}$

$V_A = \frac{V_0\ R_1}{R_1+R_f} + \frac{V_{cm}\ R_f}{R_1+R_f}$

5. $Vd = VB - VA = \frac{V_{cm}\ R_f}{R_1+R_f} - \frac{V_0\ R_1}{R_1+R_f} - \frac{V_{cm}\ R_f}{R_1+R_f} = -\frac{V_0\ R_1}{R_1+R_f}$

6. $Ad = \frac{V_0}{V_d} = -\left[\frac{R_1+R_f}{R_1}\right]$

7. $CMRR = \left|\frac{A_d}{A_c}\right| = \frac{R_1+R_f}{R_1\ A_C}$ =90 dB= Antilog $\frac{90}{20}$ = 31622.8

$31622.8 = \frac{100+4700}{100\ A_C}$

$Ac = 1.52 \times 10^{-3}$

8. $Ac = \frac{V_0}{V_{cm}} = 1.52 \times 10^{-3}$

9. $V_{cm} = \frac{5\ (10^{-3})}{1.52\ (10^{-3})}$ = 3.29 v (rms)

1 UNIT CONCLUDED

LINEAR INTEGRATED CIRCUIT APPLICATION
(ECE 404 PC)
UNIT -2

OP-AMPS AND APPLICATIONS:

Basic Information of OP-AMP, Instrument amplifier, ac amplifier, V to I and I to V converters, Sample & Hold circuits, multipliers and dividers, differentiators and Integrators, Comparators, Schmitt trigger, multivibrators, introduction to Voltage regulators, features of 723

Text books :

1. Linear integrated circuit by D.Roy chowdhary New Age International(P) Ltd
2. Op=Amps & linear ICs Ramakanth, A,Gayakwad , PHI

BASIC INFORMATION ON OP-AMP

Q 1. What are the salient features of Op-Amps?

- 1. Op-Amp is a differential amplifier with a very large gain which can be assumed to approach infinity for mathematical computations. This is also called open loop gain
- 2. It has two input terminals a) Inverting input b) Non-Inverting input and one output terminal. It requires +ve and –ve supplies.
- 3. For linear applications it is not used in open loop mode but is used in closed loop mode. Feedback network consisting of resistor and capacitor is connected for various linear applications.
- 4. If used in nonlinear mode, its output approximately saturates at +ve supply or –ve supply. This can be used for Comparator operation.
- 4. It has very high input impedance. So its input currents are negligible and can be assumed to be zero.
- 5. It has very low output impedance
- 6. Because of the above, its two input terminals will be assumed to be at the same potential. Thus if one terminal is grounded , the other is assumed to be at ground terminal. This is called Virtual Ground.

INSTRUMENTATION AMPLIFIER

Q 2. List the requirements of good Instrumentation Amplifier

- 1. High gain stability for temperature variations
- 2. Low temperature coefficient. Low thermal drift and low time drift
- 3. High CMRR
- 4. High input impedance
- 5. Low output impedance and low dc offset voltage
- 6. Low power consumption

Q 3. State the necessity and applications of Instrumentation amplifier

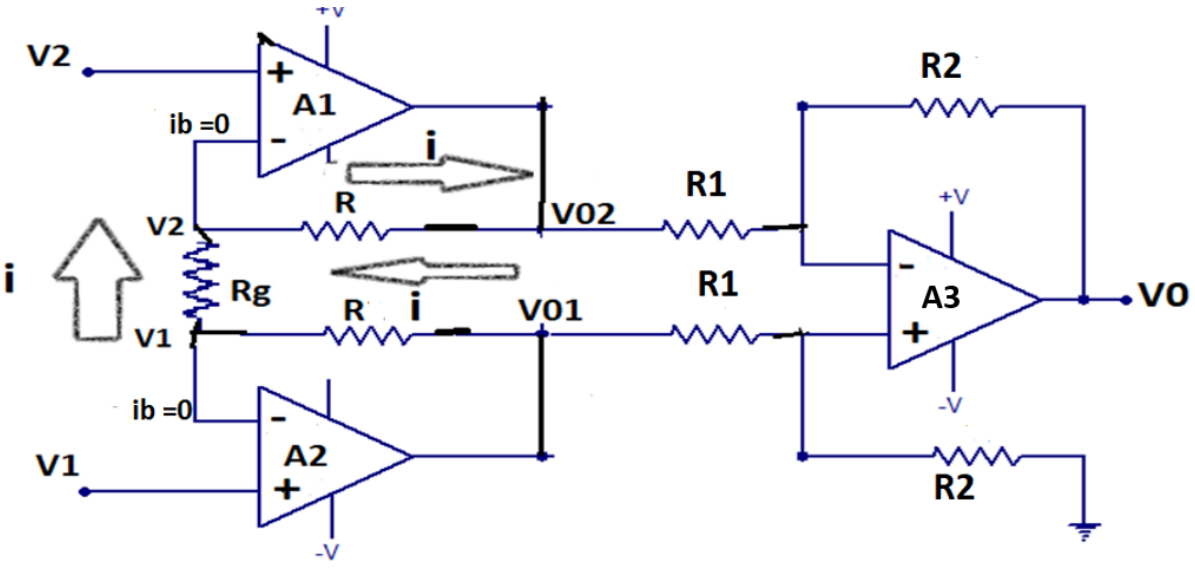
NECESSITY: In industrial and consumer applications , it is necessary to measure and control physical quantities like temperature, humidity, light intensity, water flow etc. Transducers convert the physical quantity to electrical voltage. The output voltage is required to be amplified so that it can be shown on a proper display.

- Normally the transducers have low signal energy. We cannot draw large currents from them. Therefore the Instrumentation amplifier that is connected should have very high input impedance. It should draw very little current from the transducer.
- All transducers will have two terminals +ve and−ve as output. They are connected to IA by long two wires though long distances. The transducers will pick up common mode signals such as noise when transmitted over long wires. So the IA should have to reject the noise present on both the wires. Both the wires will have same noise. This is done by subtraction of signals This is possible when the Instrumentation Amplifier has very high CMRR. Common Mode Rejection Ratio

APPLICATION OF INSTRUMENTATION AMPLIFIER:

- 1. As process control instruments
- 2. Temperature controllers and temperature indicators
- 3. Light intensity meters
- 4. Weight measuring instruments
- 5. Data Acquisition systems

Q4. Draw the circuit diagram of three op-amp Instrumentation Amplifier and explain its operation



INSTRUMENTATION AMPLIFIER

- The first stage consists of A1 and A2 Op-Amps operating in Non inverting mode. This gives high input impedance to the transducers connected at V1 and V2
- Op-Amp A3 is the differential amplifier. Its output
- $V_0 = \frac{R2}{R1}(V01 - V02)$

OPERATION:

- No current flows into op-amps because of high input impedances
- Assume V1 is greater than V2

- Current i flows upwards into resistor **Rg** and passes through Resistor R

$$i = \frac{(V1 - V2)}{Rg}$$

- V1 = Vo1 – I R ie Vo1 = V1 + i R
- Vo1 =V1 + R $\frac{(V1-V2)}{Rg}$
- Vo2 = V2 – i R = V2 –R $\frac{(V1-V2)}{Rg}$
- Vo = $\frac{R2}{R1}$ $(V01 - V02)$ because of Differential amplifier configuration
- Vo = $\frac{R2}{R1}$ $(V1 + R \frac{(V1-V2)}{Rg} - V2 + R \frac{(V1-V2)}{Rg})$
- Vo = $\frac{R2}{R1}$ $[(V1 - V2) + 2R \frac{(V1-V2)}{Rg})]$
- Vo = $\frac{R2}{R1}$ $(V1 - V2)[1 + \frac{2R}{Rg})]$
- Gain = $\frac{Vo}{(V1-V2)}$ = $\frac{R2}{R1}$ $[1 + \frac{2R}{Rg})]$
- Gain = If Rg =50ohms R2=R1 =25 k and R =25 k
- Gain = $\frac{25\,k}{25\,k}$ $\left[1 + \frac{2\times 25\text{k}}{50}\right]$ = 1001
- Rg can be a pot-meter which will control the gain of IA (Instrument Amplifier)

Q 4. State the advantages of three OP-Amp Instrumentation Amplifier

- 1. With the help of external pot-meter the gain can be varied
- 2. The input impedance is very high because the outputs of transducers are connected to Noninverting terminals of Op-Amp
- 3. The output impedance is very Low
- 4. Gain depends on the external resistors connected. High quality resistors can be used and the gain can be made accurate and stable
- 5. CMRR is very high. So Noise is reduced
-

PROBLEM 1. For the Instrument Amplifier determine the value of Rg if the gain required is 1000

- Assume the values of R1 =R2 = 100 KΩ and R = 470 KΩ
- Gain = = $\frac{100\,k}{100\,k}$ $\left[1 + \frac{2\times 470\text{x}1000}{\text{Rg}}\right]$ = 1000 So R_g = 940 ohms(apprx)

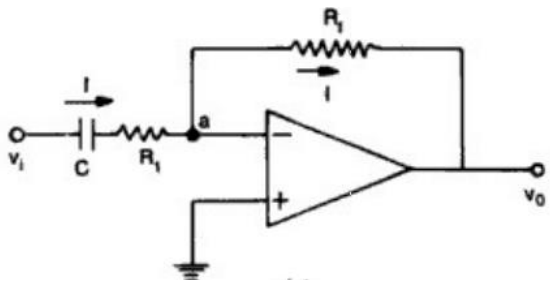
AC AMPLIFIER

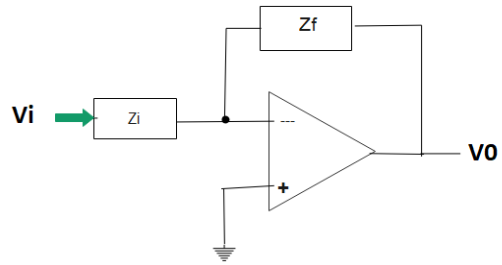
Q 5. What is an AC Amplifier?

- The inverting & Non inverting configurations discussed earlier respond to both DC and AC signals

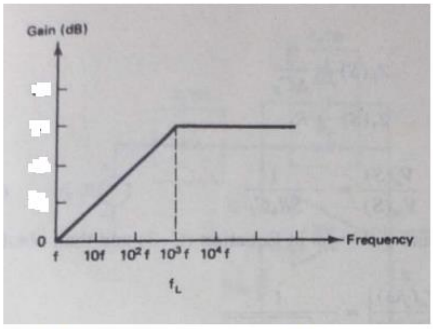
- In case the AC signal is superimposed on DC signal and if it is required to block the DC signal AC amplifiers are used
- The Op-Amp Responding to only AC signals is called AC Amplifier
- AC Amplifiers have low frequency and high frequency limit
- To block the DC signals Coupling capacitors are used

Q 6. Explain Inverting AC Amplifier

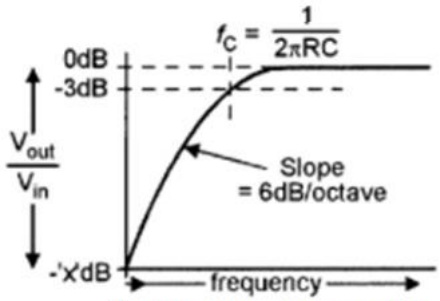




- Gain = $\frac{Vo}{Vi} = -\frac{Zf}{Zi}$
- Zf = Rf and Zi = R + $\frac{1}{SC} = \frac{RSC+1}{SC}$
- $\frac{Zf}{Zi} = -R_f \times \frac{SC}{(RSC+1)} = -\frac{Rf}{R}\frac{SCR}{(RSC+1)} = -\frac{Rf}{R}\frac{SRC}{(SRC+1)}$
- Gain = $-\frac{Rf}{R}\frac{SRC}{(SRC+1)}$
- If Rf = R
- Gain = $-\frac{SRC}{(SRC+1)} = -\frac{2\pi f RC}{1+2\pi f RC}$
- When frequency 'f' is low denominator $(1+2\pi f R C) \rightarrow 1$
- Low frequency gain is $2\pi f RC$ ie gain is directly proportional to frequency 'f'
- When frequency 'f' is high, denominator $(1+2\pi f R C) \rightarrow 2\pi f R C$
- High frequency gain is $\frac{2\pi f RC}{2\pi f RC} = 1$
- For different frequencies the gain plot is given in the graph



Frequency response of ideal AC Amplifier



Frequency response of practical AC Amplifier

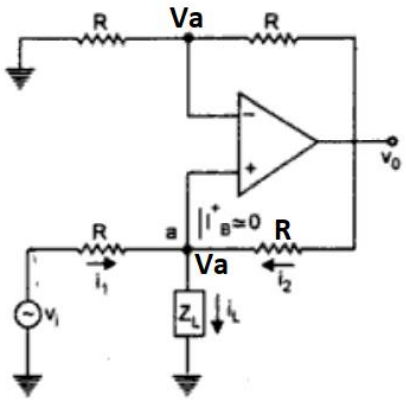
3DB GAIN POINT:

- absolute gain $antilog\left(-\frac{3}{20}\right) = 0.707 = \frac{1}{1.404} = \frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1+1}}$
- Gain = $-\frac{SRC}{(SRC+1)} = -\frac{J2\pi f RC}{1 + J2\pi f RC} = -\frac{1}{1+\frac{1}{J2\pi f RC}} = -0.707 = -\frac{1}{1.404}$
- For what value of 'f' the frequency response gain = −3dB
- Magnitude of $\left(1+\frac{1}{J2\pi f RC}\right)$
- $[1^2 + (\frac{1}{J2\pi f RC})^2] = \sqrt{(1+1)}$ we will find out f = f_C such that
- $1 = \frac{1}{2\pi R fc C}$ so $fc = \frac{1}{2\pi R C}$ where f_C is called the −3dB frequency

VOLTAGE TO CURRENT CONVERTER (V to I)

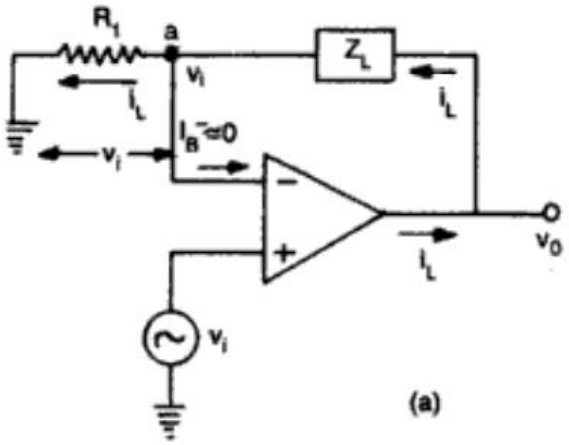
Q 7. With a neat circuit diagram explain V to I converter with grounded load

- One end of load resistor is connected to the output of V to I converter and the other end is grounded.



- Let Va be the voltage at node 'a'
- $i_L = i_1 + i_2$ (since $i_B = 0$)
- $i_L = \frac{V1-Va}{R} + \frac{Vo-Va}{R} = \frac{V1+Vo-2\,Va}{R}$
- $Va = \frac{V1+Vo-i_L R}{2}$ (take V_a to LHS)
- Gain of noninverting amplifier = $\left(1 + \frac{Rf}{Ri}\right)$
- Make Rf =Ri = R
- $Vo = \left(1 + \frac{R}{R}\right) Va = 2\,Va = 2 \times \frac{V_1+V_0-i_L R}{2}$
- $= V1 + Vo - iL\,R$
- $V1 = i_L R$
- $i_L = \frac{V1}{R}$
- The above equation shows the load current i_L depends on V1 and the resistor R

Q 8. With a neat circuit diagram, explain V to I converter for a floating load



i_L is the load current

$Vi = i_L\ R1$ (since $i_B = 0$)

$$i_L = \frac{Vi}{R1}$$

- So the current i_L flowing in the load Z_L is proportional to input voltage Vi
- Op-amp must be capable of providing this load current
- So the load current is proportional to the input voltage
- If the load is a capacitor it will charge or discharge at a constant rate. This property can be used to generate sawtooth or triangular waveforms

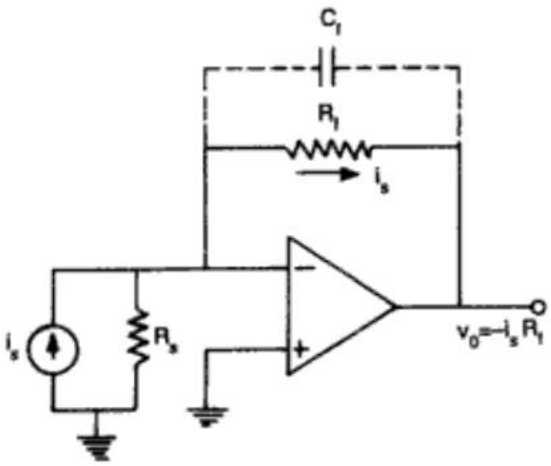
Q 9. State the applications of V to I converter

- 1. Low voltage AC voltmeter
- 2. Low voltage DC voltmeter
- 3. Diode tester
- 4. Zener diode tester

CURRENT TO VOLTAGE (I to V) CONVERTER

Q 11. With a neat circuit diagram, explain current to voltage converter

- In I to V converter the output voltage is proportional to the input current
- The (−) terminal is at ground potential since (+) terminal is grounded. So no current flows through resistor R_s .
- $Vo = -i_s R_f$ So Vo is proportional to i_s
- The lowest current this circuit can measure will depend on bias current I_B
- 741 op-amp has I_B = 3 nano amp
- Sometimes Ci is shunted to reduce noise



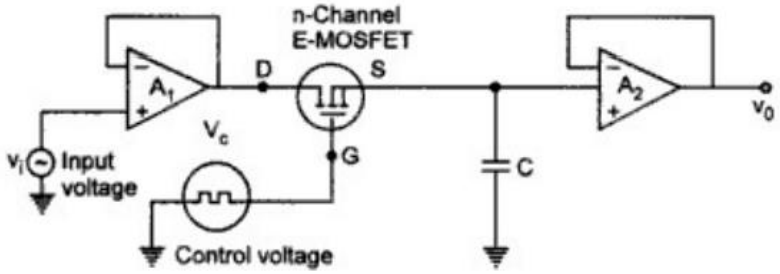
Q 12. State the applications of I to V converter

- 1. Some Transducers like photocell, photodiode, photovoltaic cell etc, give an output current. The current through these devices can be converted to voltage. The applications include a) photo diode detector b) Photo FET detector

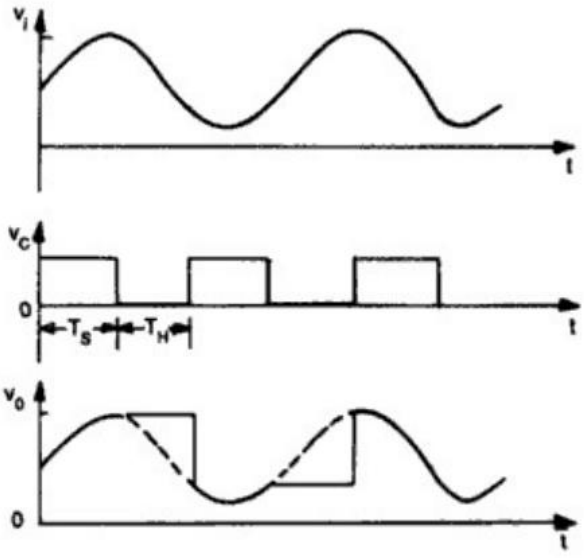
- Thus the amount of light or radiant energy incident can be measured by measuring the voltage. This is done by I TO V converter.

SAMPLE AND HOLD CIRCUIT

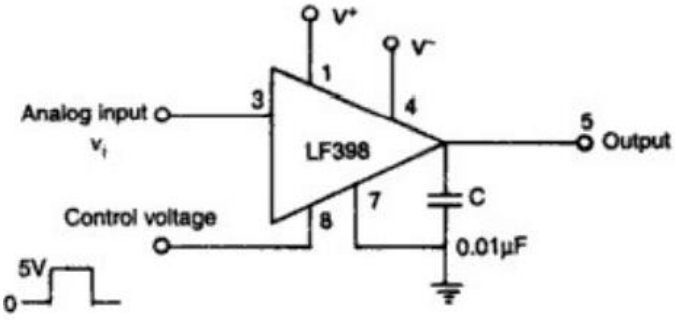
Q 13. Draw and explain Sample and Hold circuit using Op-Amp



- The S/H circuit samples the analog input signal for a short time when the MOSFET switch closes in response to a sampling command. It holds the analog signal at the output until a new sampling command is given to the switch.
- A1 is the Buffer amplifier and provides high input impedance to the input signal
- The switch used between A1 buffer and storage capacitor is the n-channel E-MOSFET switch.
- The switch is controlled by the control voltage **VC**
- When **VC** is positive the switch turns on, and the capacitor C charges to the instantaneous value of input Vi . The capacitor C charges with a time constant of
- [Ro + rDS] × C
- Ro = output resistance of voltage follower A1
- rDS = on resistance of n- channel switch
- Since both the values are small the Capacitor C quickly charges to the input Voltage Vi
- Voltage follower A2 has very high input impedance. It does not load capacitor C. it retains the charge during Hold mode.
- When v_c =0 the MOS FET switch is off
- During the sampling period the voltage across capacitor C is equal to the input voltage since the charging time constant is very small. This is called Sampling period Ts
- During the Hold period T_H the switch is OFF. The voltage across capacitor is held constant. This is called Hold period or hold time
- The frequency of the control (sampling) voltage should be kept higher than twice the input frequency as per Nyquist theorem
- S/H circuits are extensively used in A/D converters
- In commercial market ready- made S/H ICs are available .
- EX: HA2420 (Harris Semiconductor) LF 198, LF 398 (National semiconductor)



Input and output waveforms



Q 14. State the applications of Sample and Hold circuit

- 1. Analog to Digital converter
- 2. Pulse modulation
- 3. Digital interfacing circuits
- 4. Multiplexer circuits

Q 15. Draw the circuit of Log Amplifier and derive the expression for its output voltage

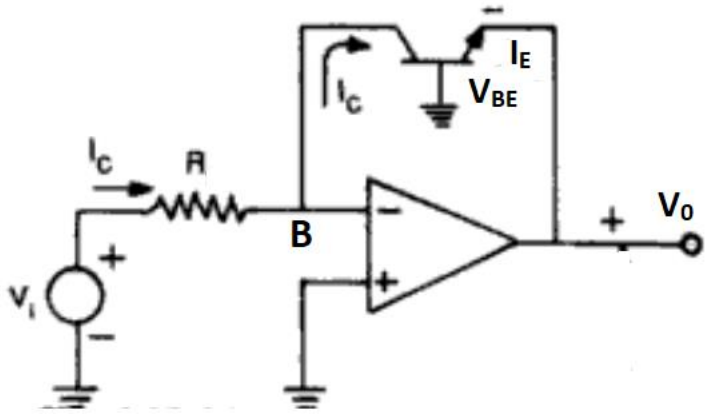
- The Log amplifier consists of a Op-Amp using a BJT (transistor) as a diode in the negative feedback of an Op-Amp
- From transistor theory $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$

  Where V_{BE} = Voltage between base and emitter

  I_C = collector current

  I_S = emitter saturation current

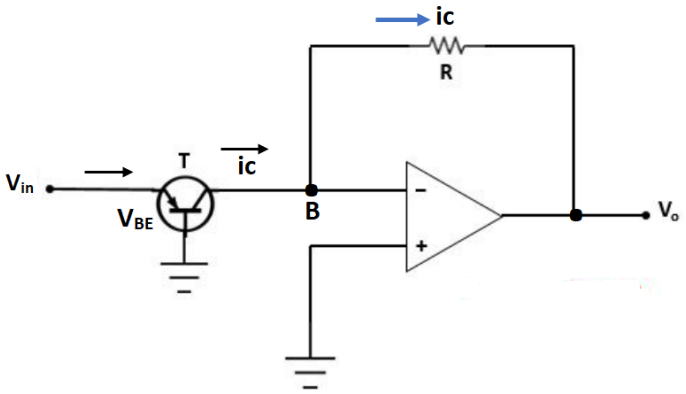
  V_T = diode's thermal equivalent voltage (assumed to be constant for a given transistor)



- Voltage at node B = 0 since it is at virtual ground.
- No current flows into Op-Amp from node B
- Ic = $\frac{V_{in}}{R}$ where ic is collector current
- V_{CB} = 0 since collector is at virtual ground and emitter is grounded. So the transistor can be considered as a diode
- $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$
- $V_0 + V_{BE} = 0$
- $V_{BE} = -V_0$
- $V_{BE} = V_T \ln\left(\frac{\frac{V_{in}}{R}}{I_S}\right) = V_T \ln\left(\frac{V_{in}}{R\, I_S}\right) = V_T \ln\left(\frac{V_{in}}{V_{ref}}\right)$
- $V_{BE} = V_T \ln\left(\frac{V_{in}}{V_{ref}}\right) = -V_0$
- $V_0 = -V_T \ln\left(\frac{V_{in}}{V_{ref}}\right)$
- Since V_T and V_{in} are constants
- The output V_0 is proportional to ln of (V_{in})

Q 16. Draw the circuit of anti- Log Amplifier and derive the expression for its output voltage

- Anti-logarithmic or exponential **amplifier** (or simply **antilog amplifier**) is an **op-amp** circuit configuration, whose output is proportional to the exponential value or anti-log value of the input. **Antilog amplifier** does the exact opposite of **a log amplifier.**



- Node B is at virtual ground and VCB = 0
- $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$
- $\frac{V_{BE}}{V_T} = \ln\left(\frac{I_C}{I_S}\right)$
- Taking anti-logarithms both sides
- $I_C = I_S \ e^{\frac{V_{BE}}{V_T}}$
- $I_C = \frac{-V_o}{R} = I_S \ e^{\frac{V_{BE}}{V_T}}$
- $V_O = -R\, I_S \ e^{\frac{V_{BE}}{V_T}} = -V_{ref} \ e^{\frac{V_{BE}}{V_T}} = -V_{ref} \ e^{\frac{V_{in}}{V_T}}$ because $V_{in} = V_{BE}$
- $V_O = -V_{ref} \ e^{\frac{V_{in}}{V_T}}$
- ∴Output voltage is proportional to the exponential of V_{in} ie antilog of V_{in}

MULTIPLIERS AND DIVIDERS

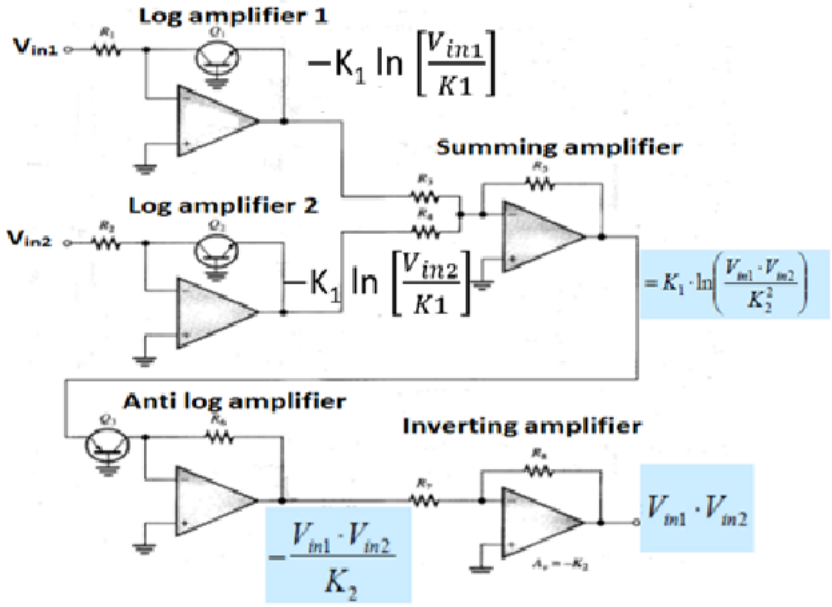
Q 16. Draw and explain the operation of Analog multiplier using Op-Amp

The output of Log amplifiers are stated as follows

$$V_{out(\log 1)} = -K_1 \cdot \ln\left(\frac{V_{in1}}{K_2}\right)$$

$$V_{out(\log 2)} = -K_1 \cdot \ln\left(\frac{V_{in2}}{K_2}\right)$$

Where $K_1 = V_T$ and $K_2 = \frac{1}{V_{ref}}$



The two outputs from Log Amplifiers are added and inverted by the unity gain summing amplifier to produce the result as follows

$$V_{out(sum)} = K_1 \cdot \ln\left[\ln\left(\frac{V_{in1}}{K_2}\right) + \ln\left(\frac{V_{in2}}{K_2}\right)\right] =$$

$$= K_1 \cdot \ln\left(\frac{V_{in1} \cdot V_{in2}}{K_2^2}\right)$$

The above output is applied to the Antilog amplifier. The output of Antilog amplifier is given as below

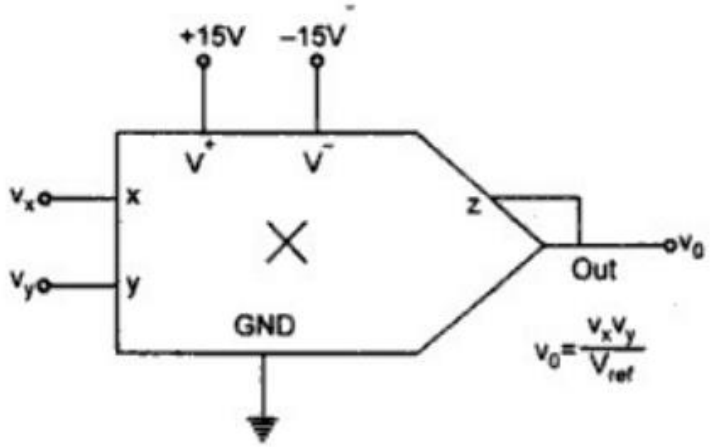
$$V_{out(\exp)} = -K_2 \cdot \exp\left(\frac{V_{out(sum)}}{K_1}\right) = -K_2 \cdot \exp\left[\frac{1}{K_1} K_1 \cdot \ln\left(\frac{V_{in1} \cdot V_{in2}}{K_2^2}\right)\right] =$$

$$= -K_2\left(\frac{V_{in1} \cdot V_{in2}}{K_2^2}\right) = -\frac{V_{in1} \cdot V_{in2}}{K_2}$$

The output of the Anti-log amplifier is given to a constant $\frac{1}{K_2}$ times the product of input voltages. The final output is obtained by passing the signal through an Inverting amplifier with a gain of $-K_2$

$$Vout = -K_2\left(-\frac{V_{in1} \cdot V_{in2}}{K_2}\right) = V_{in1} \cdot V_{in2}$$

Q 17. Explain the four quadrant multiplier IC and state its applications



- The multiplier gives out the product of two input signals
- The multiplier requires Dual supplies generally $\pm$ 15 volts
- V_X and V_Y the two inputs to the Multiplier
- Output V_0 = K V_X V_Y where K is a constant and is equal to $\frac{1}{V_{ref}}$
- V_{ref} is set to 10 V internally
- $V_0 = \frac{V_X V_Y}{10}$
- Both inputs should be below V_{ref} so that the output will not saturate

QUADRANT OPERATION OF MULTIPLIER:

- The polarity of both the inputs of the Multipliers determines the classification of Multipliers
- **1. ONE QUADRANT MULTIPLIER** : The polarities of both the inputs should be positive only
- **2, TWO QUADRANT MULTIPLIER**: One input is held positive and the second input can be positive or negative
- **3. FOUR QUADRANT MULTIPLIER:** Both the inputs are allowed to swing in both positive and negative polarities

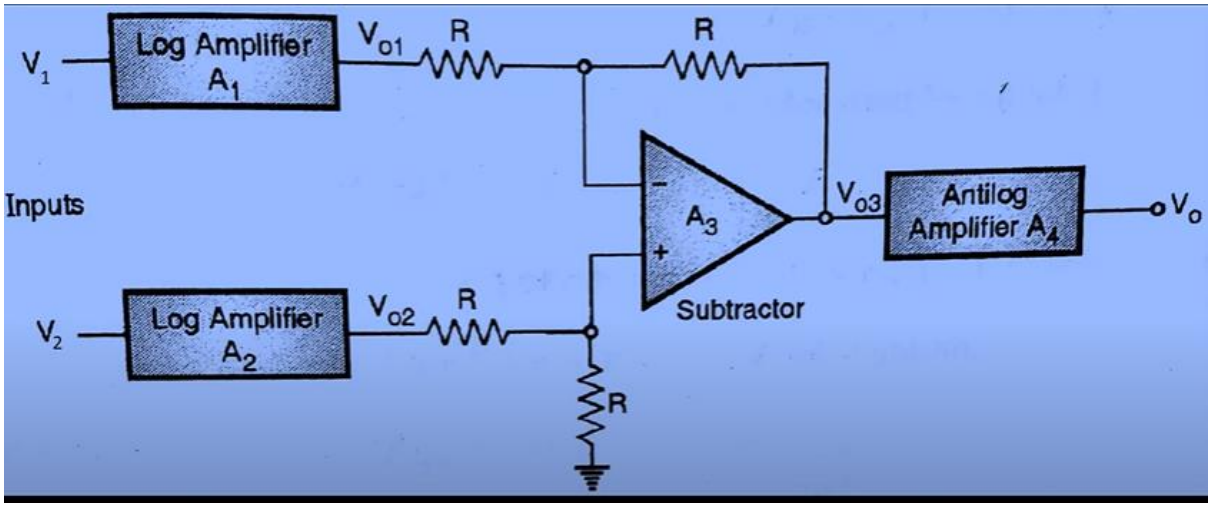
Q 18. What are the applications of Multipliers?

- 1. Squarer
- 2, Square Rooter
- 3. Frequency Doubler
- 4. Phase Angle Detector
- 5. RMS detector

Q 19. Draw and explain the operation of Analog Divider using op-amp

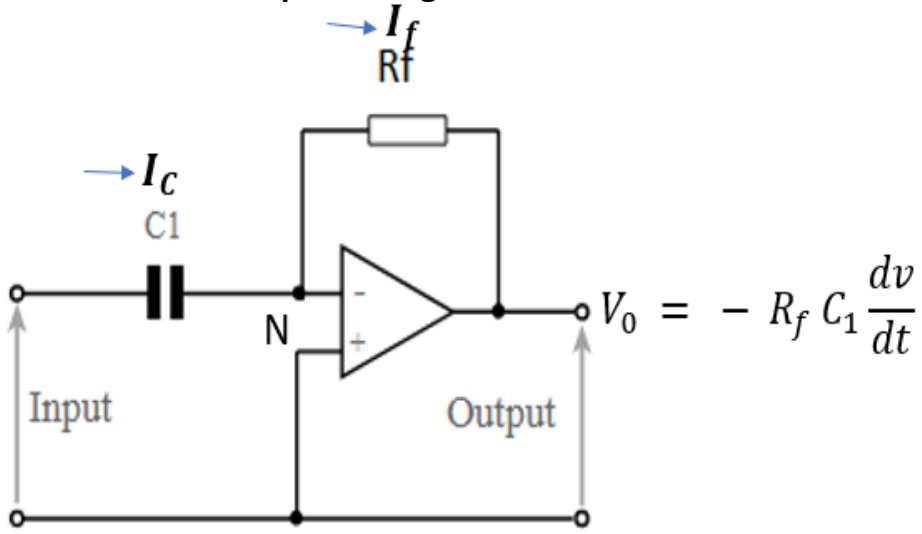
- Analog divider is a circuit in which the output voltage is proportional to division of input voltage
- The out puts of Log amplifiers are give as
- $V_{o1} = K_1 \ln K_2 V_1$
- $V_{o2} = K_2 \ln K_2 V_2$

- The output of Difference Amplifier is
- $V_{03} = V_{02} - V_{01} = K_1 \ln K_2 V_2 - K_1 \ln K_2 V_1$
- $V_{03} = K_1 \ln \left(\frac{V_2}{V_1}\right)$
- This signal is given to the Antilog amplifier which gives
- $V_0 = \frac{1}{K_2} \ln^{-1} K_1 \left[\frac{\ln \frac{V_2}{V_1}}{K_1}\right] = \frac{1}{K_2} \left(\frac{V_2}{V_1}\right)$
- The output is proportional to the division of the two analog inputs

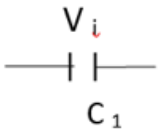


OP-AMP DIFFERENTIATOR

Q 20. Draw the circuit diagram of the Op-Amp Differentiator and derive the expression for its output voltage



- The node N is virtually grounded



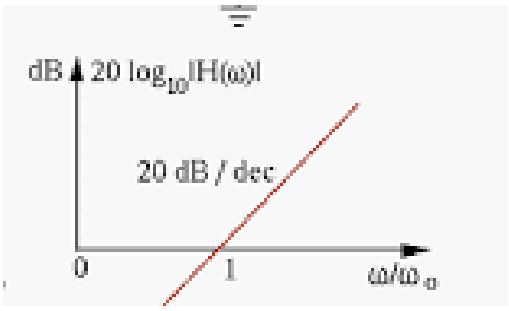
-

- Current flowing in capacitor C1 = ic = C1 $\frac{d\,v_i}{d\,t}$
- $i_f = \frac{0 - v_0}{R_f} = -\frac{-v_0}{R_f}$
- But $i_C = i_f$
- $i_C = C1\,\frac{d\,v_i}{d\,t} = i_f = \frac{-v_0}{R_f}$
- $v_0 = -R_f\,C1\,\frac{d\,v_i}{d\,t}$
- output v_0 = derivative of v_i input voltage multiplied by – (Rf C1)
- — ve sign indicates 180 deg phase shift

Gain for different frequencies :

- Gain G =

  Gain = $\frac{\text{Feed back impedance}}{\text{Input impedance}} = \frac{Z_f}{Z_i}$
- $Zf = Rf \text{ and } Zi = \frac{1}{j\omega\, c1}$
- $G = \frac{v_o}{v_i} = -\frac{R_f}{\frac{1}{J\omega C_1}} = -R_f C_1 J\omega = -J\omega R_f C_1$
- $|G| = |-j\,\omega\,R_f\,C1| = \sqrt{(\omega\,R_f\,C1)^2} = (\omega\,R_f\,C1) = (R_f\,C1\,2\,\pi\,f)$
- R_f and $C1$ are constants $|G| \propto f$
- Gain increases with frequency at a rate of + 20 dB /decade. At higher frequencies it becomes large. This leads to instability and noise problems
- $$|G| = \frac{f}{\frac{1}{2\pi R_f\,C1}} = \frac{f}{f_a}$$
- Where $f_a = \frac{1}{2\pi R_f\,C1}$
- At $f = f_a$
- |G| = 1 ie 20 log 1 =0 dB
- $|G| \propto f$; if Frequency is increased to 10 f, |G| increases by 10 times
- 20 log 10 = + 20 dB. So the gain increases at a rate of +20 dB /decade
- (decade =10)



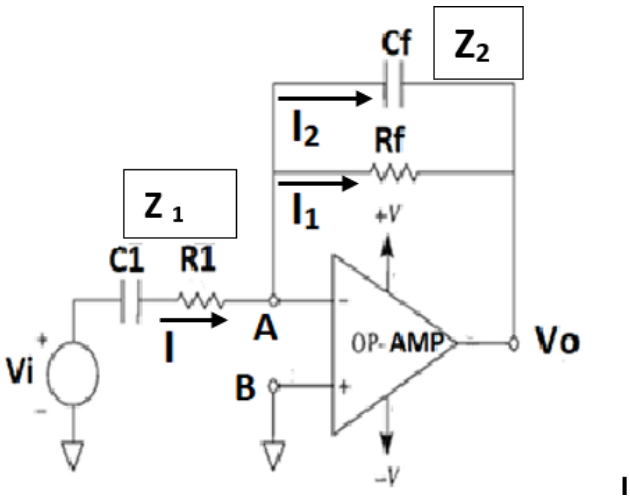
Q 21. What are the limitations of an ideal Differentiator?

- 1. Since $|G|$ is directly proportional to frequency $(\propto f)$, as the frequency of input frequency increases the gain also increases uncontrollably. At high frequencies the gain becomes very large leading to unstability , It may break into oscillations.
- 2. There is a possibility that the op=amp may go into oscillations
- 3. Noise at high frequencies will be amplified enormously since the gain is high at higher frequencies
- 4. The input impedance $\frac{1}{J\,\omega C1}$ decreases with frequency

Q 22. List the applications of Differentiator

- 1. wave shaping requirements
- 2. Determining rate of change of various signals

Q 23. Draw and explain the circuit of a practical Differentiator



Z1

I

$V_A = V_B = 0$ (Because of virtual ground)

$I = \frac{V_{in} - V_A}{Z_1} = \frac{V_{in}}{Z_1}$ where $Z1 = R1 + \frac{1}{S\,C_1}$

$I = \frac{S\,C_1\,V_{in}\,(s)}{(1 + S\;R_1C_1)}$

$$I_1 = \frac{V_A - V_0}{R_f} = -\frac{V_0}{R_f}$$

$$I_2 = C_f \frac{d\,(V_A - V_0)}{dt}$$

$$= -\,C_f \frac{d\,V_0}{dt}$$

Taking laplace transform $I_2(s) = -S\,C_f\,V_0(s)$

But $I = I_1 + I_2$

$$\frac{S\,C_1\,V_{in}(s)}{(1 + S\,R_1 C_1)}$$

$$-\frac{V_0}{R_f} - S\,C_f\,V_0(s)$$

$$V_0(s) = \frac{-\,S\,R_f\,C_1\,V_{in}(s)}{(1 + S\,R_f\,C_f)\,(1 + S\,R_1\,C_1)}$$

To make the equation simple $R_f\,C_f = R_1\,C_1$

$$\frac{V_0(s) = \left(-\,S\,R_f\,C_1\,V_{in}(s)\right)}{(1 + S\,R_1\,C_1)^2}$$

But $R_f\,C_1$ is much greater than $R_1\,C_1$

$$V_0(s) = -S\,R_f\,C_1\,V_{in}(s)$$

Taking inverse Laplace transforms

$$V_0(t) = -R_f\,C_1\,\frac{d\,V_{in}(t)}{dt}$$

PROBLEM 1.

Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 500 Hz. Draw its frequency response,
If a Sine wave of 2 V peak at 500 Hz is applied to the differentiator , write expression for its output and draw output wave form

$$G = -\frac{j\,\frac{f}{fa}}{\left(1 + j\,\frac{f}{fb}\right)^2}$$

$$f_a = \frac{1}{2\,\pi\,R_f\,C_1}$$

$$f_b = \frac{1}{2\,\pi\,R_1\,C_1} = \frac{1}{2\,\pi\,R_f\,C_f}$$

f_a = 500 Hz

Choose C_1 = 0.1 μF

$$f_a = \frac{1}{2\pi R_f C_1} = 500 = \frac{1}{2\pi R_f (0.1)(10^{-6})}$$

R_f = 3183 Ω

f_b is normally chosen 10 times f_a . So $f_b = 5000Hz$

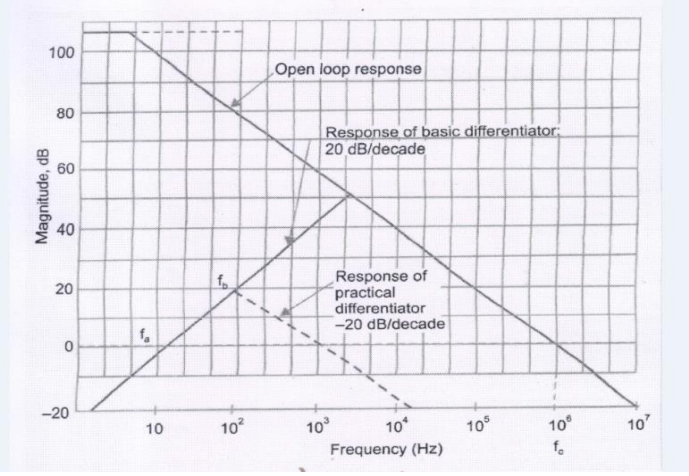
$$R_1 C_1 = R_f C_f$$

5000 =

$$\frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_1 (0.1)(10^{-6})}$$

$$R_1 = 318.3\,\Omega$$

$$C_f = \frac{R_1 C_1}{R_f} = 10 \times 10^{-9}\ \text{F} = 10\ \text{nF}$$



V_{in} = 2 sin (2π f t) = 2 sin (2 π (500) t)

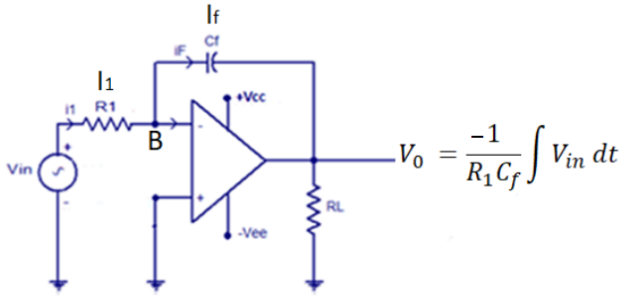
$$V_0(t) = -R_f C_1 \frac{dV_{in}}{dt} =$$

$$-3183\,(-.1)(10^{-6})(2)(3.141)Cos\,(2\pi\,(500)t) = -2\,Cos\,(3141.5\,t)$$

OP-AMP INTEGRATOR

Q 24. Draw an Ideal integrator circuit using Op-Amp and derive expression for its output

- A circuit in which the output voltage is the integral of current is called INTEGRATOR. Integrator is obtained by replacing the feedback resistor in a Inverting op amp circuit with a Capacitor



- Let at node B (-ve teriminal) voltage is v_x
- From Kirchoff 's law $I_1 = I_f$
- Relationship between current and voltage across a capacitor is

$I_c = C \frac{dv_c}{dt}$

$\frac{v_{in} - v_x}{R1} = C \frac{d}{dt}(v_x - v_o)$

But v_x =0 (Voltage between + ve and – ve teriminal is zero)

$\frac{vin}{R1} = C \frac{d}{dt}(-vo)$

Integrating both sides with respects to time

$$\int_0^t \frac{v_{in}}{R_1}\, dt = \int_0^t C \frac{d}{dt}(-v_o)$$

(Assume initial condition as zero)

$$\int_0^t \frac{v_{in}}{R_1}\, dt = C\ (-v_o)$$

$$v_o = -\frac{1}{R_1\ C} \int_0^t v_{in}\ dt$$

- 1. So as per the equation the output $v_o = -\frac{1}{R_1\ C}$ times of integral of input v_{in}. R_1 C_f is called the time constant
- 2. The negative sign indicates that there is a shift of 180^0

Q 25. Mention the limitations of ideal integrator

1. In the absence of input signal the following happens.

a) Due to the high DC gain the input offset voltage gets amplified and the Op-amp may go into saturation

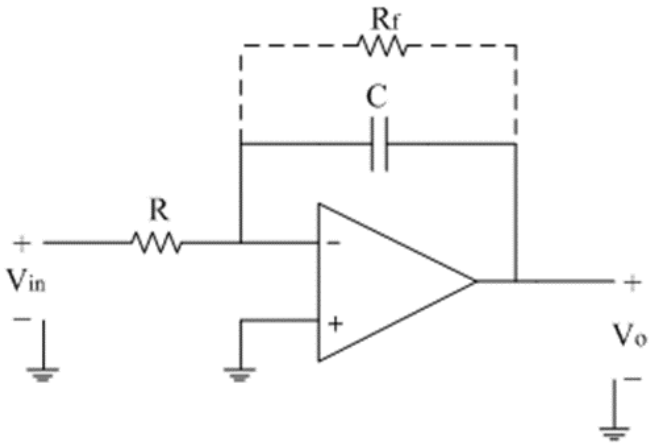
b) Bias current slowly charges the capacitor and Op-Amp goes into saturation

2. In the presence of input signal also the offset voltage and bias current appear as error voltages at the output

3. The bandwidth of ideal integrator is very small

Q 26. Draw the circuit of Practical Integrator and derive the frequency response

- The limitations of an ideal integrator can be minimized in the practical circuit by adding resistor R_f in parallel with capacitor C thus Rf avoids op-amp going into open loop configuration at low frequencies
-



The voltage gain 'A' is given by the equation as follows

$$A = \frac{R_f \| X_c}{R}$$

$$\therefore A = \frac{\left[\frac{R_f \times \frac{1}{j\omega C}}{R_f + \frac{1}{j\omega C}} \right]}{R}$$

$$\therefore A = \frac{\left[\frac{R_f}{j\omega C R_f + 1} \right]}{R}$$

$$\therefore A = \frac{R_f}{R(j\omega C R_f + 1)}$$

$$\therefore A = \frac{R_f}{R} \left[\frac{1}{(j2\pi f C R_f + 1)} \right]$$

Let $f_a = \frac{1}{2\ \pi\ R_f\ C}$ = Break frequency or Corner frequency

$$A = \frac{R_f}{R} \left[\frac{1}{1 + j\left(\frac{f}{f_a} \right)} \right]$$

Where f=Operating frequency
The magnitude of gain A is

$$|A| = \left| \frac{R_f}{R} \left[\frac{1}{1 + j\left(\frac{f}{f_a}\right)} \right] \right|$$

$$|A| = \left| \frac{R_f}{R} \left[\frac{1}{\sqrt{1 + \left(\frac{f}{f_a}\right)^2}} \right] \right|$$

Consider the following cases:

1. When f=0 ,the gain |A|= $\frac{R_f}{R}$ ——dc gain
2. When 0<f<fa ,the gain |A|≅ $\frac{R_f}{R}$
3. When f>fa ,the gain |A|≪ $\frac{R_f}{R}$
4. When f= fa , the gain |A|= $\frac{R_f}{R\ (\ (1/\sqrt{2})}$ Hence, |A|=|0.707 $\frac{R_f}{R}$ |

the gain in dB is given as

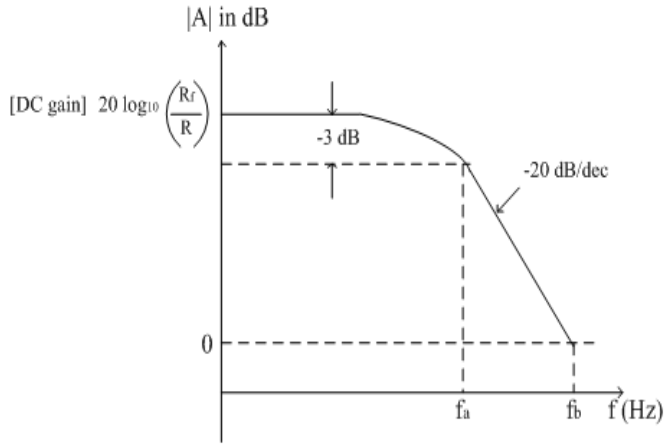
20log |A|=20log |0.707 $\frac{R_f}{R}$|

|A| in dB=20log (0.707)+20log ($\frac{R_f}{R}$)

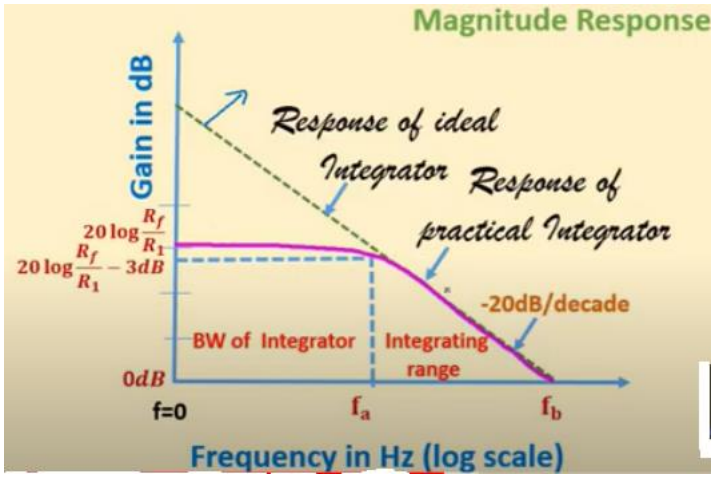
|A| in dB=20log ($\frac{R_f}{R}$) – 3dB

|A| in dB=DC gain (i.e.maximum gain) – 3dB

Thus the frequency fa is the frequency at which gain is reduced by 3 dB from its maximum value. Hence frequency fa is also called as 3dB frequency.
From ideal integrator response, we have defined frequency fb which is 0dB frequency (or unity gain frequency).
The detailed frequency response of practical integrator is shown in figure below



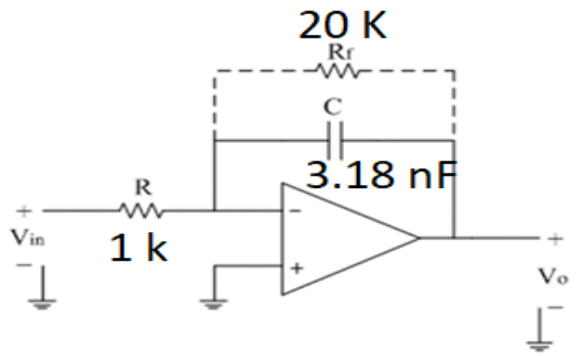
- Between the frequency ranges fa to fb the response is highly linear and dropping at the rate of –20dB/decade. Thus the frequency range fa to fb is referred as true integration range where actual integration of the input signal is possible.
- Thus the true integration is possible over the range $fa < f < fb$
- The practical integrator is also called as lossy integrator as it integrates only frequencies greater than fa (i.e. higher frequencies) effectively.
- Thus we can have following observations from frequency response of practical integrator:



1. Bandwidth of practical integrator is fa which is higher than BW of an ideal integrator.
2. DC gain (at f=0) is $|\frac{R_f}{R}|$ which is typically ≥10.
3. For better integration fb ≥ 10 fa.
4. For proper integration Time period T of input signal ≥ R_f C

PROBLEM 2. Design a practical integrator circuit with a DC gain of 20 to integrate a square wave of 25 KHz

- DC gain = $\frac{R_f}{R_1} = 20$
- f_{in} = 25 000 Hz
- For proper integration $f_{in} > 10\ f_a$
- f_a = 2500 Hz = $\frac{1}{2\pi C_f R_f}$
- $R_f C_f = 6.366 \times 10^{-5}$
- Choose R1 = 1000Ω then $R_f = 20000$
- $C_f = \frac{6.366 \times 10^{-5}}{20000}$ = 3.18 (10^{-9}) = 3.18 nF



PR0BLEM 3. Find R1 and R2 in the lossy integrator so that the peak gain is 20 dB down from its peak when ω = 10,000 rad/sec , use a capacitor value of 0.01 μF

Peak gain = 20 db = $20 \log \frac{R_f}{R_1}$

$\frac{R_f}{R_1} = 10$

At $\omega = 10{,}000$ rad/sec , gain is down by 3 dB from its peak value ie $20-3 = 17$ dB

$$\left[20\, log \frac{\frac{R_f}{R_1}}{\sqrt{1 + \left([\![\frac{f}{f_a}]\!] \right)^2}} \right] = 17$$

$$\mathrm{f} = \frac{\omega}{2\,\pi} = \frac{1000}{2\,\pi} = 1592$$

$$\mathrm{Log} \left[\frac{10}{\sqrt{1+\left([\![\frac{1592}{fa}]\!] \right)^2}} \right] = \frac{17}{20} = 0.85$$

$$\left[\frac{10}{\sqrt{1+\left([\![\frac{1592}{fa}]\!] \right)^2}} \right] = 7.08$$

$$1 + (\frac{1592}{f_a})^2 = 1.996$$

$f_a = 1595$ Hz $= \frac{1}{2\,\pi\, C_f\, R_f}$

Choose $C_f = 0.01 \mu F$

$R_f = 9.97\ k\Omega = 10\mathrm{K}\Omega$

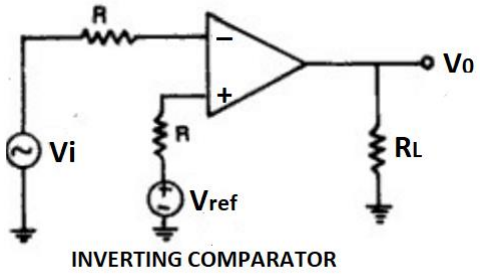
$R_1 = \frac{R_f}{10} = 1K\Omega$

COMPARATORS

Q 27. Explain the use of op- amp as a Comparator

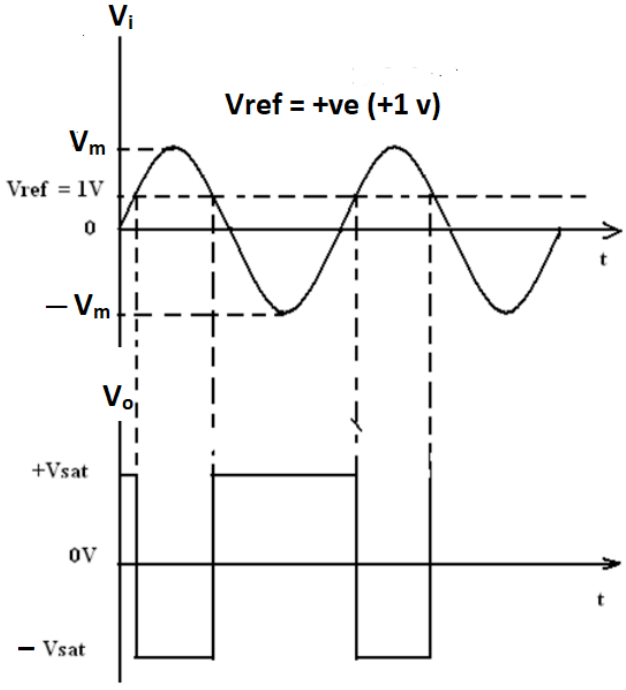
- OP-Amp in open loop configuration functions in a nonlinear manner.
- This function is used to configure a Comparator
- Comparator has two inputs. i) One input is the reference voltage ii) second input is the input voltage.
- Output is either $+V_{sat}$ or $-V_{sat}$. Output changes from $+V_{sat}$ to $-V_{sat}$ or vice versa, with a small increment in input of only 2 Milli Volts between + **input** terminal and **–input** terminal
- There are two types of Comparators i) Inverting Comparator
- and ii) NonInverting Comparator
- **INVERTING COMPARATOR:**

  V_{ref} is applied to (+ input terminal)
- Time varying signal is applied to − input terminal
- Output is at $+V_{sat}$ for $V_i < V_{ref}$ because the voltage at the –input is less than that at the + input
- Output is at $-V_{sat}$ for $V_i > V_{ref}$



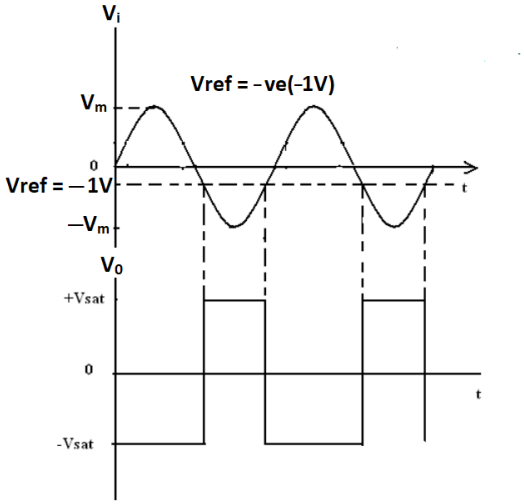
INVERTING COMPARATOR

- Input and output waveforms for the comparator when the reference is +1 volt is shown below



Q 28. Draw the Inverting comparator using Op-Amp with negative reference and explain its operation with waveforms

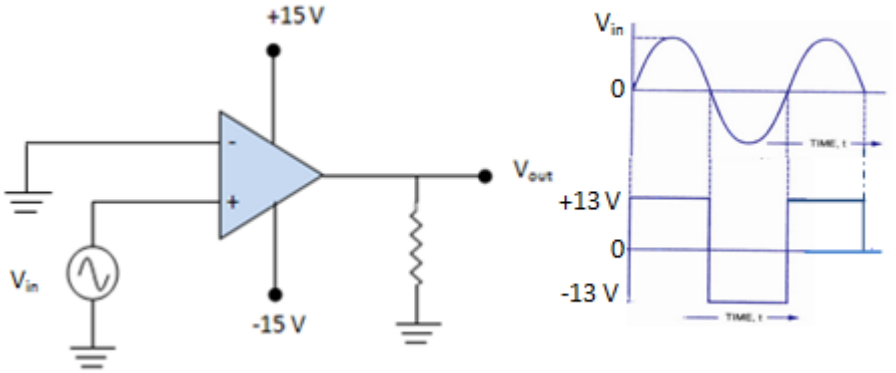
- V_{ref} is applied to (+ input terminal)
- Time varying signal is applied to − input terminal
- Output is at $-V_{sat}$ for $V_i > V_{ref}$ because the voltage at the –input is greater than that at the + input
- Output is at $+V_{sat}$ for $V_i < V_{ref}$



Q 27. Explain the working of Op-Amp as zero crossing detector

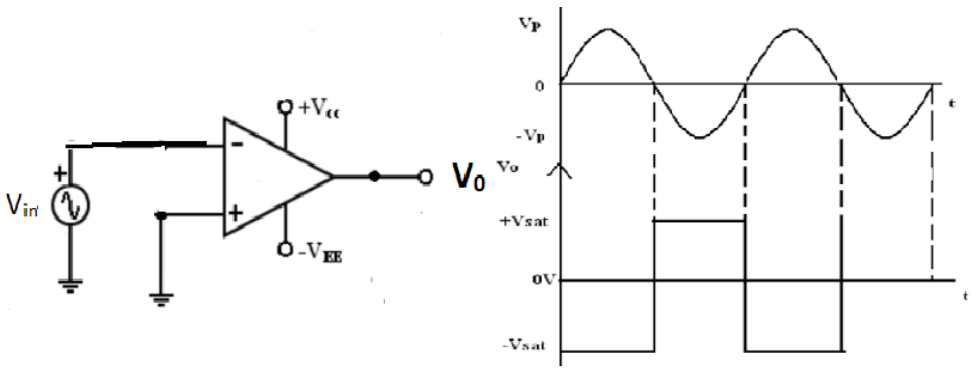
- Zero crossing detector is a comparator with zero reference voltage.
- A **zero crossing detector** is the simplest circuit configurations of **opamp** switching circuits. In this configuration, the input signal is applied to one of the input terminals while the other input is connected to ground. This circuit needs no feedback connection.

NON INVERTING ZERO CROSSING DETECTOR



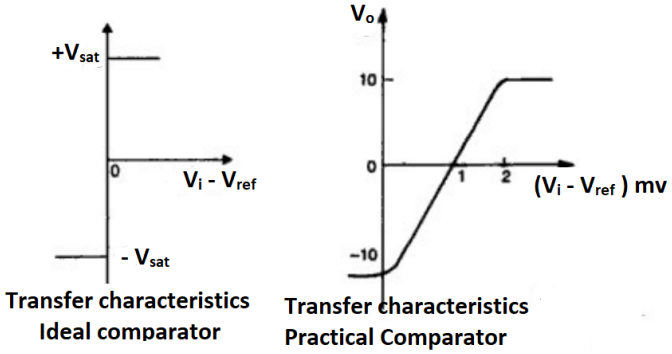
- During the positive half cycle of the sinewave V_{in} is positive . Since positive voltage is connected to + terminal the output is $+$ Vsat
- During the negative half cycle of the sine wave V_{in} negative . Since negative voltage is connected to + terminal the output is $-V_{sat}$

INVERTING ZERO CROSSING DETECTOR



- Here the Non Inverting (+terminal) is grounded ie $V_{ref} = 0$. Sine wave input is given to the Inverting (–terminal)
- For positive V_{in} , output is $-V_{sat}$ and for negative V_{in} ,the output is $+ V_{sat}$

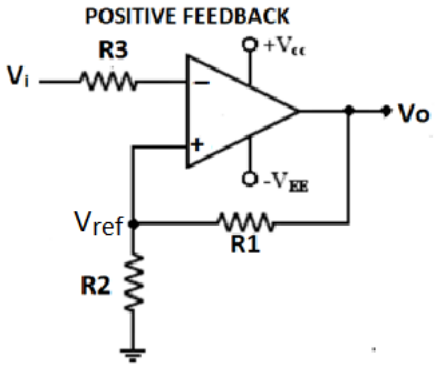
DRAW BACKS OF ZERO CROSSING DETECTOR



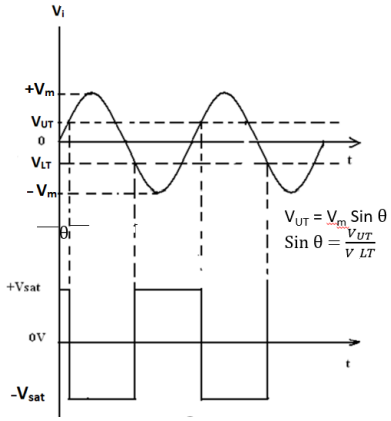
- In some applications, the input **Vi** may be a slowly changing waveform, (i.e) a low frequency signal.
- It will take **Vi** more time to cross **0 V**, therefore **Vo** may not switch quickly from one saturation voltage to the other. Because of the noise at the op-amp's input terminals the output **Vo** may fluctuate between 2 saturations voltages **+Vsat** and **–Vsat.**
- Both of these problems can be cured with the use of regenerative or **positive feedback** that cause the output **Vo** to change faster and eliminate any false output transitions due to noise signals at the input.
- Inverting comparator with positive feedback is known as **Schmitt Trigger**

SCHMITT TRIGGER

Q 28. With a neat circuit diagram explain the operation of Schmitt trigger using Op-Amp



- The inverting configuration produces opposite polarity output. The same polarity is fed ack to the +terminal
- When $\mathbf{V_{in}}$ is slightly positive than $\mathbf{V_{ref}}$, the output will go to $\mathbf{-V_{sat}}$
- When $\mathbf{V_{in}}$ becomes more negative than $-\mathbf{V_{ref}}$ the output will go to $\mathbf{+V_{sat}}$
- Therefore the output voltage is always either $-\text{Vref}$ or $+\text{Vref}$
- $+\text{Vref} = V_{UT} = \frac{V_0}{R_1+R_2} R_2 = \frac{+V_{sat}}{R_1+R_2} R_2$ where V_{UT} is called the Upper Threshold Voltage
- $-\text{Vref} = V_{LT} = \frac{V_0}{R_1+R_2} R_2 = \frac{-V_{sat}}{R_1+R_2} R_2$ where V_{LT} s called the Lower Threshold
- V_{UT} and V_{LT} can be adjusted by varying $R_1 and \ R_2$
- The difference between V_{UT} and V_{LT} is called the Hysterisis
- Hysterisis $= \frac{+V_{sat}}{R_1+R_2} R_2 - \frac{-V_{sat}}{R_1+R_2} R_2 = \frac{2\,V_{sat}\,R_2}{R_1+R_2}$



Q 29. Mention applications of Schmitt trigger

- 1. Overcoming the comparator chatter
- 2. As a square wave generator
- 3. On /Off controllers

Q 30. Design an inverting Schmitt trigger to have trigger voltages of $\mp$ 4 V . Use Op-Amp with supply of $\mp$ 15 V

- $\text{V}_{\text{UT}} = +4\ \text{V}$ and $V_{LT} = -4\ \text{V}$

- $\mp V_{sat} = 0.9 \times 15 = 13.5\ V$
- For Op-Amp 741 from manufacturers table $bias\ current = I_{B(\max)} = 500$ nA
- Let the current through R_1 and R_2 is I_2
- I_2 should be at least 100 times of bias current $=100$ x 500 nA $= 50$ μA
- $R_2 = \frac{V_{UT}}{I_2} = \frac{4}{(50)(10^{-6})} = 80\ K\Omega$
- Use standard 82 KΩ. For this the $I_2 = \frac{4}{(82)(10^3)} = 48.78$ μA

$$R_1 = \frac{+V_{sat} - V_{UT}}{I2} = \frac{+13.5 - 4}{(48.78)(10^{-6})} = 195\ K\Omega$$

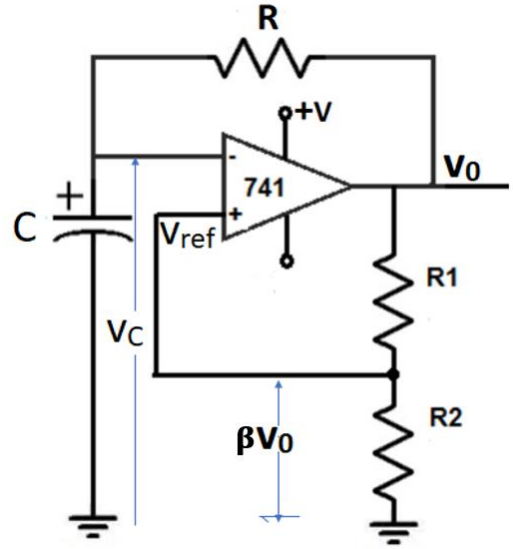
Q 31. Compare Schmitt trigger and Comparator

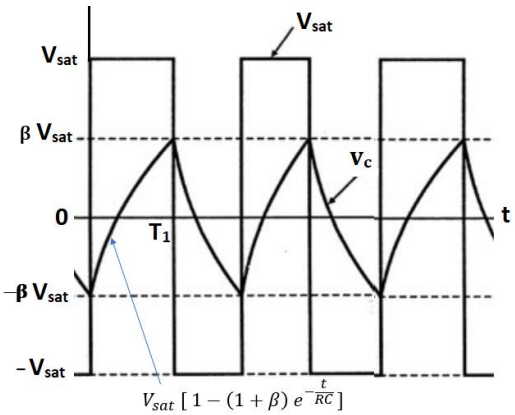
Sl.No.	SCHMITT TRIGGER	COMPARATOR
1	Feedback is used	No feedback
2	False triggering due to noise is avoided	False triggering due to noise can not be avoided
3	Two threshold voltages exist V_{UT} and V_{LT}	Single reference voltage
4	Hysterisis exists	Hysterisis does not exist
5	Output voltage is either +Vsat or -Vsat	Output voltage is either +Vsat or –Vsat
6	Inverting and Non inverting Schmitt configurations exist	Inverting and Non inverting Comparators modes possible
7	Used in squar wave generators, on-off controllers, convert waveforms to square waveforms	Used I zero crossing detectors, window detectors

ASTABLE MUTIVIBRATOR

Q 31. Draw and explain the Astable multivibrator using Op-Amp and state its application

- This is also called free running oscillator. This consists of a Schmitt trigger and R & C circuit connected in negative feedback
- **PRINCIPLE OF OPERATION:**
- The op-amp operates in saturation mode in both states of astable operation
- $V_{ref} = +\beta v_o$ or $-\beta v_o$
- Low pass combination of RC circuit is used in feedback
- Whenever input at –ve terminal just crosses V_{ref} (upwards or downwards) switching takes place
- This results in quasi stable states





- The following steps takes place during the self oscillations
- 1. Let the output V_0 is just switched from $-V_{sat}$ to $+V_{sat}$
- 2. Voltage at + ve terminal switches to $+\beta V_{sat}$ (from $-\beta V_{sat}$)
- 3. Voltage at −ve terminal (junction of capacitor C and resistor R) start charging C to $+\beta V_{sat}$ from $-\beta V_{sat}$ because V_0 is now is $+V_{sat}$
- 4. The voltage charging curve follows the equation

$$v_C = v_f + (v_i - v_f)\, e^{-\frac{t}{RC}}$$

where v_C =capacitor charging voltage

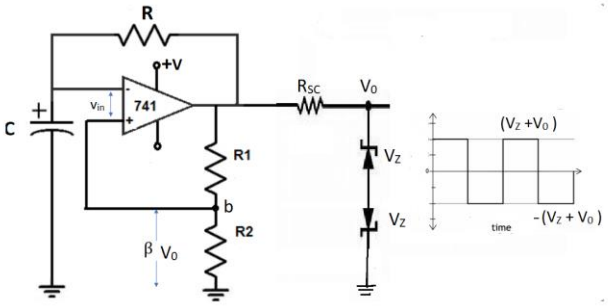
$v_f = +V_{sat}$

$v_i = -\beta V_{sat}$

- 5. While C is charging towards $+V_{sat}$ it reaches the value $+\beta V_{sat}$ and suppose to go upto $+V_{sat}$ goes beyond this value.
- 6. But once it crosses $+\beta V_{sat}$ the voltage at −ve terminal becomes more positive than at +ve terminal $(+\beta V_{sat})$. Since the gain of Op-amp nears infinity the output of op-amp V_0 goes to $-V_{sat}$
- 7. The v_{ref} now goes to $-\beta V_{sat}$. The capacitor C starts charging towards $-V_{sat}$

- 8. The cycle repeats as shown in the diagram and the multivibrator becomes as Astable multivibrator

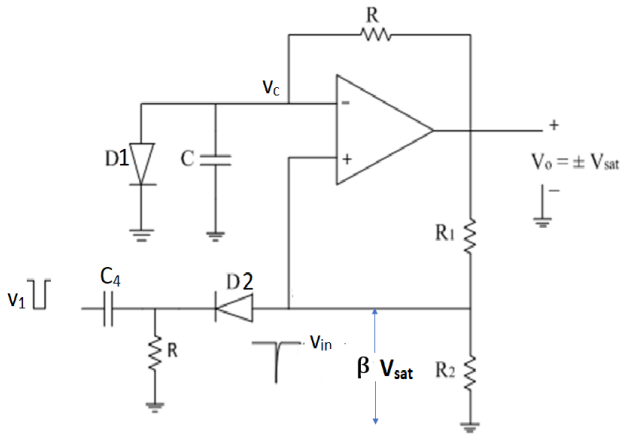
FREQUENCY OF MULTIVIBRATOR:

- $v_C = v_f + (v_i - v_f)\, e^{-\frac{t}{RC}}$
- $V_c = V_{sat} + (-\beta\, V_{sat} - V_{sat})\, e^{-t/RC}$
- $V_c = V_{sat} - V_{sat}\,(1+\beta)\, e^{-t/RC}$
- At $t = T_1$ voltage across capacitor reaches $+\beta\, V_{sat}$ and switching takes place
- $V_C\,(T1) = \beta\, V_{sat} = V_{sat} - V_{sat}\,(1+\beta)\, e^{-T1/RC}$
- $\beta = 1 - (1+\beta)\, e^{-T1/RC}$
- $(1+\beta)\, e^{-T1/RC} = (1-\beta)$
- $e^{-T1/RC} = \frac{1-\beta}{1+\beta}$ and $e^{T1/RC} = \ln \frac{1+\beta}{1-\beta}$
- taking natural logarithms both sides $T1 = RC \ln \frac{1+\beta}{1-\beta}$
- $T1$ is only half the period
- Total time period $T = 2T1 = 2\ RC\ \ln \frac{1+\beta}{1-\beta}$
- The peak to peak output amplitude can be limited to any value by choosing proper Zener diodes V_0 peak to peak $= 2\,(V_Z + V_D)$
- R_{SC} limits the current drawn from Op-amp $i_{sc} = \frac{V_{sat} - V_Z}{R_{SC}}$
- 

MONOSTABLE MULTI VIBRATOR

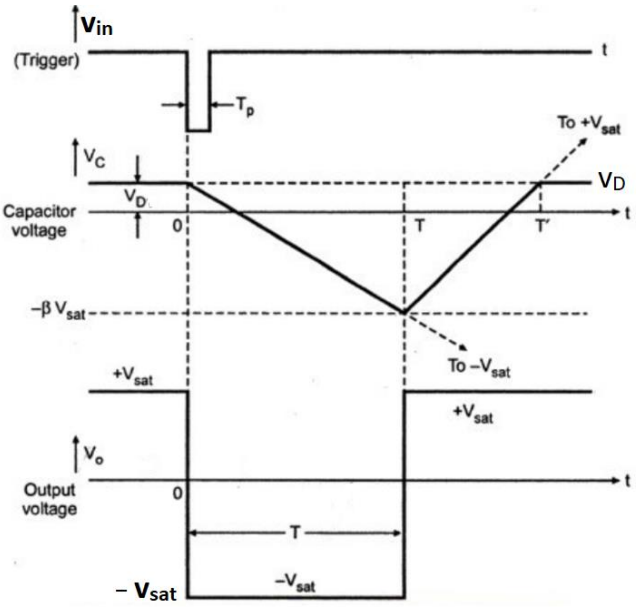
Q 32. Draw and explain the Monostable multivibrator using Op-Amp and state the application

- Monostable multivibrator has one stable state and the other is quasi stable state. Quasi means temporary.
- The width of output pulse in quasi state depends on components R and C shown in the diagram
- The circuit is same as that for Astable Multivibrator except that across the Capacitor C a diode $D1$ is connected and the circuit requires a trigger to drive it into quasi stable state which is temporary.
- The diode across the capacitor clamps the capacitor voltage to $0.7\ V$ when the output is at $+V_{sat}$



Functioning of Circuit:

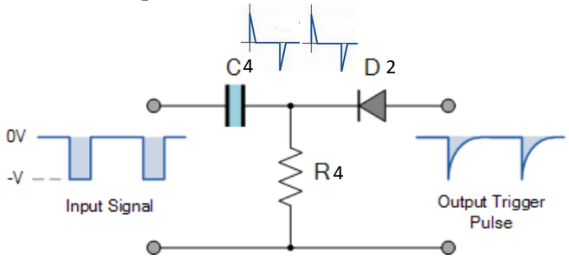
- **Stable State:**
- 1. The circuit is in stable state. Output V_0 is at $+V_{sat}$
- 2. Current flows into Capacitor C through Resistor R and it charges. C might have charged to $+V_{sat}$(if diode 1 is not across C). But due Diode $D1$ voltage of C gets clamped to $+0.7$ volts
- 3. Voltage at + terminal of op-amp is $+\beta V_{sat}$. This is more than $+0.7V$ at $-$input terminal. The output V_0 saturates and its value is $+V_{sat}$ This is the stable state for the circuit.
- 4. Value of $\beta = \frac{R_2}{R_1+R_2}$



Quasi Stable State:

- C_4 and R_4 forms as a differentiating circuit.
- At the edges of input, positive and negative spikes are observed. Diode D_2 removes the positive spikes
- A negative trigger of magnitude V_1 is applied to the + input terminal.
- The magnitude of trigger should make the voltage at + input terminal less than $+0.7$ V ie $[\beta V_{sat} + (-V_1)] < 0.7$

- The voltage at −input terminal is more positive than the + input terminal. So the output V_0 switches to $-V_{sat}$
- The diode is reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through resistor R because V_o is now $-V_{sat}$



- Since V_0 has changed from $+V_{sat}$ to $-V_{sat}$ the voltage at + input terminal is now $-\beta V_{sat}$
- Capacitor C while charging towards $-V_{sat}$ it has to pass the stage where the voltage reaches $-\beta V_{sat}$. Once V_c becomes slightly more negative than $-\beta V_{sat}$ the output of op-amp switches to $+V_{sat}$.
- The capacitor now starts charging to $+V_{sat}$ through R until V_c is 0.7 volts since the capacitor C gets clamped to this voltage by the diode D_1
- So this is the earlier stage which is the stable state

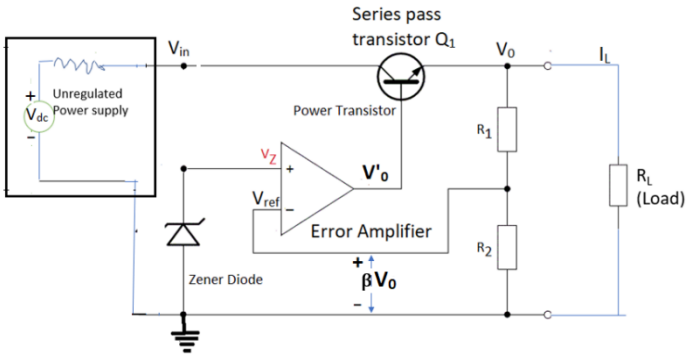
PULSE WIDTH OF MONOSTABLE:

- From theory the voltage across the charging capacitor C is given by
- $V_C = V_f - (V_i - V_f)\, e^{-\frac{t}{RC}}$
- But $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage)
- $V_C = -V_{sat} + (V_D + V_{sat})\, e^{-\frac{t}{RC}}$
- At $t = T$, $V_c = -\beta V_{sat} = -V_{sat} + (V_D + V_{sat})\, e^{-\frac{T}{RC}} =$
- $-\beta V_{sat} = -V_{sat} + V_{sat}\,(1+V_D/V_{sat})\, e^{-\frac{T}{RC}}$
- $1-\beta = (1+V_D/V_{sat})\, e^{-\frac{T}{RC}}$ So $e^{-\frac{T}{RC}} = \frac{1-\beta}{1+\frac{V_D}{V_{sat}}}$
- $e^{\frac{T}{RC}} = \frac{(1+\frac{V_D}{V_{sat}})}{1-\beta}$
- Taking natural logarithms $\frac{T}{RC} = \ln \frac{(1+\frac{V_D}{V_{sat}})}{1-\beta}$
- $T = RC \ln \frac{(1+\frac{V_D}{V_{sat}})}{1-\beta}$ if $R_1 = R_2$ then $\beta = 0.5$ and $V_{sat} \gg V_D$
- $T = RC \ln \frac{1}{1-0.5} = 0.69\, RC$

VOLTAGE REGULATOR

Q 33. What is voltage regulator? Define Line and Load regulation.

- A voltage Regulator is a power supply which removes the ripple contents on the output voltage and makes the output smooth. Secondly it regulates the output voltage such that it remains constant irrespective of load changes or line fluctuations voltage



LOAD REGULATION:

- Load regulation is the change in the regulated output voltage when the load current is changed from minimum (no load) to maximum (full load) , expressed as a fraction of full load voltage

$$\%\ Load\ Regulation\ = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

LINE REGULATION:

- Line regulation is the change in regulated output voltage when the input line voltage is changed . The line regulation is also called Source regulation (SR)
- $\%\ line\ Regulation\ = \frac{SR}{V_{nom}} \times 100$
- where SR = V_H (High line voltage) $-$ V_H (Low line voltage)
- and V_{nom} = Nominal load voltage

Q 34. Draw and explain the internal diagram of IC 723

FUNCTION OF A VOLTAGE REGULATOR:

- The function of a voltage regulator is to provide a stable DC voltage independent of load current for powering electronic circuits.
- The circuit consists of 4 (four) parts
- 1. Reference voltage circuit 2. Error amplifier
- 3. Series pass transistor 4. Feedback network
- There are two types of voltage regulators
- 1. Series regulator 2. switching type regulator
-

OPERATION OF VOLTAGE REGULATOR

- The power transistor Q1 is in series with the Unregulated DC voltage Vin and the regulated output voltage.
- Q1 absorbs the difference between V0 and Vi whenever V0 varies due to load current fluctuations

- Q_1 is connected in Emitter follower configuration and base current is provided by the Op-Amp. So sufficient current gain is available for driving the load current.
- The output voltage is sampled by the R_1 and R_2 divider. The feedback is provided to – ve input terminal.
- The sampled output voltage is compared with a fixed reference voltage provided by the Zener diode
- The Output of Op-Amp V'_0 drives the Series Transistor Q_1
- The Op-Amp in this configuration acts as an Error amplifier
- In case the output voltage V_0 increases due to variations in load current the sampled voltage βV_0 also increases. $\beta = \frac{R_2}{R_1 + R_2}$
- Output V'_0 reduces because of 180^0 phase shift of the –ve terminal input
- Reduction in base voltage of transistor reduces the emitter voltage ie V_0
- Thus the increase in V_0 due to load variation is nullified and output voltage is regulated

Q 35. State the various advantages of IC voltage regulators

- The ic voltage regulator is conveniently used for local regulation.
- The ic voltage regulator is easy to use.
- It is most efficient and reliable.
- The ic voltage regulator is versatile.
- It is very cheap due to mass production and easily available.
- It is compact in size, rugged and light in weight.
- The power supply design becomes easy and quick.
- It is easily manufactured with features like built in protection, programmable output, current or voltage boosting, internal protections such as thermal shutdown, floating operation to facilitate higher output voltage etc.
- It has fast transient response.

2 UNIT CONCLUDED

LINEAR INTEGRATED CIRCUIT APPLICATION
(ECE 404 PC)
UNIT -3

ACTIVE FILTERS & OSCILLATORS:

- Introduction , Ist order LPF, HPF filters, Bandpass , Band reject and all pass filters, Oscillator types and principle of operation – RC, Wein, and quadrature type, Wave form generators , triangular, sawtooth, square wave and VCO

Text books :

- 1. Linear integrated circuit by D.Roy chowdhary New Age International(P) Ltd
  2. Op Amps & linear ICs Ramakanth, A,Gayakwad , PHI

ACTIVE FILTERS INTRODUCTION

Q 1. What is a Filter and what are the broad categories

- Filters are circuits that are capable of passing signals with in a band of frequencies while blocking signals of frequencies outside this band. This is called frequency selectivity.
- Filters are mainly used in Communication and Signal processing circuits. They are also employed in a wide range of applications such as entertainment , medical electronics etc.

BROAD CATEGORIES OF FILTERS:

- An Analog filter processes continuous time signal
- A Digital filter processes discrete time signals
- The analog or digital filters can be subdivided into
  (a)Low pass filters
  (b) High pass filters
  (c) Band pass filter
  (d) Band stop filters
  (e) All pass filters

Q 2. Distinguish between active and passive filters

- Analog filters can be subdivided into
- **PASSIVE FILTERS** : The circuits built using RC ,RL or RLC components
- **ACTIVE FILTERS :** The circuits which uses one or more OP-AMPS, transistors in the design in addition to resistors and capacitors

PASSIVE FILTERS:

Uses passive components – resistors, capacitors and inductors

ii) no amplifying elements like transistors, op-amps etc.
iii) no signal gain
iv) Ist order design is simple
v) 2nd order design uses complex equations
vi) require no power supplies
vii) buffer amplifiers may be required
viii) for accuracy high quality inductors are required

PROBLEMS WITH INDUCTORS REQUIRED IN PASSIVE FILTERS:

i) for large inductance values the physical size becomes very large

ii) tuning inductors to the required values is time consuming and expensive for large quantities of filters
iii) difficult to implement at frequencies below 1 KHz. Because large values of inductances are required
v) lossy
vi) often prohibitively costly

Q 3. What are the advantages of active filters over the passive filters?

ADVANTAGES OF ACTIVE FILTERS.

i) No inductors
ii) op-amps , resistors and capacitors used
iii) provides required gain
iv) easier to design
v) high input impedance prevents excessive loading of the driving source
vi) low output impedance prevents the filter from being affected by the load
vii) easy to adjust over a wide frequency range without altering the desired response
viii) reduced size and weight
ix) increased reliability and improved performance
x) in larger quantities its cost is less compared to passive filter

DISADVANTAGES OF ACTIVE FILTERS:

i) Limited bandwidth of active devices limits the operation at higher frequencies. Passive filters can work at higher frequencies also.
ii) Require power supply unlike passive filters
iii) Increased sensitivity to variations in circuit parameters caused by environmental changes compared to passive filters

Q 4. 1. Explain various types of filters along with their frequency responses

OR

4.2. How are filters classified

OR

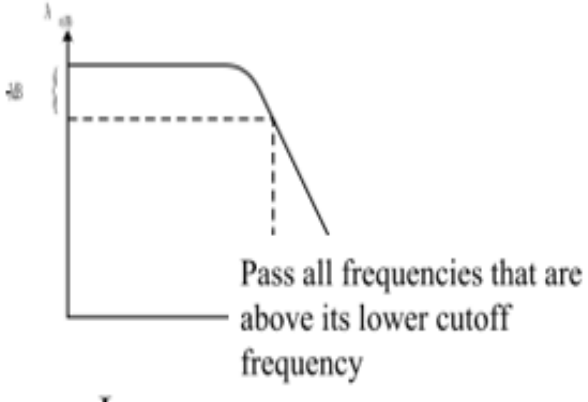
4.3. List the different types of Active filters

OR

4.4. Classify the Active filters and sketch their frequency responses

LOW PASS FILTER:

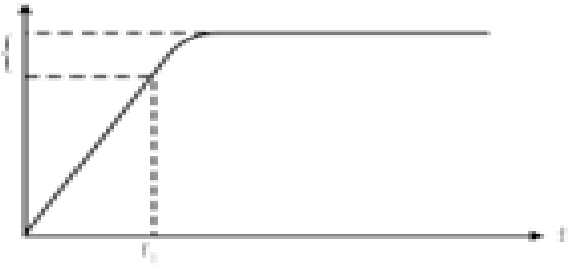
- Pass all frequencies from DC upto the upper cutoff frequency



Low-pass response

HIGH PASS FILTER:

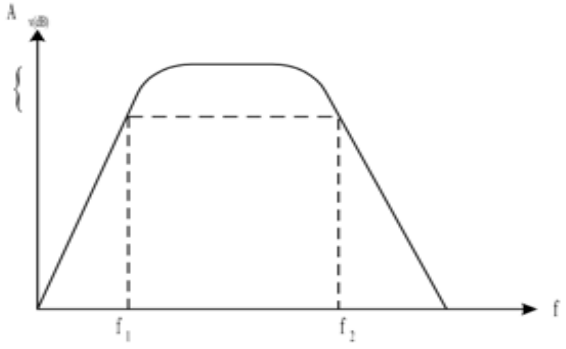
- Pass all frequencies that are above its lower cutoff frequency



High-pass response

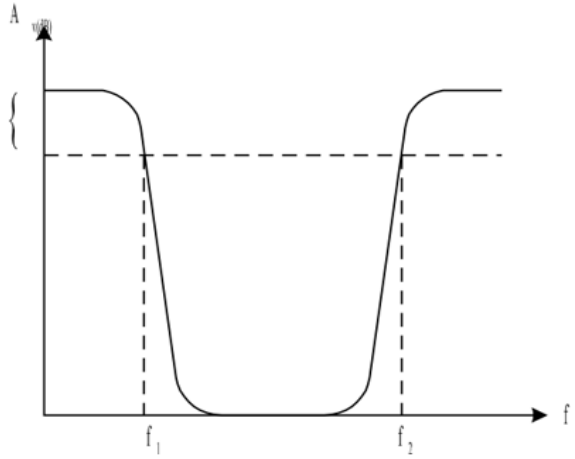
BAND PASS FILTER:

- Pass only the frequencies that fall between its values of the lower and upper cut off frequencies



BAND STOP (NOTCH) FILTERS:

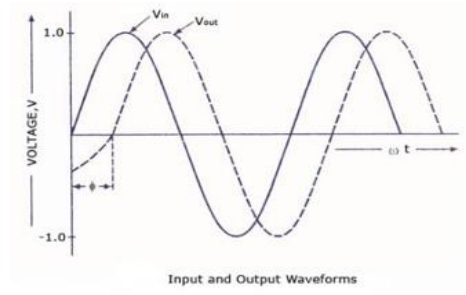
- Eliminate all signals within the stop band while passing all frequencies outside this band



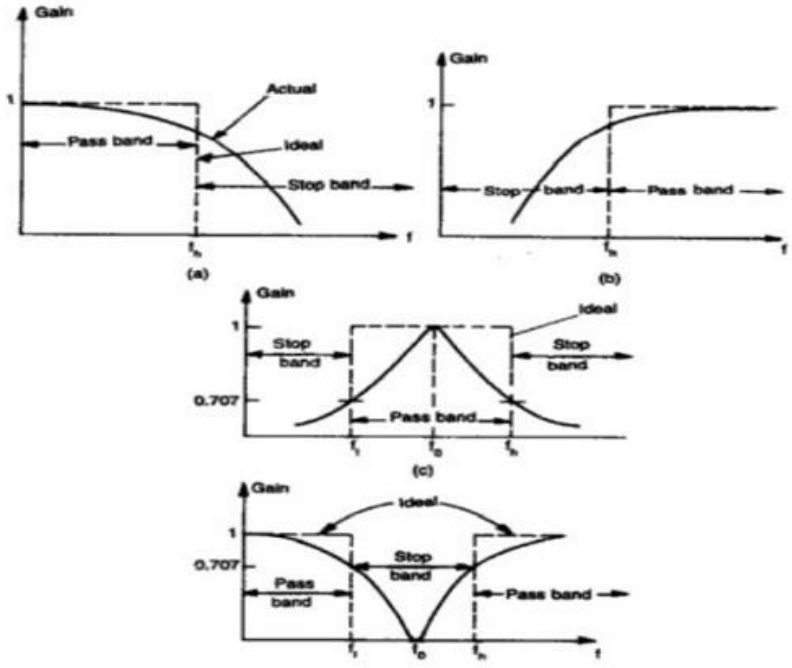
ALL PASS FILTERS :

- An all pass filter is that which passes all frequency components of the input signal without attenuation but provides predictable phase shifts for different frequencies

of the input signals. The all pass filters are also called Delay Equalizers or Phase correctors



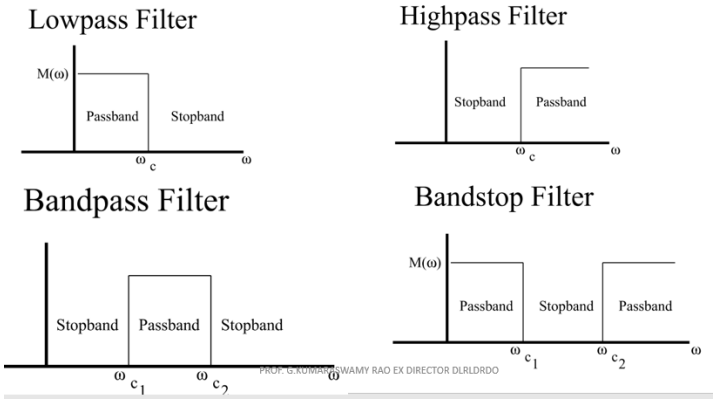
PRACTICAL FILTERS



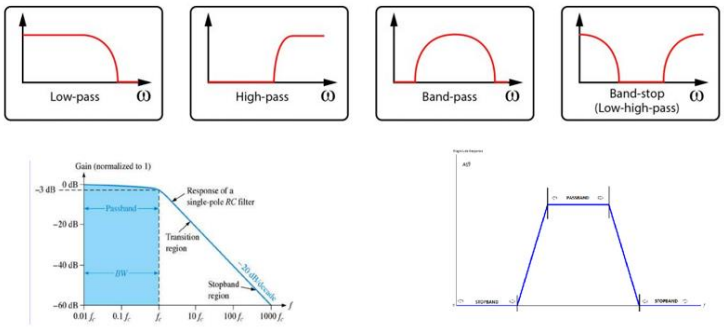
Q 5. What is pass band and stop band for filters?

- **PASSBAND** – Pass-band is the particular range of frequencies which a filter allows to pass through it.
- A passband is the range of frequencies or wavelengths that can pass through a filter. For example, a Radio receiver contains a bandpass filter to select the frequency of the desired radio signal out of all the radio waves picked up by its antenna. The passband of a receiver is the range of frequencies it can receive when it is tuned into the desired frequency (channel)
- STOPBAND – A filter always carries filters within a given band, and rejects the frequencies which are below the given range. This particular range is known as a Stopband.
- **PASS BAND:**
- It is the range of frequencies that are allowed to pass through the filter with minimum attenuation usually defined as less than −3dB (0.707)
- TRANSITION REGION:
  This shows the area where fall-off occurs
- STOP BAND:
- This is the range of frequencies that have the most attenuation

- CUTOFF FREQUENCY:
  This is also called CRITICAL FREQUENCY f_H . This is defined as the end of pass band and normally specified at the point where the response drops −3dB (70.7%) from the pass band response
- **IDEAL FILTER RESPONSES**

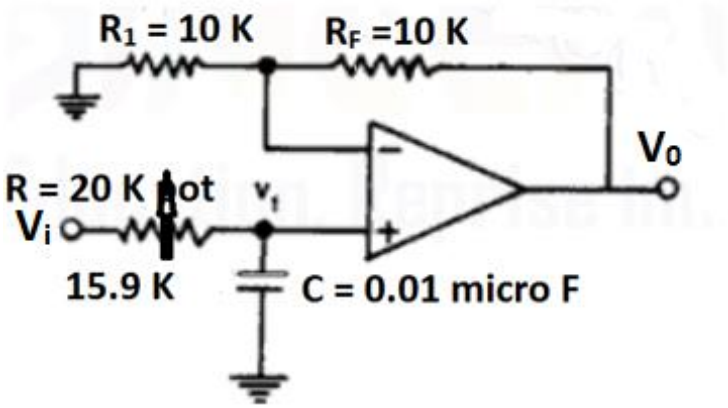


- **PRACTICAL FILTER RESPONSES**



PROBLEM 1. Design a Low pass filter using Op-amp at a cut off frequency of 1 KHz and with a pass gain of 2

- 1. f_H = 1 KHz. 2. Let C = 0.01 µF
  3. Then R = $\frac{1}{2\pi f_H C}$ = $\frac{1}{2\,\pi\, 10^3 \times 0.01 \times 10^{-6}}$ =15.9 KΩ
  Use a 20 K ohms potentiometer and adjust it to get required value
- 4. Pass band gain is $2 = 1+\frac{R_F}{R_1}$. So $R_F = R_1$ the value can be 10KΩ

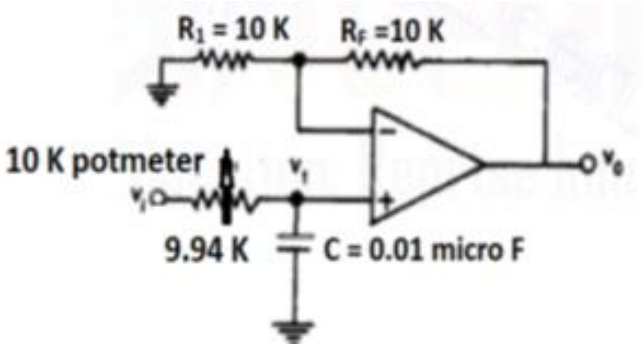


Q 6. What is Frequency scaling?

- **FREQUENCY SCALING:**
- Some-times it is necessary to change the cutoff frequency . The procedure to change cutoff frequency from f_H to f'_H is called Frequency Scaling
- Let M= $\frac{original\ cutoff\ frequency}{new\ cutoff\ frequency}$
- New Value of Resistor = M × original value of resistor
- A pot meter can be used if the value of resistor is nonstandard and required adjustment can be made

PROBLEM 2. Convert the 1 KHz cutoff frequency filter (earlier example) to cutoff frequency of 1.6 KHz

- M = $\frac{original\ cutoff frequency}{new\ cutoff\ frequency} = \frac{1\ KHz}{1.6\ KHz}$= 0.625
- ∴ New resistor R = 15.9 × 0.625 = 9.94 K
- So pot-meter of value 10 K can be used and its value adjusted to 9.94 K



PROBLEM 3. Plot the frequency response of a low pass first order butter-worth filter whose cut-off frequency is 1 KHz and pass band gain is 2

- $|Gain| = \frac{A_F}{\sqrt{1+(\frac{f}{f_H})^2}}$

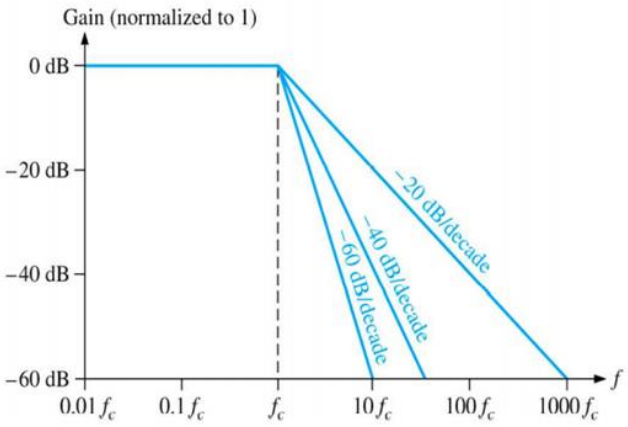
$|Gain| = \frac{2}{\sqrt{1+(\frac{f}{1000})^2}}$

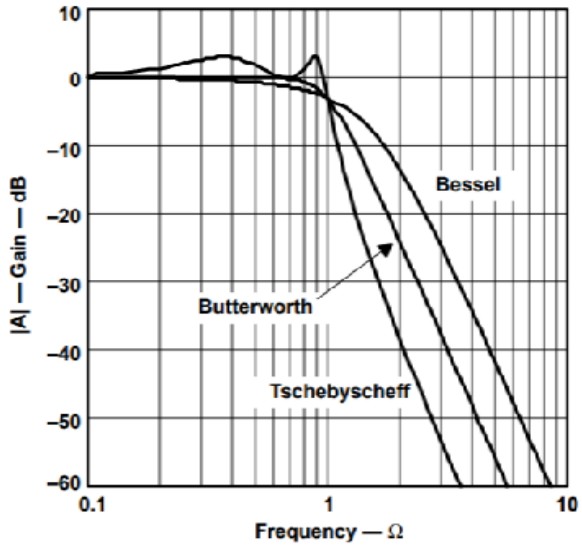
By Substituting different values of f , we can get the value of |Gain| and prepare a table as given below.

Frequency = f	|Gain |	|Gain | in dB
10	2	6.02
100	1.99	5.98
200	1.96	5.85
700	1.64	4.29
1000	1.41	3.01
3000	0.63	-3.98
7000	0.28	-10.97
10000	0.20	-14.02
30000	0.07	-23.53
100000	0.02	-33.98

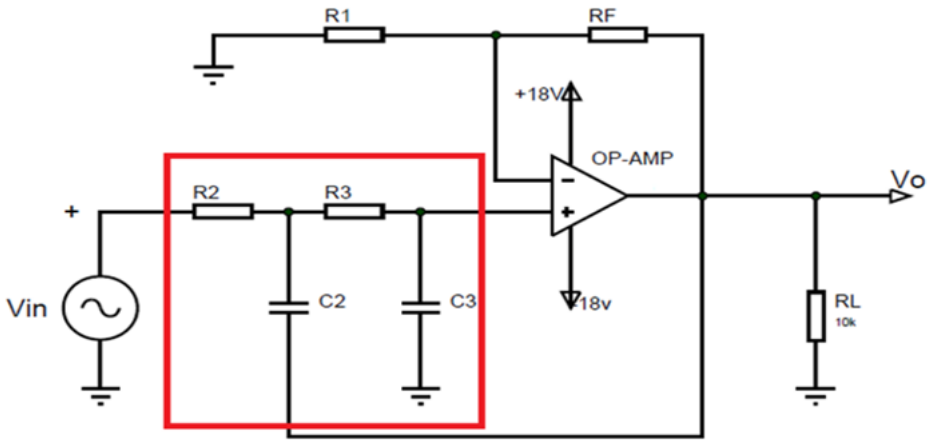
Q 7. Draw the circuit of second order Low pass Butterworth filter and state the expressions for the cut-off frequency and gain of the filter. Sketch the frequency response

- **ORDER OF LOW PASS FILTERS:**
- First order(single pole) has −20 dB/decade roll off
- Second order(two poles) has −40 dB/decade roll off
- Third order(three poles) has −60 dB/decade roll off
-





- **CONFIGURATION OF SECOND ORDER SALLEN KEY FILTER**



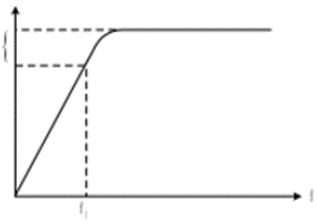
- **STEPS FOR FILTER DESIGN:**
- $f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$ Let us make $R_2 = R_3 = R$ and $C_2 = C_3 = C$
- $f_H = \frac{1}{2\pi\sqrt{R^2C^2}} = \frac{1}{2\pi RC}$
- 1. Set the desired value for f_H
- 2. Choose a value of C < 1µ F
- 3. Calculate R using the equation $R = \frac{1}{2\pi f_H C}$
- 4. Since we are setting $R_2 = R_3 = R$ and $C_2 = C_3 = C$ and we are proposing the same filter response as that of first order filter , a Butterworth filter meets the requirement (Q = 0.707). Because of this the pass band voltage gain A_F should be equal to 1.586 (derivation not included)

  $A_F = (1 + \frac{R_F}{R_1})$ ie $R_F = 0.586\ R_1$

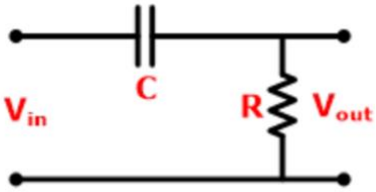
- **PROBLEM 4. Design a second order low pass Butterworth filter with a high cutoff frequency of 1 KHz.**
- **1**. f_H = 1 KHz
- **2.** Let $C_2 = C_3 = .0047\ \mu F = C$
- **3**. Use the equation $R = \frac{1}{2\pi f_H C} = \frac{1}{(2\pi)\quad 10^3 \times 0.047 \times 10^{-6}}$
- ∴ $R_2 = R_3 = 33$ K
- **4**. RF = 0.586 R1 Let $R_1 = 27$K
- $R_F = 0.586 \times 27 = 15.82$ K (use 20 K pot)
- $R_2 = R_3 = 33$ K
- $C_2 = C_3 = 0.047\ \mu F$
- $R_1 = 27$ K and $R_F = 15.8$ K (20 K pot may be used)

Q 8. WHAT IS A HIGH PASS FILTER?

- A high pass filter is an electronic filter that permits signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than that of cutoff frequency.
- The circuit diagram of high pass and low pass filter is the same. Just interchange the capacitor and resistor in a Low pass filter to obtain High pass filter



High-pass response



First Order RC High Pass Filter

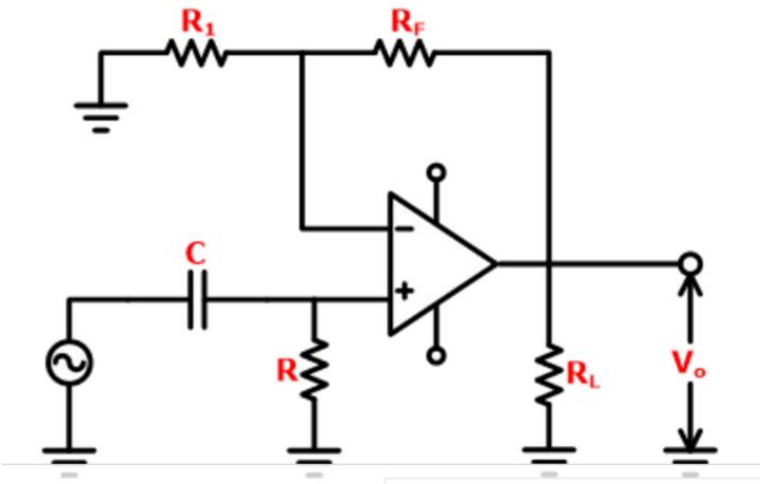
Q 9. Obtain the transfer function of first order High-pass Butterworth filter

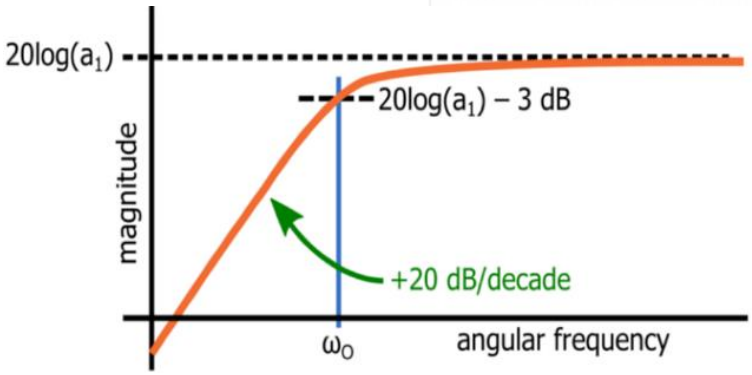
OR

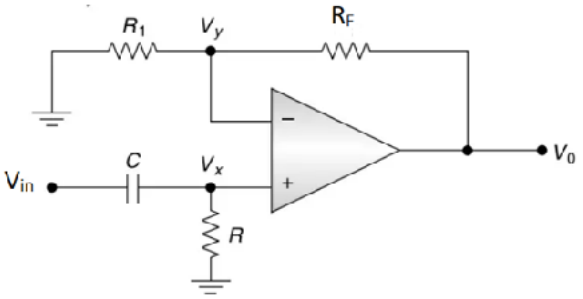
Draw the circuit of High- pass filter and sketch frequency response

Butterworth High Pass Filter:

- The Butterworth filter is designed to have a flat frequency response in the pass band. So, in the pass band, there is no ripple in the frequency response.







- $V_y = \frac{R_1}{R_1+R_F} V_0$
- $V_x = \frac{R}{R+\frac{1}{j\omega C}}$ Vin But $V_y = V_x$
- $\frac{R_1}{R_1+R_F} V_0 = \frac{R}{R+\frac{1}{j\omega C}}$ Vin
- Gain = $\frac{V_0}{V_{in}} = \frac{R}{R+\frac{1}{j\omega C}} \times [\frac{R_1+R_F}{R_1}]$
- Gain = $[1+\frac{R_F}{R_1}]$ $\frac{J\omega C R}{j\omega C R+1} = A_F \frac{J 2\pi f C R}{1+j 2\pi f C R}$
- Where $A_F = [1+\frac{R_F}{R_1}]$ Let Low cutoff frequency = $f_L = \frac{1}{2\pi RC}$
- $\therefore 2\pi RC = \frac{1}{f_L}$
- Gain = $A_F \frac{j\ (\frac{f}{f_L})}{1+\ j\ (\frac{f}{f_L})}$
- |Gain| = $\left| \frac{V_0}{V_{in}} \right| = A_F \frac{(\frac{f}{f_L})}{\sqrt{1+\ (\frac{f}{f_L})^2}}$

PROBLEM 5 Design a High pass filter with a cut-off frequency of 1 KHz and with a pass band gain of 2

- **1**. f_L = 1 KHz.
- **2**. Let C = 0.01 µF (select a commonly available value in the market)
  3. $f_L = \frac{1}{2\pi RC}$
- $\therefore R = \frac{1}{2\pi f_L C} = \frac{1}{(2\pi)(1)(10^3)\times 0.01\times 10^{-6}} = 15.9\ K\ ohms$.
- Use a 20 K ohms potentiometer and adjust it to get required value
- 4. Pass band gain is $2 = 1+\frac{R_F}{R_1}$. So $R_F = R_1$ let the value of $R_F = R_1$ =10K

PROBLEM 6. Plot the frequency response of the filter given in previous example

$$|\text{Gain}| = A_F \frac{(\frac{f}{f_L})}{\sqrt{1+(\frac{f}{f_L})^2}} \quad \text{here } A_F = 2 \text{ and } f_L = 1 \text{ KHz}$$

- Substitute various values in f and calculate |Gain|
- Example: Take f =100 Hz

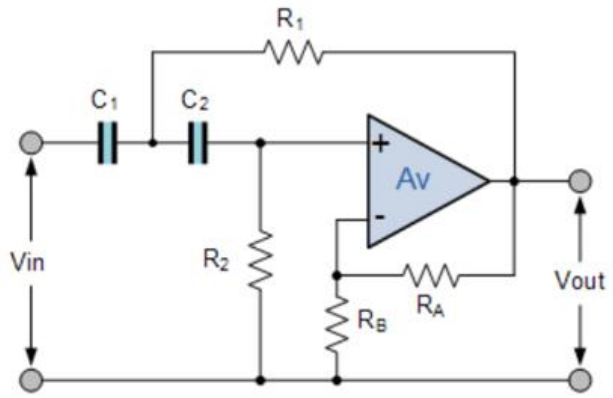
$$|\text{Gain}| = 2 \frac{(\frac{100}{1000})}{\sqrt{1+(\frac{100}{1000})^2}} = 0.20 \text{ and } 20\log(0.2) = -14.02 \text{ dB}$$

-

Frequency = f	|Gain |	|Gain | in dB
100	0.20	-14.02
200	0.39	-8.13
400	0.74	-2.58
700	1.15	1.19
1000	1.41	3.01
3000	1.90	5.56
7000	1.98	5.93
10000	1.99	5.98
30000	2	6.02
100000	2	6.02

Q 10. Draw the circuit of second order High-pass Butterworth filter and state the expression for the cutoff frequency and gain of the filter. Sketch the frequency response

- The second order High pass filter is formed by interchanging R and C components in second order low pass filter



Gain (Av) = $1 + \frac{R_A}{R_B}$

If Resistor and Capacitor values are different:

$f_C = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$

If Resistor and Capacitor values are the same:

$f_C = \frac{1}{2\pi RC}$

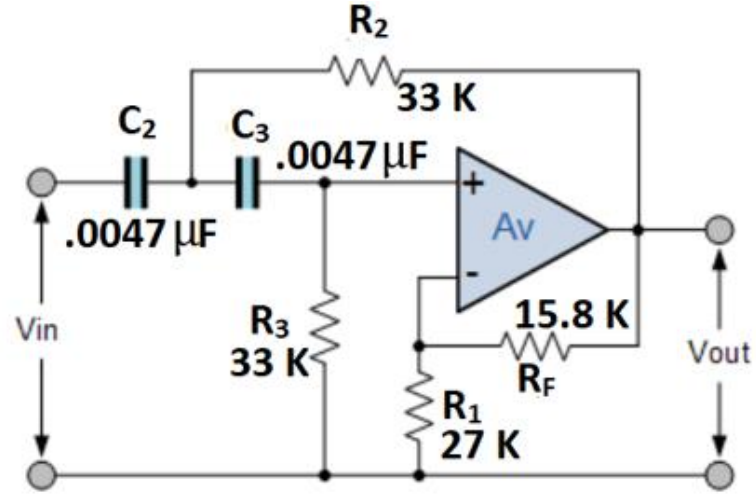
- The voltage gain magnitude of the high pass second order is given as

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(\frac{f_L}{f})^4}}$$

- Where pass band gain A_F = 1.586 (since we have chosen Butterworth filter)
- f = input signal frequency
- f_L = low cut off frequency
- Second order low pass and high pass are same circuits except that the positions of resistors and capacitors are interchanged and the design of filter is same

PROBLEM 7. Determine the low cutoff frequency of the filter shown in diagram

$$f_L = \frac{1}{2\pi\sqrt{(33\times1000)^2(.0047\times10^{-6})^2}} = 1 \text{ KHz}$$



PROBLEM 8. Determine the frequency response plot of the filter

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f_L}{f}\right)^4}}$$

where A_F = 1.586 (because the filter is Butterworth)

Substitute different values for frequency 'f' and calculate the

$$|\text{gain}| = \left|\frac{V_0}{V_{in}}\right|$$

- Take f=100 Hz

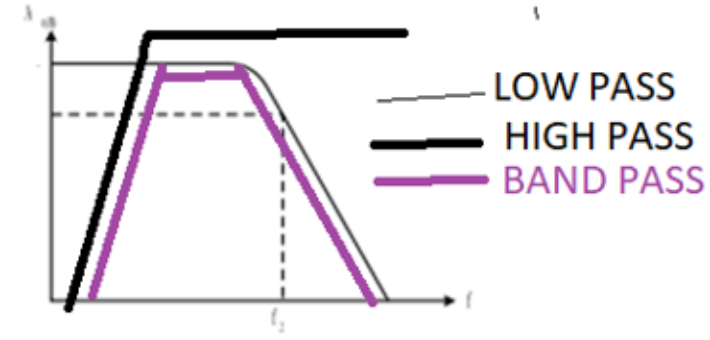
$$\left|\frac{V_0}{V_{in}}\right| = \frac{100}{\sqrt{1+\left(\frac{1000}{100}\right)^4}} = 0.01586 \text{ and } 20\log(.01586) = -35.69 \text{ dB}$$

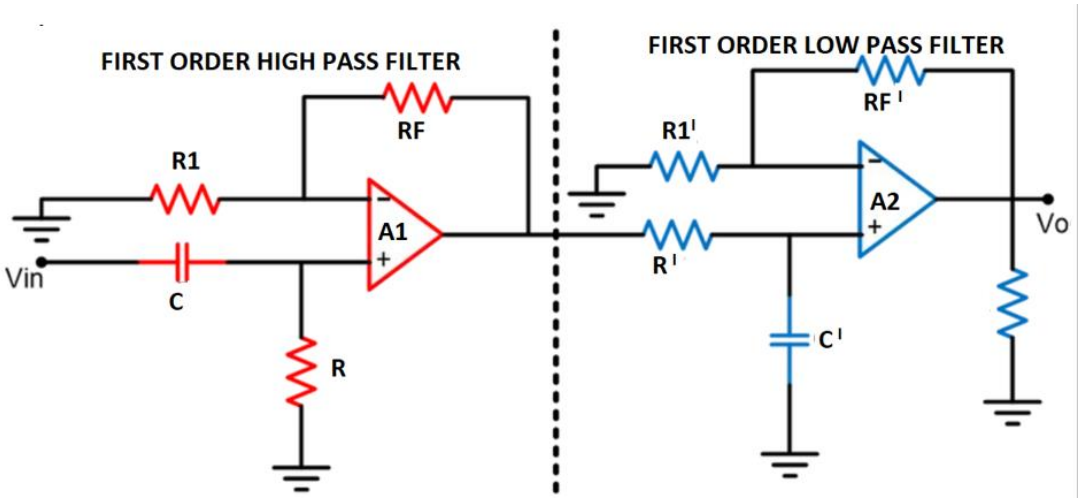
INPUT FREQUENCY =f	GAIN MAGNITUDE (V_0/V_{IN})	MAGNITUDE IN dB
100	0.01586	−35.69
200	0.0634	−23.96
700	0.6979	−3.124
1000	1.1215	0.9960
3000	1.5763	3.953
7000	1.5857	4.004
10000	1.5859	4.006
30000	1.5860	4.006
100000	1..5860	4.006

Q 11. What is Band-pass filter? Which are the two types ? Draw their frequency responses

- A band pass filter (also known as a BPF or pass band filter) is defined as a device that allows frequencies within a specific frequency range and rejects (attenuates) frequencies outside that range.
- Band pass filter can be realized by the cascade connection of high pass and low pass filter
- The Band Pass Filter has two cutoff frequencies. The first cutoff frequency is from a high pass filter. This will decide the lower frequency limit of a band that is known as the low cutoff frequency (fc -low). The second cutoff frequency is from the low pass filter. This will decide the higher frequency limit of the band and that is known as higher cutoff frequency (fc-high).
- The cut-off or corner frequency of the low pass filter (LPF) is higher than the cut-off frequency of the high pass filter (HPF) and the difference between the frequencies at the -3dB point will determine the "bandwidth" of the band pass filter while attenuating any signals outside of these points.
- The higher corner point (f_H) as well as the lower corner frequency cut-off point
- (f_L) are calculated the same way as before in the standard first-order low and high pass filter circuits. Obviously, a reasonable separation is required between the two cut-off points to prevent any interaction between the low pass and high pass stages.

- The cut-off or corner frequency of the low pass filter (LPF) is higher than the cut-off frequency of the high pass filter (HPF) and the difference between the frequencies at the −3dB point will determine the "bandwidth" of the band pass filter while attenuating any signals outside of these points.

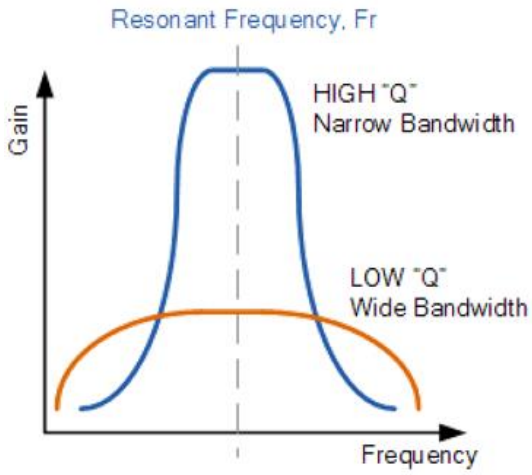




- **TYPES OF BAND PASS FILTER:**
- Basically there are 2 types of band pass filters
- 1. Wide band-pass filter
- 2. Narrow band-pass filter

QUALITY FACTOR OR FIGURE OF MERIT:

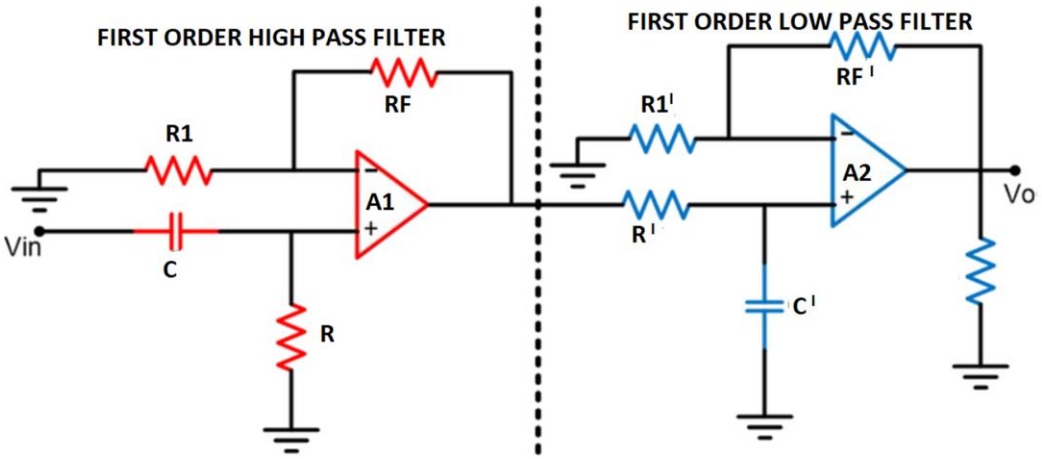
- Quality factor 'Q' is a measure of the selectivity. Higher the value of Q the filter is more selective which means the bandwidth (BW) is narrower
- $Q = \frac{f_C}{BW} = \frac{f_C}{f_H - f_L}$



- Wide band filter $Q < 10$
- Narrow band filter $Q > 10$.
- In this filter the gain peaks at centre frequency f_C

Q12. Explain the operation of Wide Band-pass filter with a neat diagram

- Wide band pass filter is formed by cascading high pass and low pass filters



- To obtain a ± 20 dB /decade band-pass filter first order High pass filter and first order Low pass filter are cascaded
- To obtain a ± 40 dB/decade band-pass filter second order High pass filter and second order Low pass filter are connected in series
- To realize the band-pass f_H (low pass filter cut off) must be greater than f_L (high pass filter cut off)

FREQUENCY RESPONSE OF BAND-PASS FILTER:

- Voltage Gain for High Pass filter:

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_H \ (\frac{f}{f_L})}{\sqrt{1+ \ (\frac{f}{f_L})^2}}$$

- Voltage gain for Low Pass filter:

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_L}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

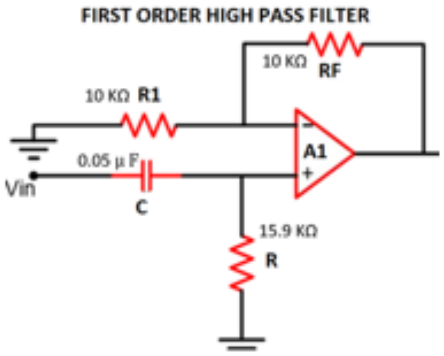
- Voltage gain of Band-Pass filter = product of the above two gains

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_{FT}\ \left(\frac{f}{f_L}\right)}{\sqrt{\left[1+\left(\frac{f}{f_L}\right)^2\right]\left[1+\left(\frac{f}{f_H}\right)^2\right]}}$$ where $A_{FT} = A_H\ A_L$

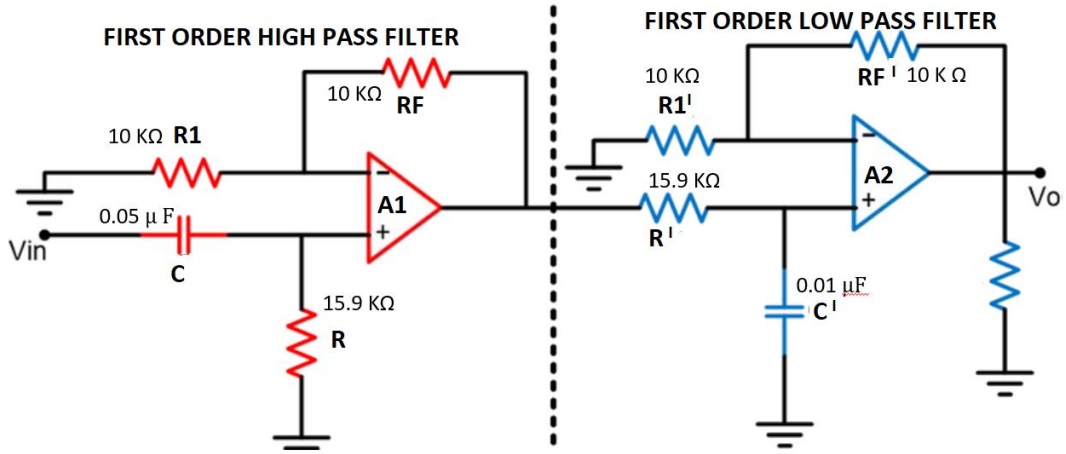
PROBLEM 9. Design a wide band-pass filter with f_L =200 Hz., f_H= 1 KHz. and a passband gain of = 4

- **First design a High pass filter at a cutoff frequency of 200 Hz**
- 1. f_L = 200 Hz.
- 2. Let C = 0.05 µF

  3. Then $R = \frac{1}{2\pi f_L C} = \frac{1}{(2\pi)200\times0.05\times10^{-6}}$ =15.9 KΩ
- Use a 20 K ohms potentiometer and adjust it to get required value .
- Pass band gain = 4 . The gain is distributed between high pass and low pass filters equally ie each =2 ($A_L\ A_H = 4$ and make $A_L = A_H = \sqrt{4}$ =2)
- Pass band gain is 2 = $1+\frac{R_F}{R_1}$. So $R_F = R_1$ let the value be 10K



- **Secondly design the low pass filter**
- **1**. f_H= 1000 Hz. (cut off for Low pass)
- **2**. Let C^1 = 0.01 µf
- **3.** $f_L = \frac{1}{2\pi R^1 C^1}$ $\therefore R^1 = \frac{1}{2\pi f_H C^1}$
- $= \frac{1}{2\pi(1000)(.01)(10^{-6})}$ = 15.9 KΩ
- **4**. Pass band gain = 4 . The gain is distributed between high pass and low pass filters equally ie each =2 ($A_L\ A_H = 4$ and make $A_L = A_H = \sqrt{4}$ =2)
- **5**. $\left(1+\frac{R_F^1}{(R_1)^1}\right) = 2$ $so\ R_F^1 = (R_1)^1 =$ say 10 K



PROBLEM 10. Draw the frequency response plot of the previous filter

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_{FT}\ (\frac{f}{f_L})}{\sqrt{[1+\ \left(\frac{f}{f_L}\right)^2\ ][1+\ (\frac{f}{f_H})^2]}}$$

- A_{FT} = total pass band gain = 4
- f_L = low cutoff frequency = 200 Hz
- f_H = high cutoff frequency = 1 KHz
- f = frequency of input signal
- Substitute various values of 'f ' and tabulate the results as shown in the table .
  Example : Say f=100 Hz

$$\left|\frac{V_0}{V_{in}}\right| = \frac{4\ (\frac{100}{200})}{\sqrt{[1+\ \left(\frac{100}{200}\right)^2\ ][1+\ (\frac{100}{1000})^2]}} = 1.780$$

  - 20 log (1.780) = 5.01 dB

INPUT FREQUENCY f	GAIN MAGNITUDE RATIO	GAIN MAGNITUDE IN DB
10	0.1997	−13.99
30	0.5931	−4.54
100	1.780	5.01
200	2.774	8.861
447.2	3.33	10.46
700	3.151	9.969
1000	2.774	8.861
2000	1.780	5.001
7000	0.5655	−4.95
10000	0.3979	−8.004

PROBLEM 11. Calculate the value of Q for the filter

- $f_C = \sqrt{(f_H)(f_L)} = \sqrt{(1000)(200)}$ = 447.2 Hz

- $Q = \frac{f_C}{BW} = \frac{f_C}{f_H - f_L} = \frac{447.2}{1000 - 200} = 0.56$
- Since Q <10, this is a wide band-pass filter

PROBLEM 12. Design a wide band-pass filter with f_L = 500 Hz and f_H = 2 KHz and pass band gain = 5 for both sections of filter. Also determine the value of Q for the filter

- First Design a High pass filter at a cutoff frequency of 500 Hz

  1. f_L = 500 Hz. 2. Let C = 0.02 µF

  3. Then $R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(500)(0.02\times10^{-6})} = 15.9\ K\Omega$

  Use a 20 K ohms potentiometer and adjust it to get required value
- 4. Pass band gain = A_{FT} = 5 ie $A_H A_L$ =5 So $A_H = A_L = \sqrt{5} = 2.236$. The gain is distributed between high pass and low pass filters equally ie each =2.236 = $(1 + \frac{R_F}{R_1})$ ∴ $\frac{R_F}{R_1}$ = 1.236 Let R_1 = 12 K

  then R_F = 1.236 × 12 = 15 K
- Secondly design the low pass filter
- 1. f_H= 2000 Hz.
- 2. Let C^1 = 0.01 µF
- 3. $f_L = \frac{1}{2\pi R^1 C^1}$ $\therefore R^1 = \frac{1}{2\pi f_H C^1} = \frac{1}{2\pi(2000)(.01)(10^{-6})} = 7.95\ Kohm$
- 4. Pass band gain = A_{FT} = 5 ie $A_H A_L$ =5 So $A_H = A_L = \sqrt{5} = 2.236$. The gain is distributed between high pass and low pass filters equally ie each = 2.236 = $(1 + \frac{R_F}{R_1})$ ∴ $\frac{R_F}{R_1}$ = 1.236 Let R_1 = 12 K
- then R_F = 1.236 × 12 = 15 K
- $f_C = \sqrt{f_L f_H} = \sqrt{500 \times 2000}$ = 1000 Hz
- BW = $f_H - f_L$ = (2000 −500) =1500 Hz
- Q = $\frac{f_C}{f_H - f_L} = \frac{1000}{1500} = 0.067$

PROBLEM 13. Design a wide band-pass filter with f_L = 400 Hz. and f_H = 2 KHz and pass band gain of 4

- First design a High pass filter at a cutoff frequency of 400 Hz
- **1**. f_L = 400 Hz. **2.** Let C = 0.05 µF

  3. Then $R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(400)(0.05\times10^{-6})}$ =7.95 KΩ

  Use a 20 K ohms potentiometer and adjust it to get required value
- 4. Pass band gain = A_{FT} = 5 ie $A_H A_L$ = 4 So $A_H = A_L = \sqrt{4} = 2$. The gain is distributed between high pass and low pass filters equally ie each

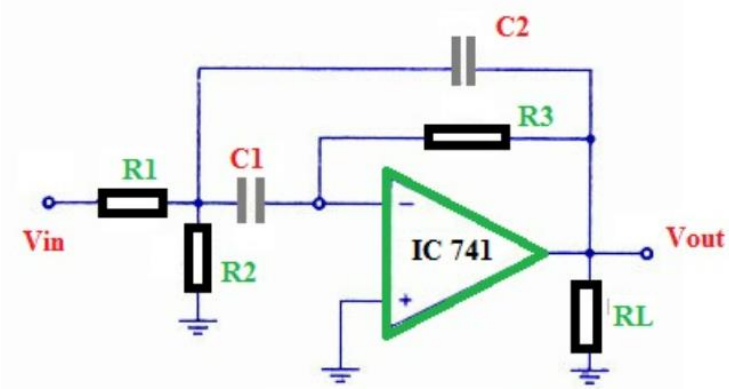
=2 = 1 + $\frac{R_F}{R_1}$ ∴ $\frac{R_F}{R_1}$ = 1 Let R_1 = 10 K then R_F = 10 K Ω

- Secondly design the low pass filter
- **1**. f_H= 2000 Hz.
- **2**. Let C^1 = 0.01 µF
- **3**. $f_L = \frac{1}{2\pi R^1 C^1}$ ∴ $R^1 = \frac{1}{2\pi f_H C^1} = \frac{1}{2\pi (2000)(.01)(10^{-6})}$ =7.95 KΩ
- **4**. Pass band gain = A_{FT} = 4 ie A_1 A2 =4 So $A_H = A_L = \sqrt{4} = 2$. The gain is distributed between high pass and low pass filters equally ie each =2
- 2= (1 + $\frac{R_F}{R_1}$) ∴ $\frac{R_F}{R_1}$ = 1 Let R_1 = 10 K then R_F =10 K

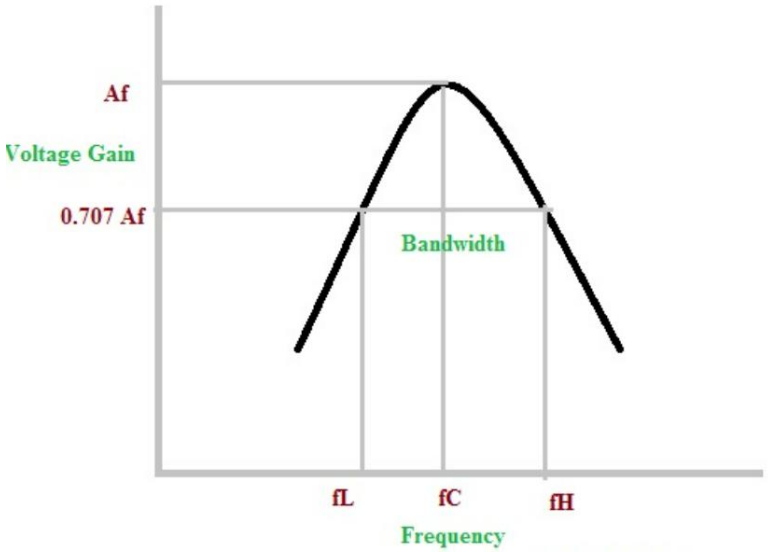
PROBLEM 14. The resonant frequency f_o of a band pass filter is 1 KHz and its band width is 3 KHz, Find the value of Q

- f_O = 1 KHz ; BW = 3 KHz
- Q = $\frac{f_O}{BW} = \frac{1000}{3000} =$ = 0.333

Q 13. Explain the operation of Narrow Band-pass filter with a neat diagram



- This filter uses a multiple feedback filter configuration (unlike earlier Sallen-key configuration) because it uses two feedback paths
- op-amp is utilized in the inverting mode



- **DESIGN EQUATIONS:**
- The Narrow band-pass filter is designed fo specific values of a) Center frequency f_C b) Q or bandwidth
- To simplify design C1 = C2 = C (in this case the following design equations are assumed)
- $R1 = \frac{Q}{2\pi f_C C A_F}$
- $R2 = \frac{Q}{2\pi f_C C (2Q^2 - A_F)}$
- $R3 = \frac{Q}{\pi f_C C}$
- A_F is the gain at f_C and $A_F = \frac{R_3}{2R_1}$
- A_F must satisfy the condition $A_F < 2Q^2$

- **ADVANTAGE OF MULTIPLE FEEDBACK FILTER:**
- The center frequency f_C can be easily changed to a new frequency f'_C without changing the gain or bandwidth. This is done by changing R2 to R'2 by using the following equation
- $R'2 = R2 \left(\frac{f_C}{f'_C}\right)^2$

PROBLEM 15. Design a multiple feedback Narrow band-pass filter with f_C = 1 KHz Q=3 and A_F =10

- Choose the values of C1 and C2 first and then calculate the values of R1, R2, and R3
- Let C1 = C2 = C = 0.01 µF

- R1 = $\frac{Q}{2\,\pi\,f_C\,C\,A_F}$ = $\frac{3}{(2\,\pi)\,(10^3)(0.01\times10^{-6})(10)}$ = 4.77 K Ω
- R2 = $\frac{Q}{2\,\pi\,f_C\,C\,(2\,Q^2\,-A_F\,)}$ = $\frac{3}{(2\pi)(10^3)(0.01\times10^{-6})[2(3^2)-10]}$ = 5.97K Ω
- R3 = $\frac{Q}{\pi\,f_C\,C}$ = $\frac{3}{(\pi)(10^3)(0.01\times10^{-6})}$ = 95.5 K Ω
- Practical values that are used are R1 = 4.7 K Ω, R2 = 6.2 K Ω and R3= 100KΩ

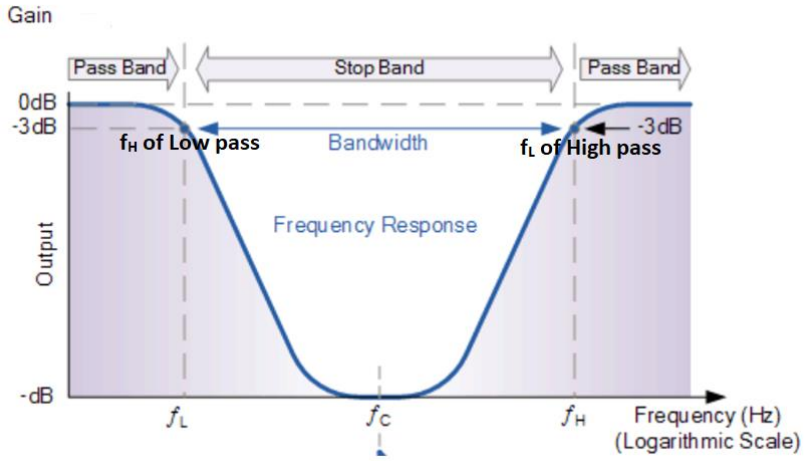
PROBLEM 16. change the center frequency to 1.5 K Ω , keeping the AF and bandwidth constant

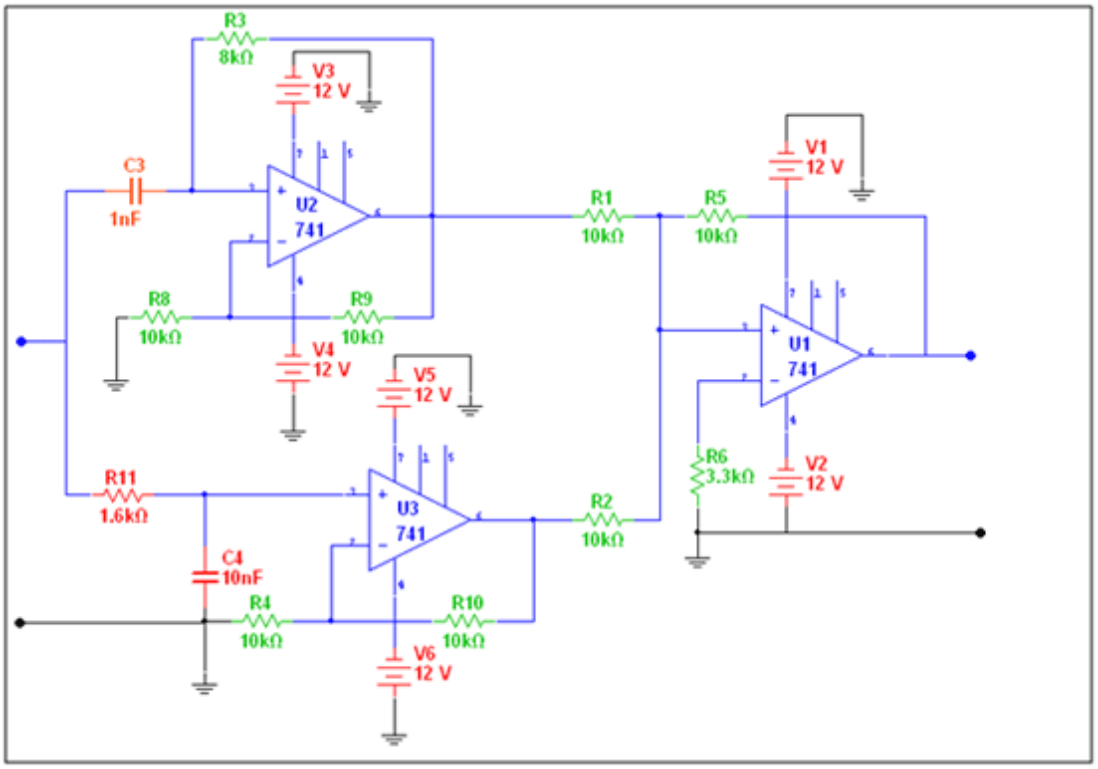
- R'2 = R2 $(\frac{f_C}{f_C})^2$ = $(5.97\times10^3)\,(\frac{1\,(10^3)}{1.5(10^3)})^2$ = 2.65 K Ω
- Practical available value of R'2 = 2.7 K Ω

WIDE BAND-REJECT FILTER

Q 14. Draw and explain the op-amp Wide Band-reject filter

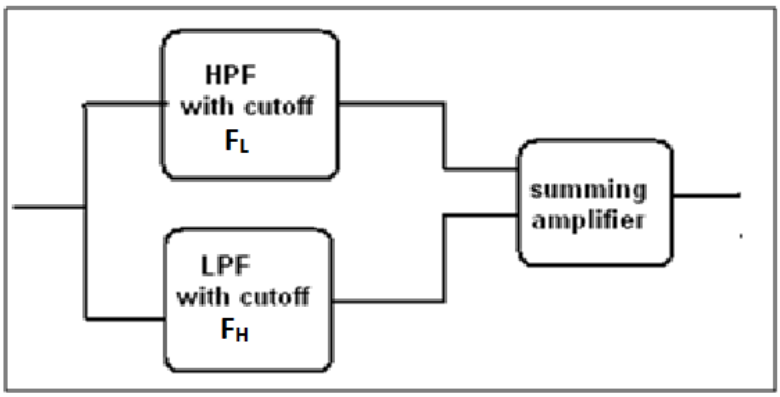
- The function of a band stop filter is to pass all those frequencies from zero (DC) up to its first (lower) cut-off frequency point f_{Low}, and pass all those frequencies above its second (upper) cut-off frequency f_{High}, but block or reject all those frequencies in-between. Then the filters bandwidth, BW is defined as: $(f_{HIGH} - f_{LOW})$.
  So for a wide-band band stop filter, the filters actual stop band lies between its lower and upper −3dB points as it attenuates, or rejects any frequency between these two cut-off frequencies. The frequency response curve of an ideal band stop filter is therefore given as



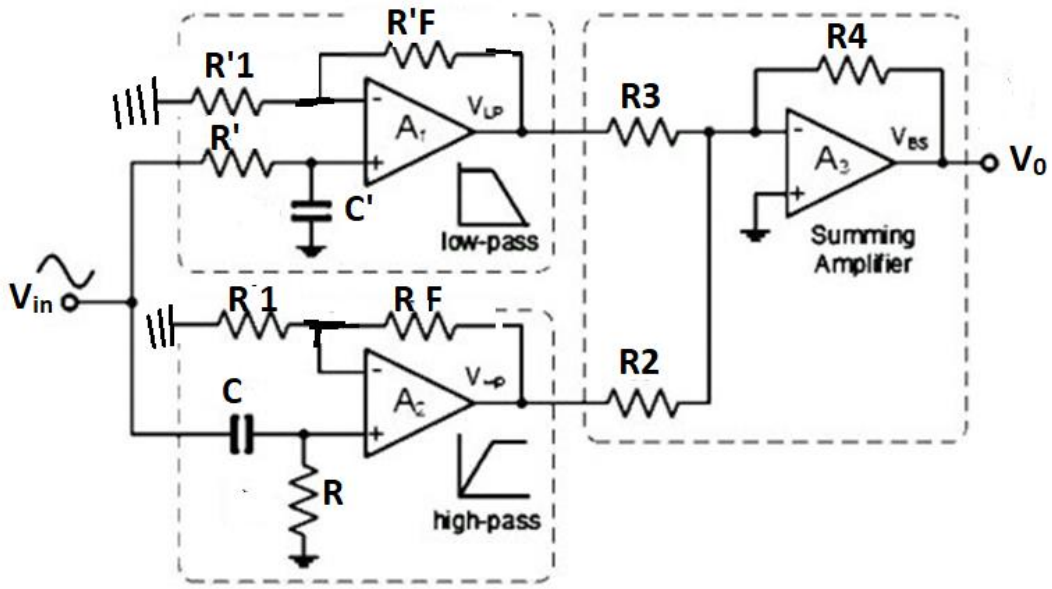


There are 2 cut off frequencies for band reject filter.

- 1. lower cut off frequency (f_{LOW}) – the frequency below which all the frequencies are passed
- 2. upper cut off frequency (f_{HIGH}) – all the frequencies above this frequency are passed
- Similar to band pass filter but the difference is f_H of Low pass is $< f_L$ of High pass
- The band pass reject filter is also called a Band stop or Band elimination filter
- Frequencies are attenuated in the Stop band while they are passed outside this band



- Like in Band-pass filter Band reject can be divided into
- i) Wide band-reject
  ii) Narrow band-reject.
- The Narrow band reject filter is also called Notch filter. Here the Q is large > 10 and the band is much smaller when compared to Wide band reject filter



- This filter uses a Low pass filter and a High pass filter. Their outputs are added in a Summing Amplifier
- In this filter the f_L which is the low frequency cutoff of HIGH PASS FILTER must be higher than the f_H which is the higher frequency of LOW PASS filter
- Also the pass band gain of low pass filter and high pass filter must be same

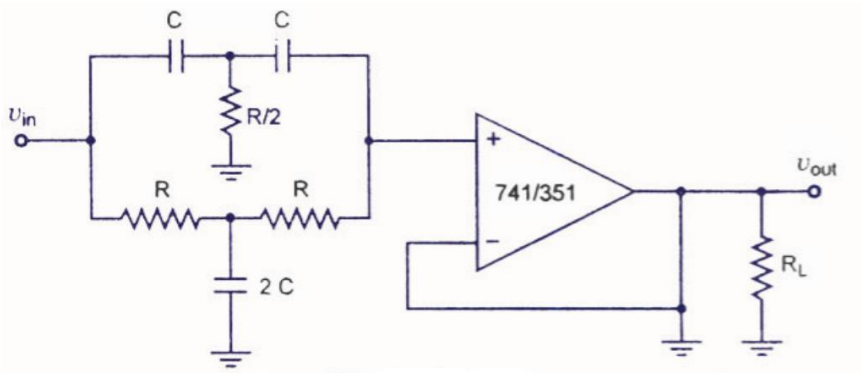
PROBLEM 17. . Design a wide band-reject filter having f_H = 200 Hz and f_L = 1 KHz,

- Though the above frequencies belong to low pass and high pass filters respectively the Wide band reject filter has f_{Low}= 200 Hz and f_{HIgh}1 KHz
- **LOW PASS FILTER WITH F_H =200 HZ**
- Let C' = 0.05 μ F
- Then R' = $\frac{1}{2\ \pi\ (200)(0.05\times10^{-6})}$ = 15.9 KΩ
- **HIGH PASS FILTER WITH f_L = 1KHz**
- Let C= 0.01 μf
- Then R = $\frac{1}{2\ \pi\ (1000)(0.01\times10^{-6})}$ = 15.9 KΩ
- Pass band gain is 2
- Gain = $(1+\frac{RF}{R1}) = (1+\frac{R'F}{R'1})$ = 2
- ∴ R1 = RF = R'F = R'1 =10 K Ω
- **SUMMING AMPLIFIER:**
- Summing amplifier gain can be =1
- ∴ R2= R3 =R4 =10 K Ω

NARROW BAND-REJECT FILTER

Q 15. Draw and explain the op-amp Narrow Band-reject filter ie. Notch filter

- **FUNCTIONAL DETAILS :**
- The narrow band-reject filter is also called the NOTCH filter.
- It is used for rejection of a single frequency for example 50/60 Hz Power line frequency hum (noise). This filter is used for eliminating undesired frequencies in communication and biomedical instruments
- The notch out frequency is the frequency at which maximum attenuation takes place



Twin T active notch filter

- Twin T network is used to obtain maximum attenuation
- Twin T network is formed by joining two T-shaped networks. One T-network consists of two resistors and a capacitor. The other T-network consists of two capacitors and a resistor
- The notch out frequency is given as
- $f_N = \frac{1}{2\pi R C}$

PROBLEM 18.. Design a 60 Hz notch filter. Draw its frequency response

- Let C = 0.068 μ F
- $f_N = \frac{1}{2\pi R C}$
- $R = \frac{1}{2\pi f_N C} = \frac{1}{(2\pi)(60)(0.068\times10^{-6})}$ = 39.01 KΩ
- For obtaining R/2 use parallel two 39 K resistors and for obtaining 2 C use parallel two capacitors 0.068 μ F

ALL PASS FILTER

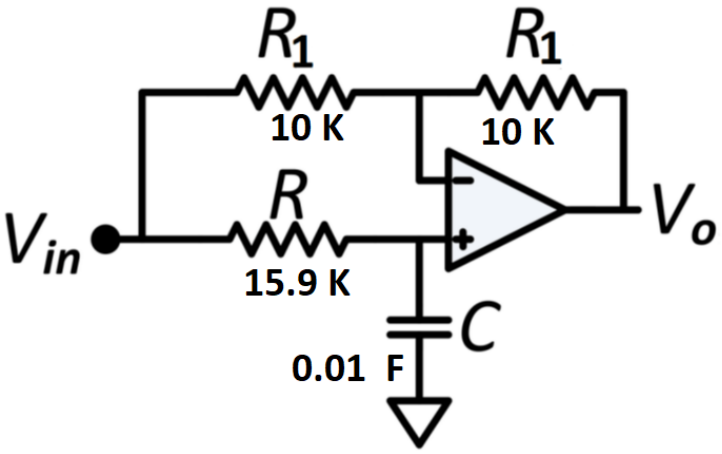
Q 16. What is All pass filter? State its characteristics

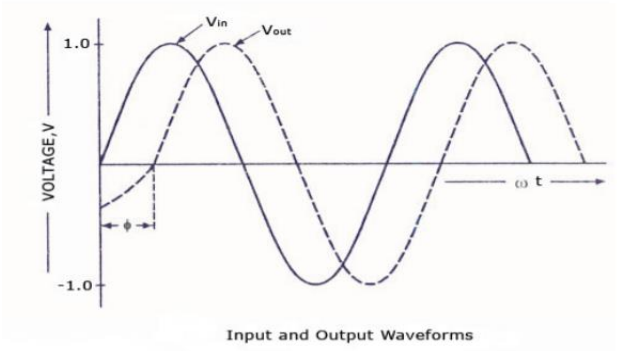
OR

Draw and explain the operation of all pass filter along with its characteristics

FUNCTION OF ALL-PASS FILTER:

- All-pass filter passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different frequencies of the input signal.
- **USEFULNESS OF FILTER**:
  When signals pass through telephone lines, they undergo change in phase. All pass filters are used to compensate for these phase changes. These filters are also called Delay Equalizers or Phase correctors





Input and Output Waveforms

- Reactance of capacitor $-j\,X_C$
- Voltage at point $V_2 = \frac{-j\,X_C}{R - j\,X_C}\ V_{in}$
- Voltage at output V_0 due to V_2

  $V_2 \times (1 + \frac{R_1}{R_1}) = 2\,V_2 = 2\,\frac{-j\,X_C}{R - jX_C}$
- Voltage at output V_0 due to $V_{in} = V_{in} \times \frac{R_1}{R_1} = V_{in}$
- There are two inputs one due to V_{in} another due to V_2
- Using Superposition theorem
- $V_0 = -V_{in} + 2\,\frac{-j\,X_C}{R - jX_C}V_{in} = V_{in}\{-1 + 2\,\frac{-j\,X_C}{R - jX_C}\}$ but $-j = \frac{1}{j}$
- and $X_C = \frac{1}{2\,\pi\,f\,C}$

- $\frac{V_0}{V_{in}} = -1 + 2\ \frac{X_C}{J(R - jX_C)}$
- $\frac{V_0}{V_{in}} = -1 + 2\ \frac{X_C}{J(R - jX_C)} = -1 + 2\frac{\frac{X_C}{X_C}}{\frac{jR}{X_C} - j^2\frac{X_C}{X_C}} = -1 + 2\frac{1}{1 + \frac{jR}{X_C}} =$
- $= -1 + 2\ \frac{1}{(1 + j\ 2\ \pi\ fR\ C)} = \frac{-1\ (1 + J\ 2\ \pi\ f\ R\ C) + 2}{(1 + 2\ \pi\ f\ \ R\ C)} = \frac{(-1 - J\ 2\ \pi\ f\ \ R\ C) + 2}{1 + 2\ \pi\ f\ R\ C} =$ $\frac{1 - J\ 2\ \pi\ R\ C}{1 + J\ 2\ \pi\ f\ R\ C}$
- Gain = $\frac{V_0}{V_{in}} = \frac{1 - J\ 2\ \pi\ f\ R\ C}{1 + J\ 2\ \pi\ f\ R\ C}$
- |Gain| = $\left|\frac{V_0}{V_{in}}\right| = \frac{\sqrt{1^2 + (2\ \pi\ f\ R\ C)^2}}{\sqrt{1^2 + (2\ \pi\ f\ R\ C)^2}} = 1$ because $\left|\frac{a + Jb}{c + Jd}\right| = \frac{\sqrt{a^2 + (b)^2}}{\sqrt{c^2 + (d)^2}}$
- Phase = $\emptyset = \tan^{-1}(-2\ \pi\ f\ R\ C) - \tan^{-1}(2\ \pi\ f\ R\ C)$
- $= -2\ \tan^{-1}(2\ \pi\ f\ R\ C)$
- $|V_0| = |V_{in}|$ Gain is unity for all frequencies
- $\emptyset$ varies between 0^0 to -180^0 for frequency variation from 0 to ∞
- $\emptyset$ is in degrees when f in hertz, R in ohms and C in farads
- If the positions of R and C are interchanged the phase shift $\emptyset$ varies from 0^0 to $+180^0$

PROBLEM 19. For the all-pass filter shown find the phase angle for frequency of V_{in} =1 KHz

- $\emptyset = -2\ \tan^{-1}(2\ \pi\ f\ R\ C)$
- $-2\ \tan^{-1}\ [\ (2\ \pi)\ (10^3\ )\ (15.9 \times 10^3\ )$
  $(0.01 \times 10^{-6}\ )\ = -90^0$
- The output voltage V_0 has the same frequency and amplitude but lags V_{in} by 90^0

PROBLEM 20. For the All pass filter the values of R and C are 7.95 K Ω and 0.02 µF respectively. If the input frequency is 1.5 KHz. Calculate the phase shift

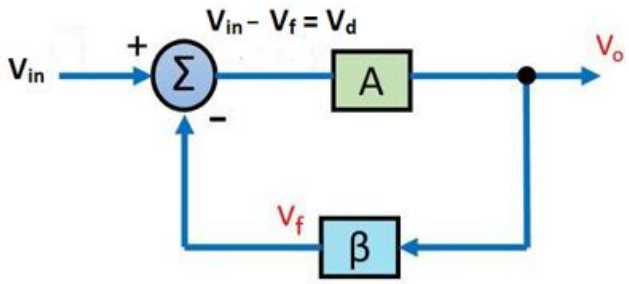
- C = 0.02 µF and R= 7.95 KΩ
- f = 1.5 KHz
- $f = -\ 2\ \tan^{-1}(2\ \pi\ f\ R\ C)$
- $-\ 2\ \tan^{-1}(2\ \pi\ (1.5 \times 10^3\ )\ (7.95 \times 10^3\ )(0.02 \times 10^{-6}\ )$
- $= -112.56^0$
- The output voltage lags input by 112.56^0
- The amplitude and frequency of output will be same as that of input

OSCILLATORS USING OP-AMPS

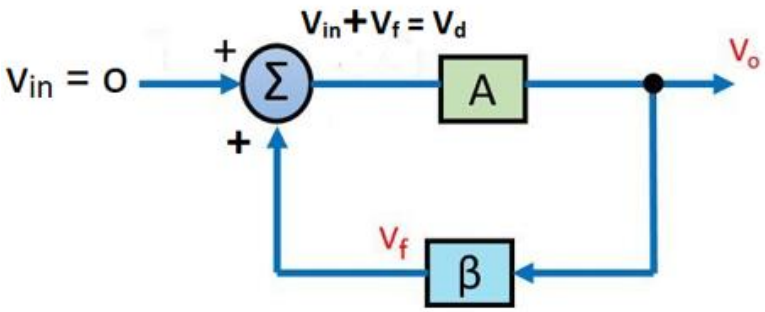
Q 17. Compare Positive Feedback And Negative Feedback

The parameter of comparison	Positive feedback	Negative feedback
The overall phase shift	0 or 360^0	180^0
Feedback signal and the input signal.	In phase.	Out of phase.
Input voltage.	Increase due to feedback.	Decrease due to feedback.
Out put voltage.	Increase due to feedback.	Decrease due to feedback
Voltage gain.	Increase due to feedback.	Decrease due to feedback.

The parameter of comparison	Positive feedback	Negative feedback
Stability.	Becomes poor	Becomes better
Noise	Increase with feedback.	Decrease with feedback.
Bandwidth	Decrease with positive feedback.	Increase with negative feedback.
Application	Oscillators Schmitt trigger.	amplifier.



Negative Feedback Operation



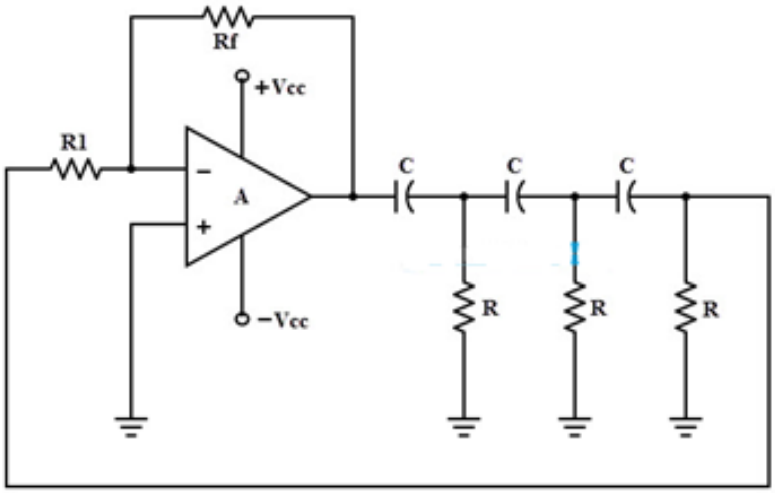
Q 17. State the THE BARKHAUSENS CRITERION

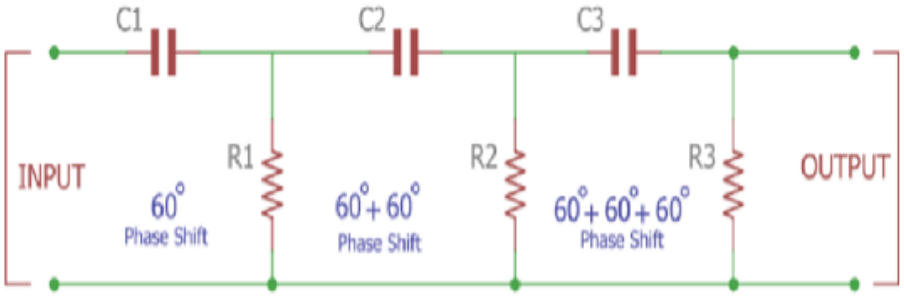
- The total phase shift around a closed loop as the signal proceed from input through amplifier output, feedback network back to input completing a closed loop is 00 or 3600 or n 2π where n= integer
- The magnitude of the product of the open loop gain of the amplifier (A) and feedback factor β is unity i.e. Aβ= 1

RC PHASE SHIFT OSCILLATOR

Q 18. Explain the function of RC oscillator using op-amp. State the expression for its frequency of operation

- **RC PHASE SHIFT OSCILLATOR:**
- The Phase Shift Oscillator consists of an operational amplifier and three RC cascaded networks in the feedback
- 360^0 phase shift is required to sustain oscillation at the given frequency of the oscillator i) 180^0 phase shift is obtained by using the Op-Amp by connecting it in Inverting mode of operation ii) the other 180^0 phase shift is provided by the feedback circuit. Three RC networks are connected in series and each network provides 60^0 phase shift
- At the specific frequency when the total phase shift is 360^0 the circuit oscillates provided the loop gain Aβ is = 1 (**BARKHAUSENS CRITERION)**
- **FREQUENCY OF OSCILLATION:**
- From theory it is known for 3 numbers of RC networks each giving 60^0 phase shift
- frequency of oscillation $f_O = \frac{1}{2\,\pi\,R\,C\,\sqrt{6}} = \frac{0.065}{RC}$
- Each network acts as a load for its previous network . From the theory to maintain the overall loop gain (for oscillations) =1 it can be deduced that the minimum gain of the inverted configuration must be 29
- $\frac{R_f}{R_1} \geq 29$ ie $R_f \geq 29\ R_1$





Three Pole Phase Shift RC Oscillator

PROBLEM 21. Design the RC phase shift Oscillator for a frequency of f_0 = 200 Hz

- Choose a capacitor with C = 0.1 μ F
- $f_o = \frac{1}{2\pi R\ C\sqrt{6}} = \frac{0.065}{R\ C}$
- $R = \frac{0.065}{f_0\ C} = \frac{0.065}{(200)\ (0.1 \times 10^{-6})}$ =3.25 KΩ
- In order to prevent loading of R (3.3 K) of third RC network the R_1 should be ≥ 3.3 K
  ∴ R_1 = 10 × 3.3 K = 33K Ω
- R_F = 29 × 3.3k = 957 K Ω (1 M Ω pot-meter may be used)
- For lower frequencies (< 1 KHz) op-amp 741 may be used
- For higher frequencies LM 318 may be used . It's slew rate is higher.

Q 19. State the advantages and limitations of RC phase shift oscillators

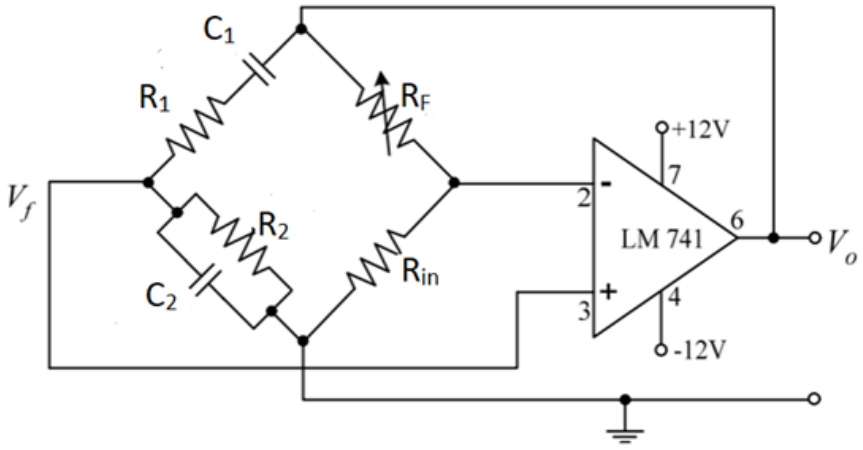
- **ADVANTAGES OF PHASE SHIFT OSCILLATORS**
- **1**. Due to the absence of expensive and bulky high-value inductors, circuit is simple to design and well suited for frequencies below 10 KHz.
- **2.** These can produce pure sinusoidal waveform since only one frequency can fulfill the Barkhausen phase shift requirement.
- **3**. It is fixed to one frequency.
-

- **DISADVANTAGES OF PHASE SHIFT OSCILLATORS**
- 1. For a variable frequency usage, phase shift oscillators are not suited because the capacitor values will have to be varied. And also, for frequency change , every time requires gain adjustment for satisfying the condition of oscillations.
- 2. These oscillators produce 5% of distortion level in the output.
  3. This oscillator gives only a small output due to smaller feedback
- 4. These oscillator circuits require a high gain which is some times practically impossible.
- 5. The frequency stability is poor due to the effect of temperature, aging, etc. of various circuit components.

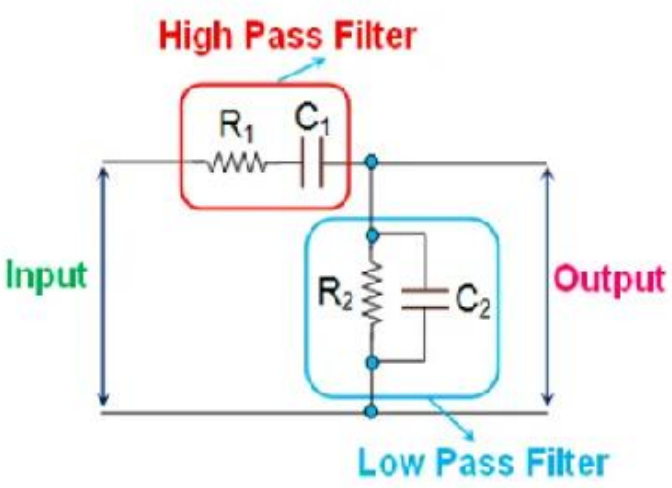
WIEN BRIDGE OSCILLATOR

Q 20. Draw the circuit of wien bridge oscillator using op-amp and explain its operation

- Due to the advantages like good frequency stability, very low distortion and ease of tuning, a Wien bridge oscillator becomes the most popular audio frequency range signal generator circuit.
- The main difference between the general oscillator and Wien bridge oscillator is that in an oscillator, amplifier stage introduces 180 degrees phase shift and additional 180 degrees phase shift is introduced by feedback network so as to obtain the 360 degrees or zero phase shift around the loop to satisfy the Barkhausen criteria.
- But, in case of the Wien bridge oscillator, a Non -inverting amplifier is used in amplifier stage. This does not introduce any phase shift. Hence there is no need of phase shift through feedback network that is required in order to satisfy the Barkhausen criteria..
- Wien bridge oscillator is an audio frequency sine wave oscillator of high stability and simplicity. The feedback signal in this circuit is connected to the non-inverting input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series combination of R1 and C1 in one arm and parallel combination of R2 and C2 in the adjoining arm. Resistors R3 and R4 are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge.
- The series and parallel combination of RC network form a lead-lag circuit. At high frequencies, the reactance of capacitor C1 and C2 approaches zero. This causes C1 and C2 appears short. Here, capacitor C2 shorts the resistor R2. Hence, the output voltage Vo will be zero since output is taken across R2 and C2 combination. So, at high frequencies, circuit acts as a 'lag circuit'.
- At low frequencies, both capacitors act as open because capacitor offers very high reactance. Again, output voltage will be zero because the input signal is dropped across the R1 and C1 combination. Here, the circuit acts like a 'lead circuit'.



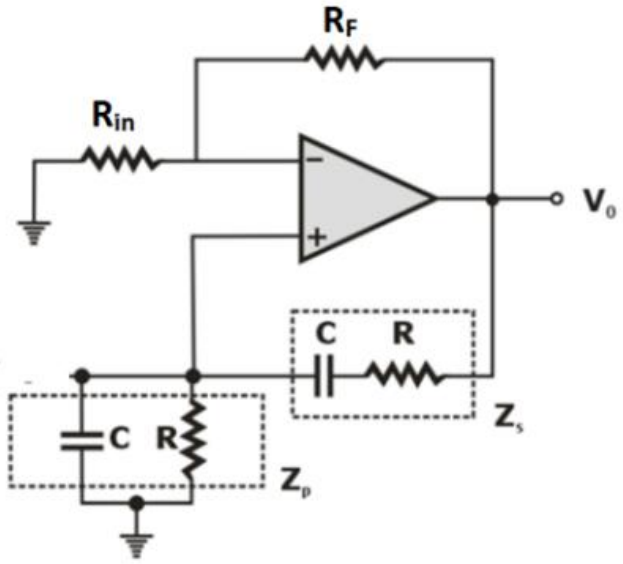
- But at one particular frequency between the two extremes, the output voltage reaches to the maximum value. At this frequency only, resistance value becomes equal to capacitive reactance and gives maximum output. Hence, this frequency is known as oscillating frequency (f)



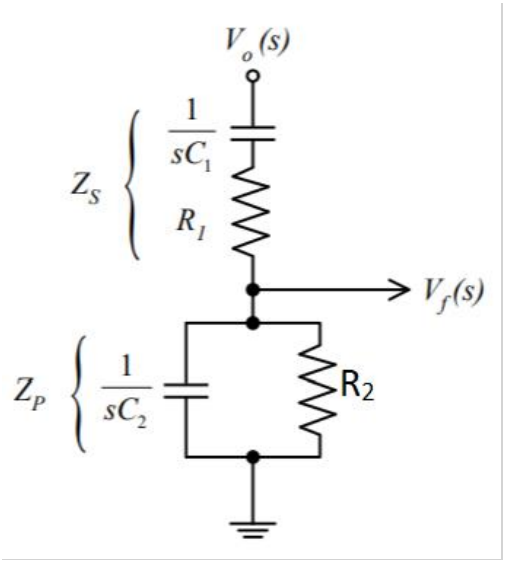
Two arms of the Wien-Bridge Network

- The same circuit is drawn as given

$$f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$



- Using the voltage divider rule
- $V_f = \frac{V_0 Z_P}{Z_P + Z_S}$
- For simplification we take $R_1 = R_2 = R$ and $C_1 = C_2 = C$



- $Z_P = R \,||\, \frac{1}{SC} = \frac{R\,\frac{1}{SC}}{R+\frac{1}{SC}} = \frac{\frac{R}{SC}}{\frac{RSC+1}{SC}} = \frac{R}{1+SRC}$
- $Z_S = R + \frac{1}{SC} = \frac{SRC+1}{SC}$
- Feed back $\beta = \frac{V_f}{V_0} = \frac{Z_P}{Z_P+Z_S} = \frac{\frac{R}{1+SRC}}{\frac{R}{1+SRC}+\frac{1+SRC}{SC}} = \frac{\frac{R}{1+SRC}}{\frac{SRC+(1+SRC)^2}{SC\,(1+SRC)}}$

$$\beta = \frac{SRC}{SRC+(1+SRC)^2} = \frac{SRC}{SRC+1+2SRC+S^2(RC)^2}$$

$$= \frac{SRC}{S^2(RC)^2+3SRC+1}$$

- $\beta = \frac{SRC}{S^2(RC)^2+3SRC+1}$ = Divide all terms by S R C

  $\beta = \frac{1}{SRC+3+\frac{1}{SRC}}$

  Gain of Non inverting Amplifier = $A_V = \frac{V_0}{V_f} = (1+\frac{R_F}{R_{in}})$

  But $A_v\ \beta = 1$ for oscillation
- $\therefore A_v\ \beta = (1+\frac{R_F}{R_{in}})\ (\frac{1}{SRC+3+\frac{1}{SRC}}) = 1$ But $S = j\omega$

  $(\frac{1}{j\omega RC+3+\frac{1}{j\omega RC}}) = \frac{1}{(1+\frac{R_F}{R_{in}})} = (\frac{1}{j\omega RC+3-j\frac{1}{\omega RC}})$
- Imaginary part is zero since phase=0 $\therefore\ \omega RC - \frac{1}{\omega RC} = 0$

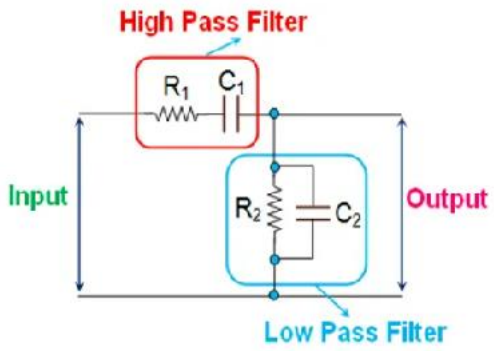
$\omega RC = \frac{1}{\omega RC}$ $\therefore\ \omega^2 = \frac{1}{(RC)^2}$ and $2\pi f_0 = \frac{1}{RC}$

$\therefore\ f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$

- Real part $\frac{1}{3} = \frac{1}{(1+\frac{R_F}{R_{in}})} \therefore 3 = 1 + \frac{R_F}{R_{in}}$
- $R_F = 2\ R_{in}$

ALTERNATIVE DERIVATION:

- Here, we can break the loop at the positive input of the op-amp and calculate the returning signal using the following Equation :



Two arms of the Wien-Bridge Network

-

$$\frac{V_{RETURN}}{V_{OUT}} = \frac{\frac{R}{RCs+1}}{\frac{R}{RCs+1}+R+\frac{1}{Cs}} = \frac{1}{3+RCs+\frac{1}{RCs}} = \frac{1}{3+j\left(RC\omega-\frac{1}{RC\omega}\right)},$$

where $s = j\omega$ and $j = \sqrt{-1}$.

- Phase shift =0 ∴ j term =0 ∴ RC $\omega = \frac{1}{R\,C\,\omega}$ ∴ $\omega^2 = \frac{1}{(R\,C)^2}$
- When $\omega = 2\pi f = 1/RC$, the feedback is in phase (positive feedback), having a gain of 1/3.
- Therefore the oscillations needs the op-amp circuit to have a gain of 3.
- When $R_f = 2R_G$, the amplifier gain is 3 and oscillation initiates at $f = 1/2\pi RC$.

PROBLEM 22. Design a Wien- bridge oscillator so that f_0 = 965 Hz

- Let C= 0.05 μ F
- But $f_0 = \frac{0.159}{R\,C}$ ∴ $R = \frac{0.159}{(0.05)(10^{-6})(965)} = 3.3\ K\Omega$
- Let R_{in} = 12 KΩ ∴ $R_F = 2 \times 12 = 24\ K\ \Omega$ (50 K pot-meter may be used)

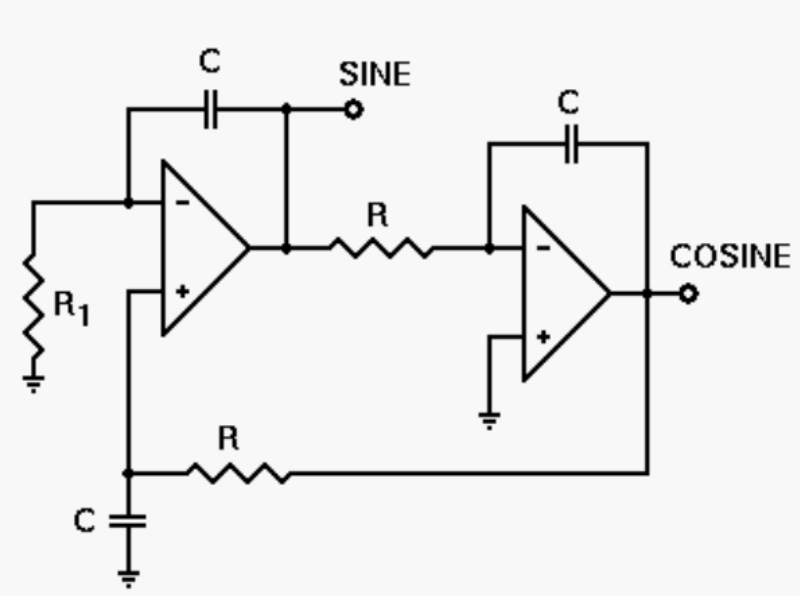
Q 21. State the advantages and limitations of Wien bridge oscillator

- **ADVANTAGES:**
- 1. By changing resistance , the frequency range can be selected easily.
- 2. By varying capacitances C the frequency of oscillation can be easily varied.
- 3. Over a wide range of frequency, it provides a stable low distortion sinusoidal output.

- 4. Good for audio frequencies
- **DISADVANTAGES:**
- 1. The maximum frequency output is limited because of the amplitude and phase shift characteristics of the amplifier.
- 2. Frequency stability is poor due to variations in temperature

QUADRATURE OSCILLATOR

Q 22. Draw the circuit of Quadrature oscillator using op-amp and explain its operation



FUNCTION OF QUADRATURE OSCILLATOR:

- This generates two signals i) cosine ii) sine. These signals are quadrature signals that is out of phase by 90^0 .
- Output of A_1 may be labeled as Sine and output of A_2 as Cosine. This configurations requires two Op-Amps. A_1 is operating in Non inverting mode. It is a noninverting integrator.
- A_2 operates in Inverting configuration and is followed by R and C voltage divider.
- The divider network acts as the feedback
- The requirement of 360^0 is fulfilled in the following manner.
- A_2 is the pure integrator and invertor. So it gives $-(180^0 + 90^0) = -270^0$ phase shift The remaining -90^0 is provided by the voltage divider and Amplifier A_1 . The total phase shift of 360^0 occurs at only one frequency and this is called frequency of oscillation.
- For simplicity sake put $R_1 C_1 = R_2 C_2 = R C$ and $R_1 = R_2 = R$ and $C_1 = C_2 = C$
- $f_0 = \frac{1}{2 \pi R C}$
- The second condition for oscillation is
- $A_v = \frac{1}{\beta} = 1.414$

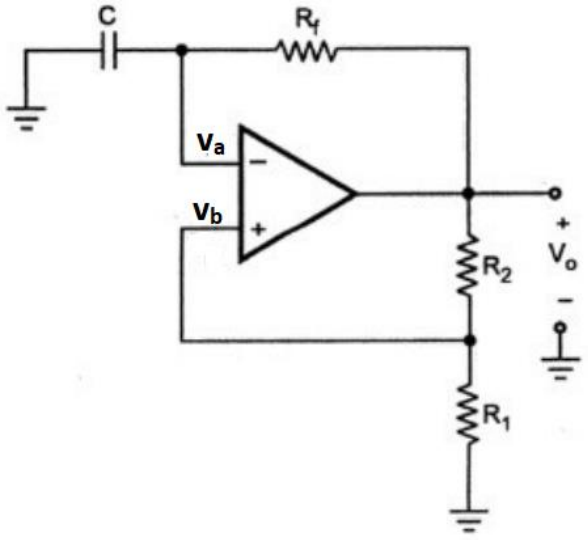
PROBLEM 23. Design the Quadrature oscillator so that f_0 = 150 Hz

- Let C= 0.001 μ F
- $f_0 = \frac{1}{2\pi R C}$
- $R = \frac{1}{(2\pi)(159)(0.01\times10^{-6})}$ =100 KΩ

ASTABLE MULTI VIBRATOR

Q 23. Explain the operations of op-amp astable multi vibrator. Suggest a method of restricting the output swing to predetermined values. State the expression for the frequency of oscillations

- A square wave generator using op-amp can also be called as an Astable multivibrator or free running multivibrator.
- No external signal is required to produce the oscillations. Since it oscillates and produces square wave output it is also called Square wave generator. The circuit is built using Schmitt trigger configuration except the input voltage is replaced with a capacitor.



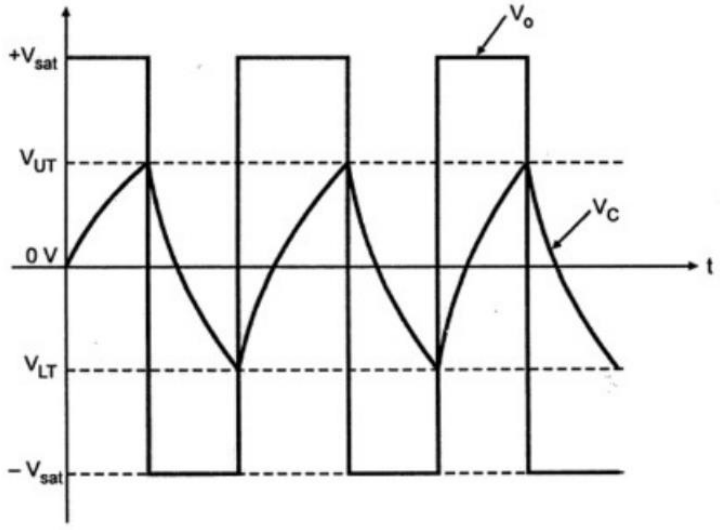
- When output voltage V_O is at $+V_{sat}$ the voltage v_b (at noninverting input) is given as

  $+V_{sat}\frac{R_1}{R_1+R_2} = v_{UT}$
- When output voltage V_O is at $-V_{sat}$ the voltage v_b (at noninverting input) is given as

  $-V_{sat}\frac{R_1}{R_1+R_2} = v_{LT}$
- The sequence of events that occur when power is turned on to the circuit is given below

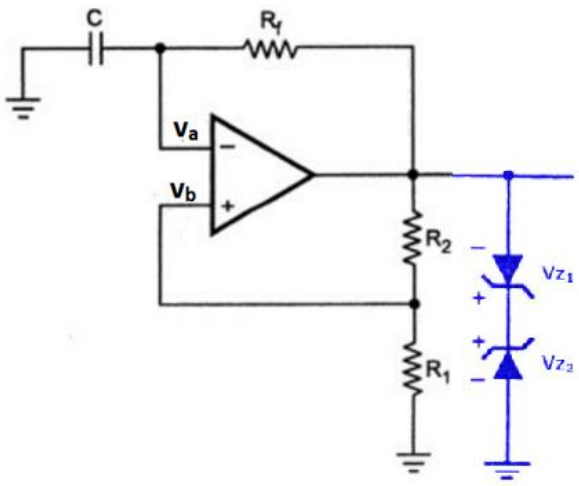
- **1.** When power is turned on , V_o automatically takes a value either + V_{sat} or $-V_{sat}$ because these are the only two states of the Schmitt trigger. Let us assume Output V_0 has taken a value + V_{sat} then V_b

  $v_{UT} = +V_{sat} \frac{R_1}{R_1+R_2}$
- **2**. Capacitor C starts charging from '0' voltage towards + V_{sat} through the feedback resistor R_f . This voltage appears at –ve terminal of op-amp as V_a. As long as V_a is less than , V_b the output voltage remain at $+V_{sat}$.
- **3**. The instant V_a (capacitor charging voltage) exceeds V_b (ie V_{UT})
  $V_a > V_b$, the V_0 swings to $-V_{sat}$. Since +ve feedback is applied through R1 and R2 the change from $+V_{sat}$ to $-V_{sat}$ is fast.
- **4**. Voltage v_b will change to $V_{LT} = -V_{sat} \frac{R_1}{R_1+R_2}$



- 5. Since V_0 has changed from $+V_{sat}$ to $-V_{sat}$ Capacitor starts discharging through R_F . From v_{UT} , v_a reaches zero and start recharging towards $-V_{sat}$.
- **6**. The instant V_a (capacitor charging voltage) becomes more negative than V_b (ie $V_{LT} = -V_{sat} \frac{R_1}{R_1+R_2}$), $V_a < V_b$, the V_0 swings back to $+V_{sat}$. The cycle repeats once again from step No. 1 above

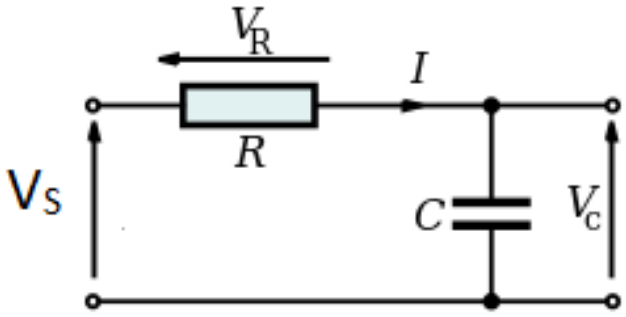
METHOD TO RESTRICT THE OUTPUT SWING TO PREDETERMINED VALUES:

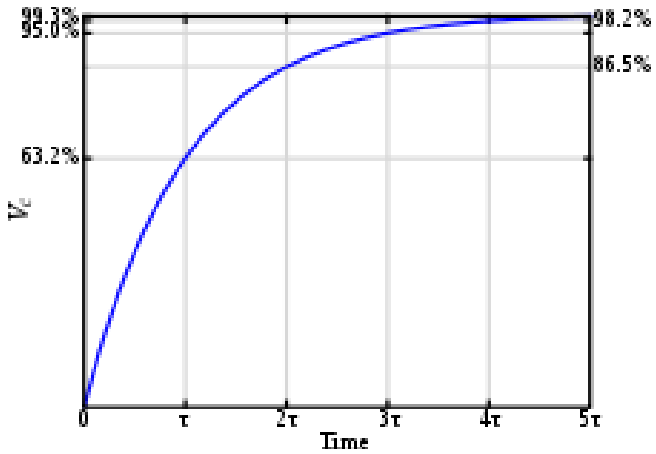


EXPRESSION FOR THE FREQUENCY OF OSCILLATION:

- $T = 2\ R_f\ C\ \ln\left[\frac{2\ R_1+R_2}{R_2}\right]\ sec$
- Frequency = $\frac{1}{T}$ Hz

WITH ZERO INITIAL CONDITION





$$v_C(t) = V_S\ (1\ -\ e^{\frac{-t}{R\ C}})$$

WITH INITIAL CONDITION V_{in}

$$v_C(t) = V_f + (V_{in} - V_f)\, e^{\frac{-t}{R_f C}}$$

PROBLEM 24. Design a square wave (astable multi vibrator) using op-amp with frequency of 10 KHz and using 0.1 µF

- Supply voltages are ∓15 V and magnitudes + V_{sat} and $-V_{sat}$ are equal
- $f = \frac{1}{2 R_f C \ \ln\left[\frac{2R_1+R_2}{R_2}\right]}$
- Choose R_1 and R_2 such that $\ln\left[\frac{2R_1+R_2}{R_2}\right] = 1$, Taking antilogarithms
- $\left[\frac{2R_1+R_2}{R_2}\right] = 2.7183 = \frac{2R_1}{R_2} + 1 \therefore R_1 = \frac{1.7183}{2} R2 = 0.86\ R_2$
- Let R_1 = 100 K $\therefore R_2$ = 86 KΩ
- $f = (10)(10^3) = \frac{1}{2 R_f C} = \frac{1}{2 R_f (0.1)(10^{-6})} \therefore R_f = 500\ \Omega$

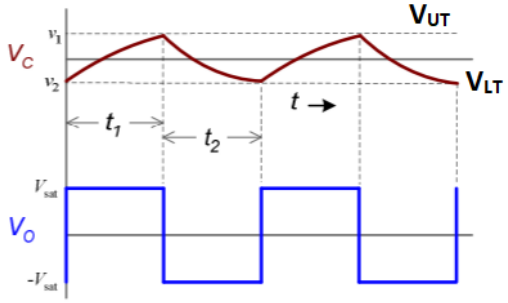
Q 24. Derive the expression for the time period of square wave generator (astable multivibrator)

- The frequency of oscillation is determined by the time it takes the capacitor to charge from V_{LT} to charge V_{UT} and vice versa
- From theory the voltage across a capacitor in a 'R C ' network is given by

$$v_C(t) = V_f + (V_{in} - V_f)\, e^{\frac{-t}{R_f C}}$$

Where V_f = final voltage towards which the capacitor charges to + V_{sat}

- V_{in} = initial voltage V_{LT}
- $v_C(t)$ = voltage across charging capacitor
- $\therefore v_C(t) = (+V_{sat}) + [V_{LT} - (+V_{sat})]\, e^{\frac{-t}{R_f C}}$
- At t= t_1 voltage across capacitor reaches V_{UT}
- $V_{UT} = \{(+V_{sat}) + [V_{LT} - (+V_{sat})]\, e^{\frac{-t_1}{R_f C}}$



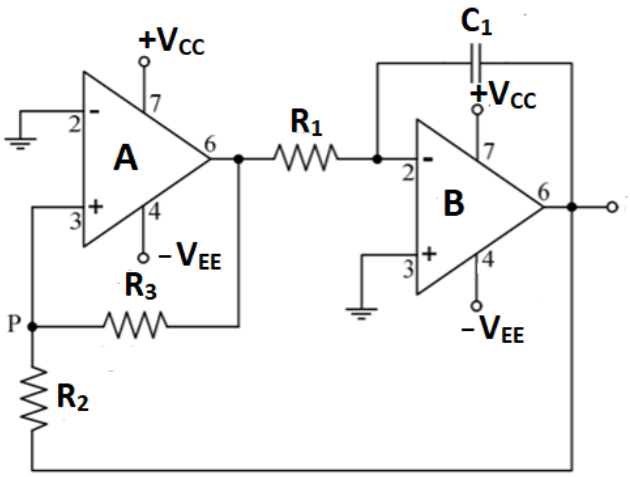
- $V_{UT} = (+V_{sat}) + [V_{LT} - (+V_{sat})] e^{\frac{-t_1}{R_f C}}$
- $[V_{UT} - (+V_{sat})] = [V_{LT} - (+V_{sat}) e^{\frac{-t_1}{R_f C}}$
- $e^{\frac{-t_1}{R_f C}} = \frac{[VUT - (+V_{sat})]}{[VLT - (+V_{sat})]} = \frac{[V_{UT} - (+V_{sat})]}{[V_{LT} - (+V_{sat})]} = \frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}$
- Taking logarithms to the base 'e'
- $\frac{-t_1}{R_f C} = \ln \frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}$ and $-t_1 = R_f C \ln \frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}$
- $t_1 = R_f C \ln \frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}$
- The time taken by capacitor to charge from V_{UT} to V_{LT} is same as time required for charging capacitor from V_{LT} to V_{UT} . The total time required for one oscillation is given as $T = 2 t_1$
- $V_{UT} = \frac{+V_{sat} R_1}{R_1 + R_2}$ and $V_{LT} = \frac{-V_{sat} R_1}{R_1 + R_2}$
- $2t_1 = T = 2 R_f C \ln \frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}} = 2 R_f C \ln \frac{+V_{sat} - \frac{-V_{sat} R_1}{R_1 + R_2}}{+V_{sat} - \frac{+V_{sat} R_1}{R_1 + R_2}}$
- $T = 2 R_f C \ln \frac{+V_{sat} (1 + \frac{R_1}{R_1 + R_2})}{+V_{sat} (1 - \frac{R_1}{R_1 + R_2})} = 2 R_f C \ln \frac{+V_{sat} [1 + \frac{R_1}{R_1 + R_2}]}{+V_{sat} [1 - \frac{R_1}{R_1 + R_2}]} =$
- $T = 2 R_f C \ln \frac{2R_1 + R_2}{R_2}$
- If $R_2 = 1.16 R_1$ $\therefore \ln \frac{2R_1 + R_2}{R_2} = \ln \frac{2 R_1 + 1.16 R_1}{1.16 R_1} = \ln \frac{3.16}{1.16} = 1$
- $T = 2 R_f C$

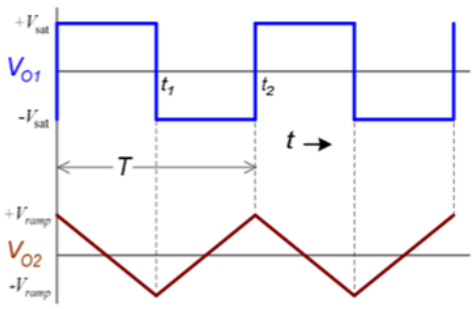
$f = \frac{1}{2 R_f C}$ if $R_f = R$ then $f = \frac{1}{2 R C}$

TRIANGULAR WAVEFORM GENERATOR

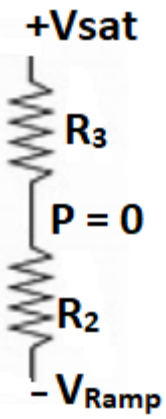
Q 25. Explain the triangular waveform generator

- Triangular waves can also be generated by integrating the output of symmetrical square wave generated by the astable multivibrator.





- The op-amp A circuit is Schmitt trigger . The op-amp B circuit is an integrator
- Output of Schmitt trigger is square wave of $\pm V_{sat}$. It is applied to the inverting input of an integrator B
- Output of the integrator is feedback as input to Schmitt trigger through voltage divider R_2 and R_3
- Assume that the output of Schmitt trigger A is at +Vsat.
- This forces a constant current $\frac{+V_{sat}}{R_1}$ through C_1 to give a negative going ramp at the output of the integrator. The time interval is 0 to t_1
- The output of B will be a negative going ramp. Thus one end of the voltage divider R1 and R2 is at $+V_{sat}$ and other is at the negative going ramp. At time t=t1 ; when the –ve going ramp attains value of $-V_{ramp}$ the effective voltage at point P first becomes zero and later slightly less than 0. This changes output of A from $+V_{sat}$ to $-V_{sat}$.
- This forces a reverse current (right to left) through C_1 to give a positive going ramp at the output of the integrator, as shown in the figure.
- When positive going ramp reaches $+V_{ramp}$, the effective voltage at point P becomes slightly above 0 V. As a result, the output of Schmitt trigger A switches from $-V_{sat}$ to $+V_{sat}$. The sequence then repeats to give triangular wave at the output of integrator B
- **FREQUENCY OF TRIANGULAR WAVE:**
- The frequencies of square wave and the triangular wave are same. The amplitude of square wave is a function of DC supplies given to Op-amp. However they can be controlled by using Zener diodes at the output.
- When the output of comparator is $+V_{sat}$, the output of integrator A2 steadily decreases until it reaches $-V_{ramp}$. At this time voltage at 'P' just crosses zero voltage and output of comparator changes from $+V_{sat}$ to $-V_{sat}$
- At the moment when voltage at P=0
- $+V_{sat}$ must be developed across R_3 and $-V_{ramp}$ must be developed across R_2



- $\frac{-V_{Ramp}}{R_2} = -\frac{+V_{sat}}{R_3}$
- $-V_{Ramp} = -\frac{R_2}{R_3}(+V_{sat})$
- Similarly the output voltage of B at which the output of A switches from $-V_{sat}$ to $+V_{sat}$ is given by
- $+V_{Ramp} = -\frac{R_2}{R_3}(-V_{sat})$
- Peak to peak output change at point 'P' is
- $v_0(pp) = +V_{Ramp} - (-V_{Ramp}) = 2\frac{R_2}{R_3}(V_{sat})$ where
- $V_{sat} = |+V_{sat}| = |-V_{sat}|$
- By increasing R_3 the amplitude of triangular wave can be decreased
- From the integrator equation
- Let the time taken to change from $-V_{sat}$ to $+V_{sat}$ is denoted by T/2
- $v_o(pp) = -\frac{1}{R_1 C_1}\int_0^{T/2}(-V_{sat}) = \left(\frac{V_{sat}}{R_1 C_1}\right)\left(\frac{T}{2}\right)$
- $T = (2 R_1 C_1)\frac{v_0(pp)}{V_{sat}}$ but $v_0(pp) = 2\frac{R_2}{R_3}(V_{sat})$
- $T = (2 R_1 C_1)\frac{2\frac{R_2}{R_3}(V_{sat})}{V_{sat}} = \frac{4 R_1 C_1 R_2}{R_3}$
- frequency of oscillation $f_0 = \frac{R_3}{4 R_1 C_1 R_2}$

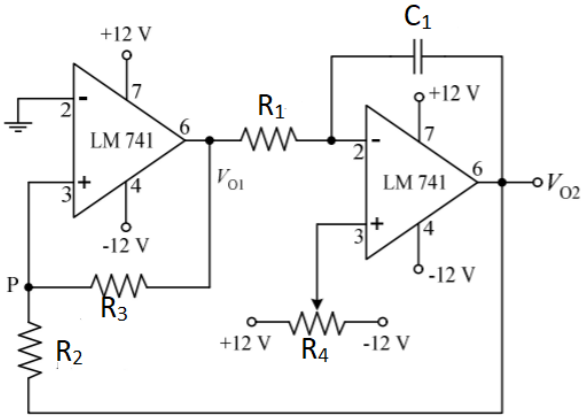
PROBLEM 25. Design a triangular wave generator so that f_0 = 2 KHz and v_0 (peak to peak) = 7V Supply voltages = ± 15 V

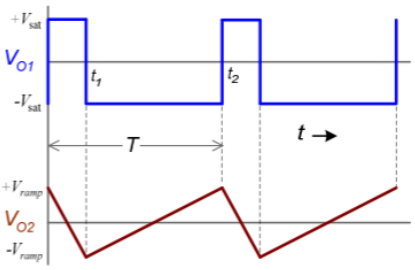
- Let V_{sat} =14 V
- $v_0(pp) = 2\frac{R_2}{R_3}(V_{sat})$
- $\frac{R_2}{R_3} = \frac{v_0(pp)}{2 V_{sat}} = \frac{7}{(2)(14)}$ $\therefore 4R_2 = R_3$ ∴Let R_2 = 10 KΩ then R_3 =40 KΩ
- $f_0 = \frac{R_3}{4 R_1 C_1 R_2} = 2000 = \frac{(40)(10^3)}{(4)(R_1 C_1)(10)(10^3)}$ ∴ $R_1 C_1 = (0.5)(10^{-3})$sec

- Let C_1 = 0.05 μF $\therefore R_1 = \frac{(0.5)(10^{-3})}{(0.05)\ (10^{-6})}$ = 10 KΩ

SAW TOOTH GENERATOR

Q 26. With the help of neat diagram explain the operation of sawtooth wave generator using op-amp





DIFFERENCE BETWEEN TRIANGULAR AND SAWTOOTH WAVEFORM:

- The rise and fall times of triangular wave is equal
- The rise and fall times of sawtooth wave is different. It may rise much faster than it may fall negatively or vice versa.

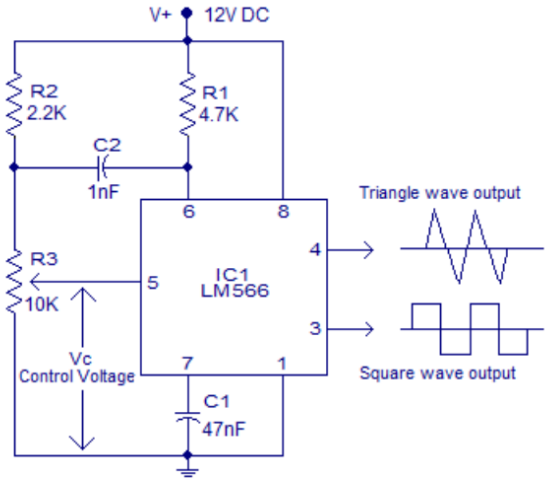
CIRCUIT OPERATION

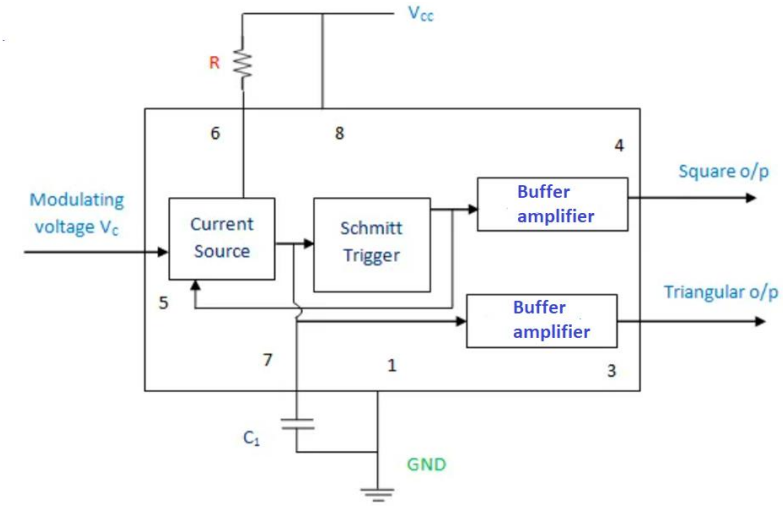
- The triangular wave generator can be converted into a sawtooth generator by injecting a variable dc voltage into the noninverting terminal of integrator A_2 . This can be done by using the potentiometer and connecting it to $+V_{CC}$ and $-V_{EE}$
- With the wiper at the center of pot-meter R_4 the output of A_2 is a triangular wave. For any other position of the R_4 the output is a saw tooth wave form
- Depending on the R_4 setting , a certain dc level is inserted in the output of A_2 . Certain dc level is added to the output triangular wave . This means the triangular wave is riding over a dc level
- If R_4 wiper is moved toward $-V_{EE}$ the rise time of saw tooth becomes longer than the fall time. If the wiper is moved toward $+V_{CC}$ the fall time becomes longer than the rise time
- Reason is when comparator output is at −ve saturaion. When wiper moves to −ve supply, a negative voltage is added to inverting terminal.
- This causes the potential difference across R1 decreases and hence the current through the resistor and capacitor decreases . Then slope of the output, I/C decreases and in turn rise time decreases
- When the comparator output goes positive , due to presence of negative voltage at the inverting terminal, potential difference of across the resistor R1 increases and hence current increases. Then slope increases and fall time decreases .

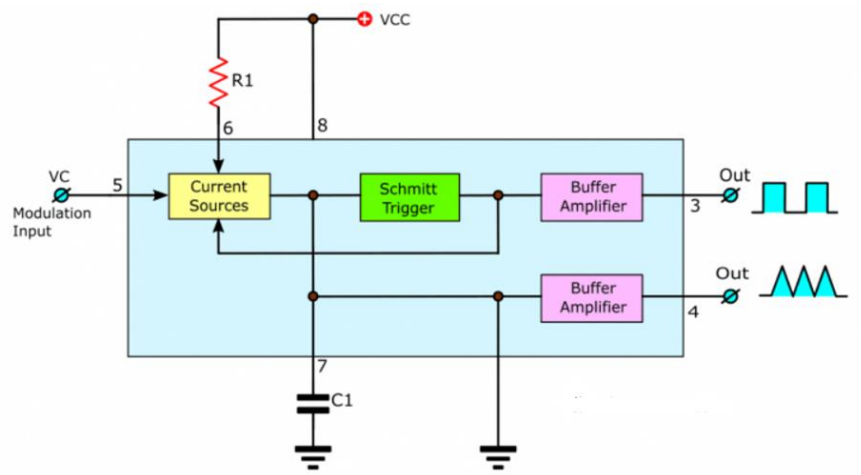
VOLTAGE CONTROLLED OSCILLATOR

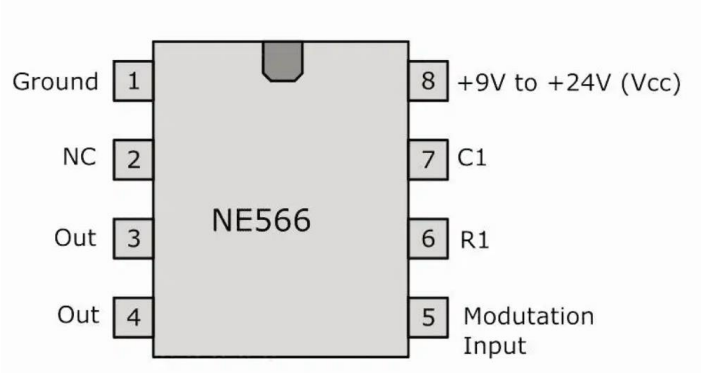
Q 27. Draw the block diagram of IC 566 VCO and explain its operation

- In normal oscillators the frequency is determined by the RC time constant.
- In VCOs (Voltage controlled oscillators the frequency is controlled by an external control voltage. The circuit is also called Voltage to frequency converter. VCOs are used for applications such as Frequency modulations (FM) ,tone generators, Frequency shift keying (FSK) etc.
- Typical commercial VCO is the NE/SE 566 made by M/S Signetics Inc. This IC provides both Square wave and triangular outputs
- The frequency of oscillations is determined by an external resistor R_1 Capacitor C, and control voltage V_c applied to the control terminal 5
- The triangular is generated by alternatively charging C_1 by one current source and by linearly discharging it by another. Schmitt trigger determines the charging and discharging levels. The Schmitt trigger provides the square wave output. Both the outputs are buffered so that the output impedance of each is $50\ \Omega$. The typical amplitude of the triangular wave is 2.4 Volts peak to peak and that of square wave is 5.4 peak to peak.

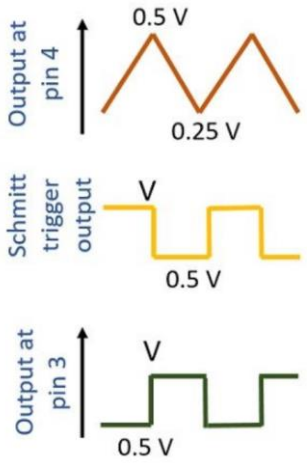








- The R_1 C_1 determines the frequency of oscillation. The control voltage V_C at terminal 5 is determined by the voltage divider formed with R_2 and R_3 . The initial voltage V_C at terminal 5 must be in the range
- $\frac{3}{4}(+V) \leq V_C \leq +V$ where +V is the total supply voltage
- The modulating signal is ac coupled with the capacitor C and must be < 3 V pp
- $f_0 \cong \frac{2(+V - V_C)}{R_1 C_1 (+V)}$ where R_1 should be in the range 2 KΩ < R_1 < 20 ΩK
- i) for a fixed V_C and C_1 , the frequency f_o can be varied by a 10:1 frequency range by choosing R_1 between 2 K Ω to 20 KΩ
- ii) for a constant R_1 C_1 product the frequency can be modulated over 10 : 1 range by varying the control voltage V_C
-



- iii) a smaller value capacitor 0.001 µF should be connected between 5 and 6 to eliminate oscillatons in the control current source
- If VCO is required to be used to drive logic circuits , dual supply of ± 5V is used so that the square has the proper DC levels

PROBLEM 26. + V =12 v , R_2 = 1.5 KΩ , R_1 = R_3 =10 KΩ and C_1 = 0.001 µF

- **a) determine the nominal frequency of the output wave forms**
  b) Compare the modulation in the output frequencies if V_c is varied between 9.5 v and 11.5 v
- **c) Draw the square wave output waveform if the modulating input is a sine wave**
- V_c at terminal 5 is $V_C = \frac{(10)(10^3)(12)}{(10+1.5)(10^3)}$ = 10.43 V
- $f_0 \cong \frac{2\,(+V - V_C)}{R_1\,C_1\,(+V)} = \frac{2\,(12 - 10.43)}{(10)(10^3)(0.001)(10^{-6})(12)}$ = 26.17 KHz
- b) f_0 (max) = $\frac{2\,(12 - 9.5)}{(10)(10^3)(0.001)(10^{-6})(12)}$ = 41.67 KHz

  f_0 (max) = $\frac{2\,(12 - 11.5)}{(10)(10^3)(0.001)(10^{-6})(12)}$ = 8.33 KHz
- Change in output frequency = 41.67−8.33 = 33.34 kHz
- C) During positive half cycle of the Sine wave V_C is increasing . So f_o will decrease which means the time period increases.
  During negative half cycle the opposite occurs and the time period decreases

Q 28. What are the applications of VCO 566

- 1. Function generator
- 2. Phase Locked loop
- 3. Tone Generator
- 4. Frequency Shift Keying
- 5. Frequency modulation
- 6. frequency multipliers
- 7. Converting low frequency signals such as EEG Electroencephalography and EKG (Electro Kardio Gram) into audio frequency range signals

UNIT 3 CONCLUDED

LINEAR INTEGRATED CIRCUIT APPLICATION
(ECE 404 PC)
UNIT -4

TIMERS & PHASE LOCKED LOOPS:

Introduction to 555 Timer, functional diagram, Monostable and Astable operations and applications, Schmitt Trigger , PLL – Introduction , block schematic, principles and description of individual blocks of 565

Text books :

1. Linear integrated circuit by D.Roy chowdhary New Age International(P) Ltd
2. Op Amps & linear ICs Ramakanth, A,Gayakwad , PHI

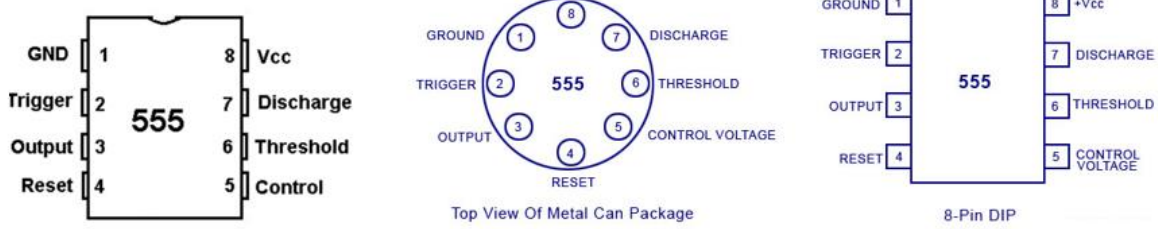
Q 1. Draw and explain the functional diagram of IC 555

- The 555 timer IC was introduced in the year 1970 by M/S. Signetic Corporation and gave the name SE/NE 555 timer.
- It is basically a monolithic timing circuit that produces accurate and highly stable time delays or oscillations.
- When compared to the applications of an op-amp in the same areas, the 555 C is also equally reliable and is cheap in cost.
- It is used as a Monostable multivibrator, Astable multivibrator and Schmitt trigger
- Applications include dc-dc converters, digital logic probes, waveform generators, analog frequency meters , tachometers, temperature measurement and control devices, voltage regulators etc.
- The timer IC works in three modes – i) one-shot or monostable ii) or as a free-running or Astable multivibrator iii) and can be used as Schmitt trigger

MAIN FEATURES OF IC 555:

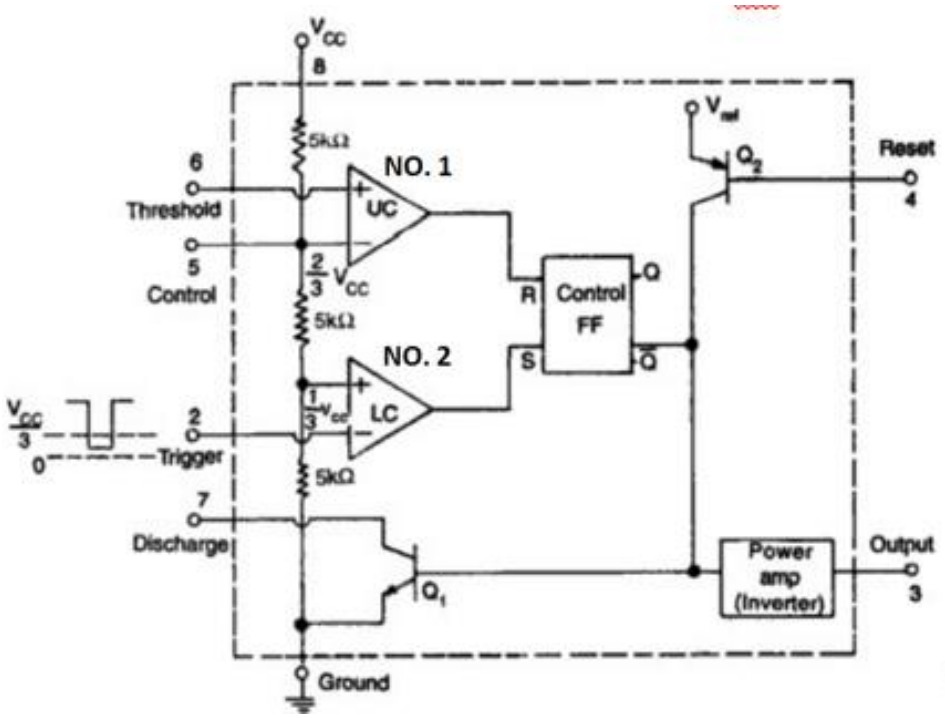
- 1. It operates from + 5 Volts to + 18 Volts supply voltage.
- 2. Sink or source 200 mA of load current.
- 3. Timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilohertz.
- 4. The output drives a transistor-transistor logic (TTL) due to its high current output.
- 5. It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005 %/ °C.
- 6. The duty cycle of the timer is adjustable.
- 7. Maximum power dissipation per package is 600 mW
- 8. Its trigger and reset inputs has logic compatibility.

- PIN DIAGRAM OF IC 555



The following devices are used in IC 555

- 1. Comparators-2 Nos
- 2, Flipflop -1
- 3.Resistors
- 4. Transistors
- The 555 Timer contains a voltage divider network, two comparators, one SR flip-flop, two transistors and an inverter.



A. VOLTAGE DIVIDER NETWORK:

- The voltage divider network consists of a three 5KΩ resistors that are connected in series between the supply voltage Vcc and ground. This network provides a reference voltage of 1/3 Vcc to Lower comparator and 2/3 Vcc to Upper comparator

B. COMPARATORS:

- 555 Timer IC consists of two comparators: an Upper Comparator (UC) No.1 and a Lower Comparator (LC) No.2
- If the voltage present at the non-inverting terminal of an op-amp is greater than the voltage present at its inverting terminal, then the output of comparator will be +Vsat. This can be considered as Logic High ('1') in digital representation.
- If the voltage present at the non-inverting terminal of op-amp is less than or equal to the voltage at its inverting terminal, then the output of comparator will be −Vsat. This can be considered as Logic Low ('0') in digital representation

C. SR FLIP-FLOP

R	S	Q-	Q
0	0	Previous	state
0	1	0	1
1	0	1	0
1	1	X	X

- Q(-) & Q are previous state & present state respectively. SR flip-flop can be used for one of these three functions such as Hold, Set & Reset based on the input conditions, when positive transition of clock signal is applied.
- The outputs of Lower Comparator (LC) and Upper Comparator (UC) are applied as inputs of SR flip-flop

D. TRANSISTORS:

- Timer 555 IC consists of one NPN transistor Q1 and one PNP transistor Q2.
- Q1 is a NPN transistor and will be turned ON if its base to emitter voltage is positive and greater than cut-in voltage. Otherwise, it will be turned-OFF.
- Q2 is a PNP transistor and used as buffer in order to isolate the Reset input from SR flip-flop and connected to NPN transistor Q1.

E. INVERTER:

- The inverter used, not only performs the inverting action but also amplifies the power level.

MAIN FUNCTION OF IC 555

- The 555 Timer IC can be used in mono stable operation in order to produce a pulse at the output. Similarly, it can be used in Astable operation in order to produce a square wave at the output. It can also be used in Schmitt trigger operation.

Pin		I/O	DESCRIPTION
NO.	NAME		
1	GND	O	Ground Reference Voltage
2	Trigger	I	Responsible for transition of SR flip-flop
3	Output	O	Output driven waveform
4	Reset	I	A negative pulse on reset will disable or reset the timer
5	Control Voltage	I	Controls the width of the output pulse by controlling the threshold and trigger levels
6	Threshold	I	Compares the voltage applied at the terminal with a reference voltage of 2/3
7	Discharge	I	Connected to open collector of a transistor which discharges a capacitor between intervals.
8	V_{CC} Supply	I	Supply voltage

PIN NO. 1: GROUND

- This pin is used to provide a zero voltage rail to the Integrated circuit. All the voltages are measured with respect to this terminal.

PIN NO.2 : TRIGGER

- It is responsible for SET transition of the flip-flop. With this the timing pulse starts. The non-inverting terminal of the second comparator is connected to the **1/3 Vcc** point . So if we decrease the voltage of the trigger pin below the **1/3 Vcc** then the output of the comparator will be **HIGH** (Set) and the FF is SET. Q =1 and $\overline{Q}$ = 0 (LOW)
- This trigger is an active low trigger.
- The output at the **pin 3** goes **HIGH** when the 555 timer is triggered through **pin 2**

PIN NO.3 : OUTPUT

- The pin 3 is an output pin and the output is digital in nature. The output may be low or high. If the output is low, then the value is close to 0 V. If the output is high, then the value is close to +5V. The output pin is connected to load. The IC can deliver up to 200mA of current through this pin. Load can be connected to pin No.3. The other end of load may be connected to ground or to Vcc

PIN NO.4 : RESET

- The pin no.4 is used to reset the flip-flop circuit. The negative pulse is applied to this pin to disable or reset. If not used it is connected to Vcc to avoid false triggering due to noise. This provides a mechanism to reset the FF . This overrides the effect of any instruction coming from Lower comparator

PIN NO.5 CONTROL VOLTAGE:

- This is directly connected to the inverting terminal of the first comparator. 2/3 Vcc is internally connected at this pin. Through this pin external voltage is connected if required
- This pin controls the timing of the 555 by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.

PIN NO.6 THRESHOLD VOLTAGE:

- As the inverting terminal of the first comparator is connected to the 2/3 Vcc point so when the voltage of the non-inverting terminal is greater than 2/3 Vcc, the output of the first comparator will be high. This resets the R-S flipflop
- The pin no.2 (Trigger) and pin no.6 (Threshold) are used to control the output of the comparators.

PIN NO. 7: DISCHARGE:

- The discharge pin is connected directly to the Collector of an internal NPN transistor Q1 which is used to "discharge" the timing capacitor to ground.
- In stable condition $(\bar{Q})$ of FF is HIGH. Base of Q1 is connected to $(\bar{Q})$ of FF. Q1 conducts and the pin no.7 shorts to ground. So capacitor is grounded.
- Output (pin 3) is LOW since $(\bar{Q})$ of FF is inverted in Power amp
- When the FF is set , $(\bar{Q})$ becomes LOW. Transistor Q1 is cutoff. The short across the capacitor is removed. C starts charging through R.
- Since $(\bar{Q})$ is low, the output at pin No. 3 becomes HIGH

PIN NO. 8 : +Vcc.

- Supply voltage +5 V to + 18 V can be applied

IC TIMER 555 FUNCTIONAL MODES

HOW IC 555 FUNCTION:

- In the stand by (stable) state, $\bar{Q}$ of the FF is High. This makes the output low because the power amplifier is an inverter
- There are 3 operational modes

1. FF SET CONDITION:

- A negative going trigger pulse is applied to trigger pin 2. its DC level should be less than $\frac{Vcc}{3}$. As the negative going edge becomes less than $\frac{Vcc}{3}$ the out put of

comparator 2 (lower) goes HIGH. This sets the FF Q =1 and $\overline{Q} = 0$
The output pin 3 becomes 1

2. FF RESET CONDITION:

If at Threshold point 6 the voltage passes above $\frac{2}{3}\ Vcc$

the output of Comparator (Upper) goes to HIGH. This resets FF Q=0 and $\overline{Q}$ =1
The output pin 3 becomes 0

3. IC IN NON FUNCTIONAL MODE: (IC RESET CONDITION)

- When Reset Pin no.4 is grounded or fed with voltage lees than 0.4 V (Low) Q2 conducts and makes $\overline{Q}$ of FF high. Because of this the output at pin no.3 goes to Low. The operation of the IC ceases. Even though Lower comparator goes to HIGH because of trigger, it will not have any effect on FF.
- When Reset pin no.4 is not used , it should be connected to Vcc.

Q 2. What is the importance of pin 5 in IC 555
PIN NO.5 CONTROL VOLTAGE:

- This is directly connected to the inverting terminal of the first comparator. 2/3 Vcc is internally connected at this pin through the resistor potential divider
- This is directly connected to the inverting terminal of the first comparator. 2/3 Vcc is internally connected at this pin through the resistor potential divider

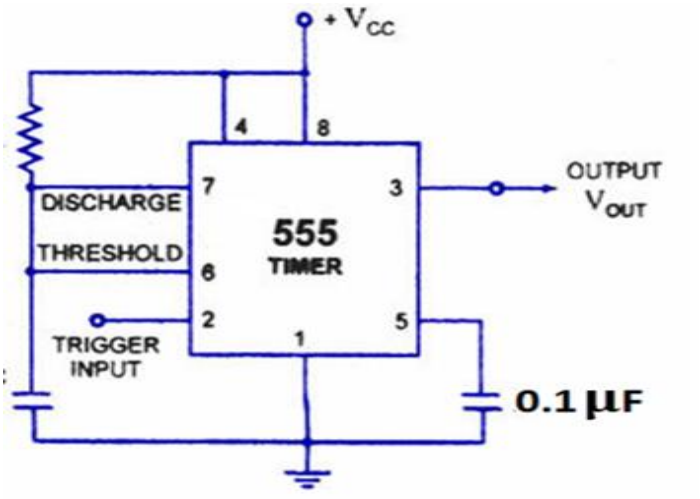
Q 3. What are the modes of operation of IC 555 timer

IC 555 timer is normally used for the 3 operations

- 1. Monostable Operation
- 2. Astable Operation
- 3. Schmitt Trigger Operation

MONOSTABLE USING IC 555

Q4. Explain the operation of Monostable multivibrator using IC 555 and derive the expression for the pulse width

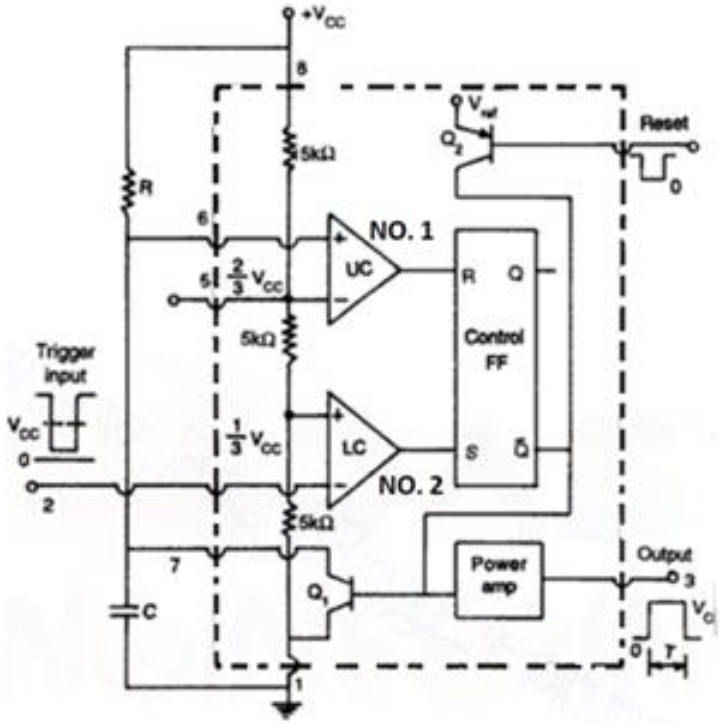


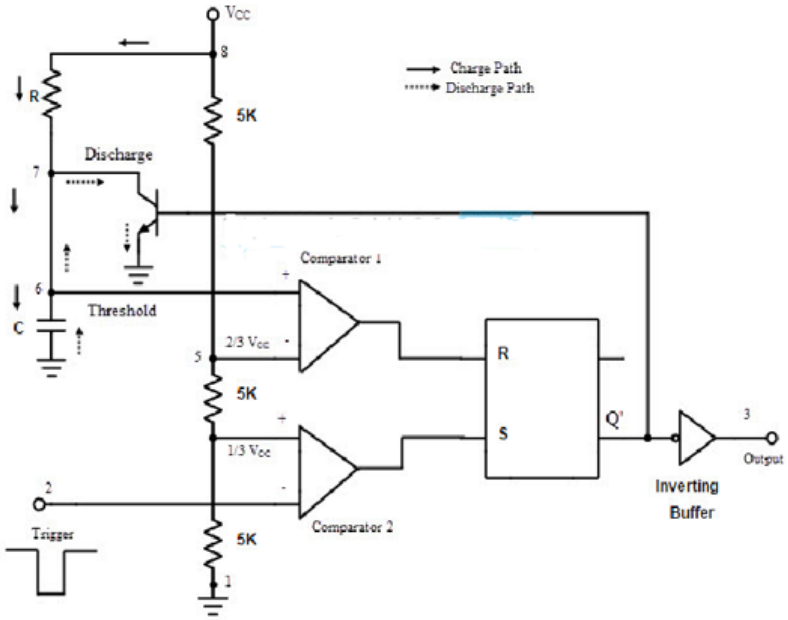
Circuit of The Timer 555 as a Monostable Multivibrator

DESCRIPTION OF MONOSTABLE OPERATION:

i) STANDBY STATE:

- Flip-flop FF Q = low and $\overline{Q} = 1$. So transistor Q1 is ON. This clamps the external capacitor and connects it to ground. Capacitor is now in discharged mode.
- Since $\overline{Q} = 1$ is connected to Power amp which is an Inverter, output at pin no. 3 is LOW.

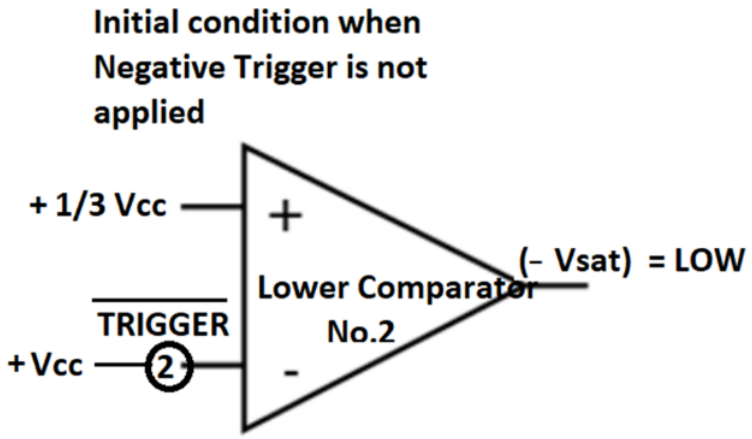


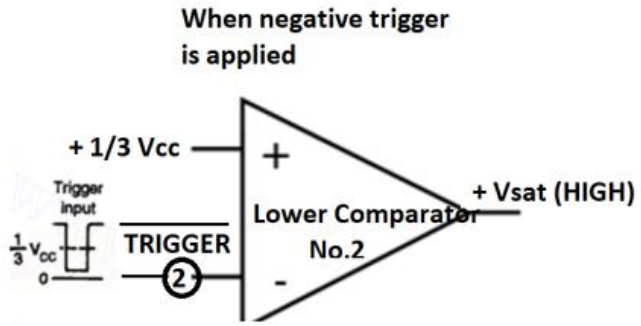


ii) TRIGGER MODE OR "SET STATE" OF FF

- Now negative trigger is applied to pin no.2 ($\overline{TRIGGER}$) . As the trigger voltage passes through $\frac{Vcc}{3}$ and become less than $\frac{Vcc}{3}$ the Lower comparator (No.2) changes state and goes to HIGH state from Low.

LOWER COMPARATOR BEFORE TRIGGER AND AFTER TRIGGER:





- The HIGH output edge from Lower Comparator is applied as SET trigger to Flip-flop.Now the IC is set. Q = High and $\overline{Q}$ = LOW. This signal gets inverted in the Power Amplifier block. The Output appears at pin No.3 and it is HIGH.. However since the trigger goes back to Vcc after a short duration, the comparator output again go back to LOW. This will not bring in any changes in FF outputs
- $\overline{Q}$ = LOW. signal goes to base of Transistor Q1 and makes it OFF (transistor switch opens). This removes the short across the Capacitor. Since Capacitor is unclamped, voltage across it rises exponentially through resistance R

3. RESET STATE OF FF:

- The rise in capacitor voltage is exponential with a time constant of RC.
  Upper comparator No.1, Inverting input is connected to a fixed voltage +2/3 Vcc. So the Comparator is at (–Vsat) LOW
- After a time period T the voltage across Capacitor reaches 2/3 Vcc and starts rising above 2/3 Vcc. This rising voltage is connected to Non inverting input of the comparator. The instant this becomes more than 2/3 Vcc, the comparator output becomes(+ Vsat) HIGH. This is applied to the RESET terminal of FLIP-FLOP.
- FF now will be reset and Q= LOW and $\overline{Q}$ = HIGH . Since $\overline{Q}$ is connected to Output pin No.3 through an inverter, the output pin becomes LOW.
- $\overline{Q}$ (HIGH) is also connected to base of Transistor Q1 and the Q1 becomes ON. (transistor switch closes). This shorts the capacitor to ground. The cycle repeats with a new trigger pulse.

PULSE WIDTH OF MONOSTABLE :

- The voltage across the Capacitor

$v_c = Vcc\ (1 - e^{-\frac{t}{RC}})$

At $t = T$, $v_c = \frac{2}{3}\ Vcc$

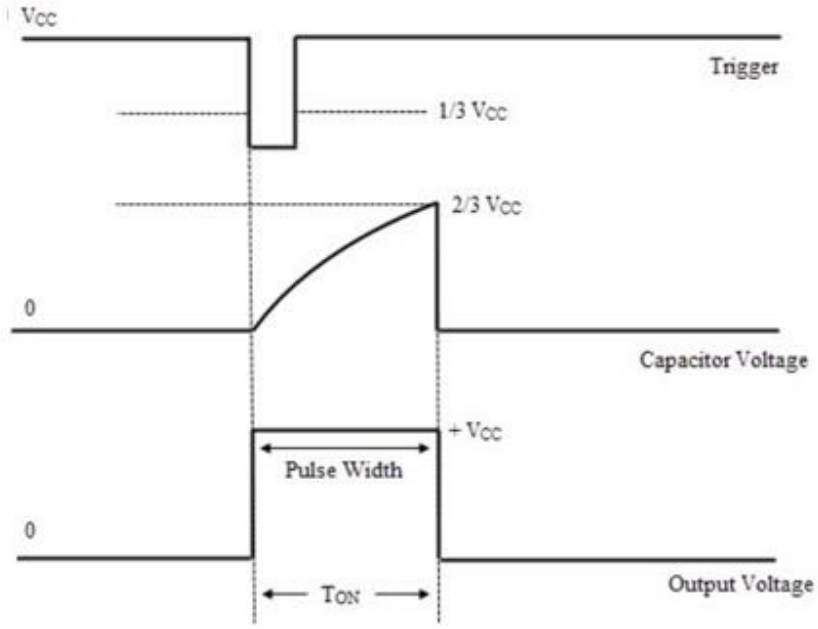
$\therefore\ \frac{2}{3}\ Vcc = Vcc\ (1 - e^{-\frac{T}{RC}})$

$$e^{-\frac{T}{RC}} = (1 - \frac{2}{3}) = (\frac{1}{3})$$

- Taking natural logarithms

$\frac{-T}{RC} = \text{Ln}\ (\frac{1}{3}) = -1.1\ \therefore\ T = 1.1\ R\ C$ secs

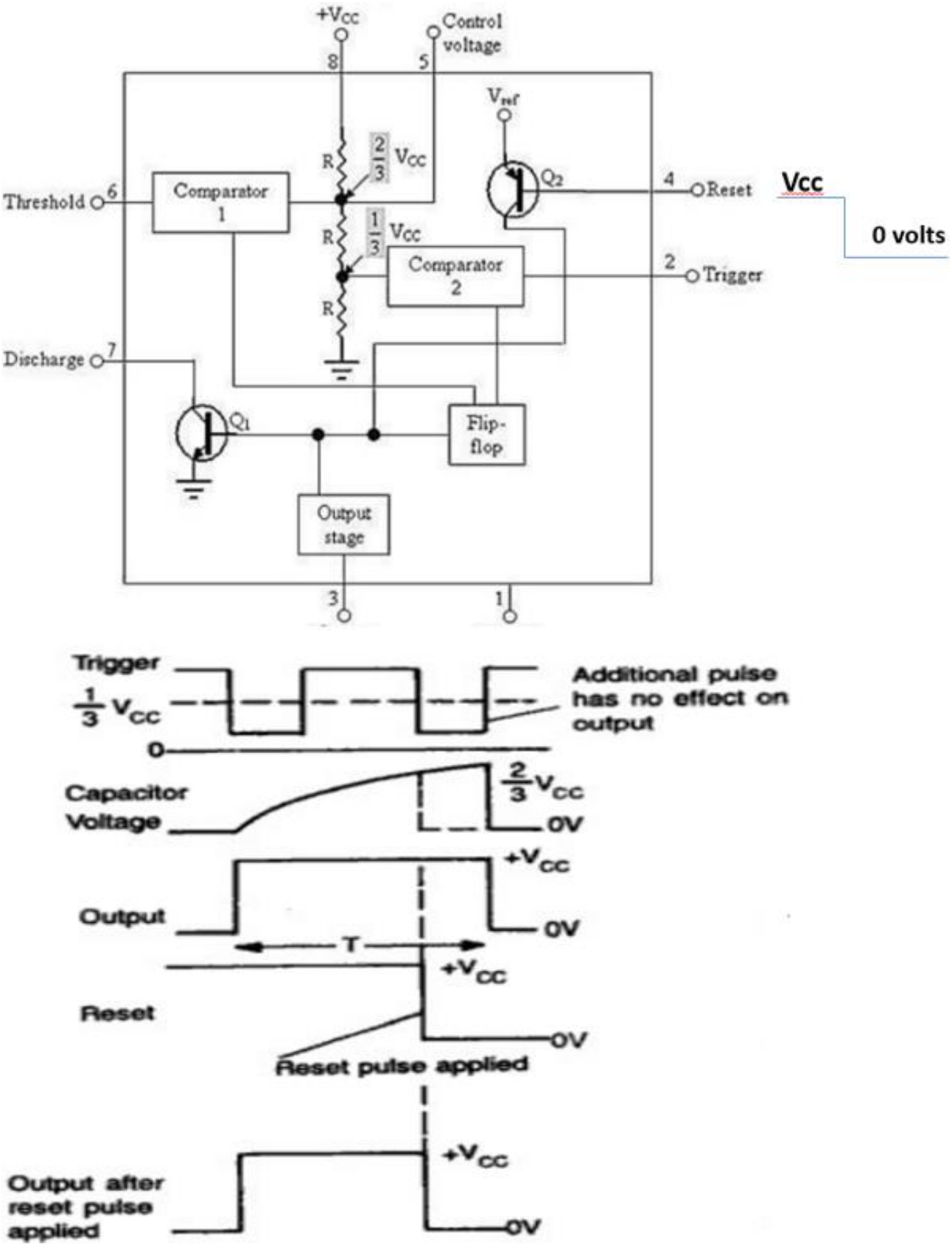
WAVE FORMS OF OUTPUT



Q 5. What is the importance of pin 4 in IC 555

ROLE OF PIN NO. 4:

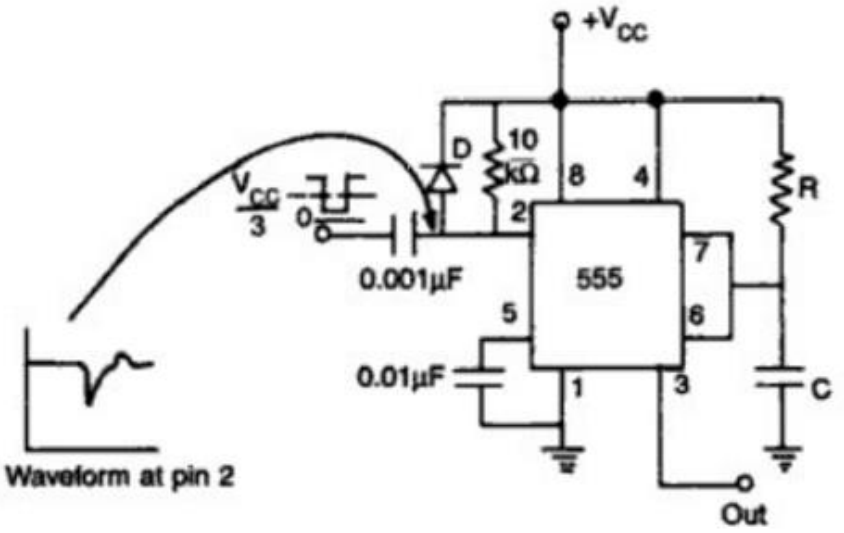
- From the formula just derived , it is noted that
- i) timing interval is independent of the supply voltage
- ii) once triggered, the output remains in HIGH state until the time T elapses , and T only depends on only R and C . Any additional trigger at pin No. 2 ($\overline{TRIGGER}$) will not change the output state.
- iii) However if a negative going Reset pulse is applied to pin no.4 during the timing pulse, Q2 becomes ON. Q2 collector becomes HIGH . Output of Q2 is connected directly to the input of Q1 so as to turn on Q1 Capacitor C is shorted to ground. Its voltage is not allowed to reach 2/3 Vcc.
- iv) Since transistor Q2 collector is connected to input of Inverter power amplifier the output pin 3 goes to LOW



MODIFIED MONOSTABLE:

- To avoid occasional miss-trigger on positive pulse edges a modified circuit is shown below.
- A differentiator circuit is used with a resistor and capacitor combination. R= 10 KΩ and C = 0.001 µF

- The positive spike generated by the differentiator is limited by the forward biased diode to 0.7 V



PROBLEM 1. Design a monostable Multivibrator using 555 timer to produce a pulse width of 100 ms

- Let R = 100 K Ω
- T = 1.1 R C; **C** = $\frac{T}{(1.1)R}$ = $\frac{(100)(10^{-3})}{(1.1)(100)(10^{3})}$ = **0.9 μ F**

OR

- **Let C = 1 μF**
- **R** = $\frac{T}{(1.1)C}$ = $\frac{(100)(10^{-3})}{(1.1)(1)(10^{-6})}$ = **99.1 *KΩ***

APPLICATIONS OF MONOSTABLE

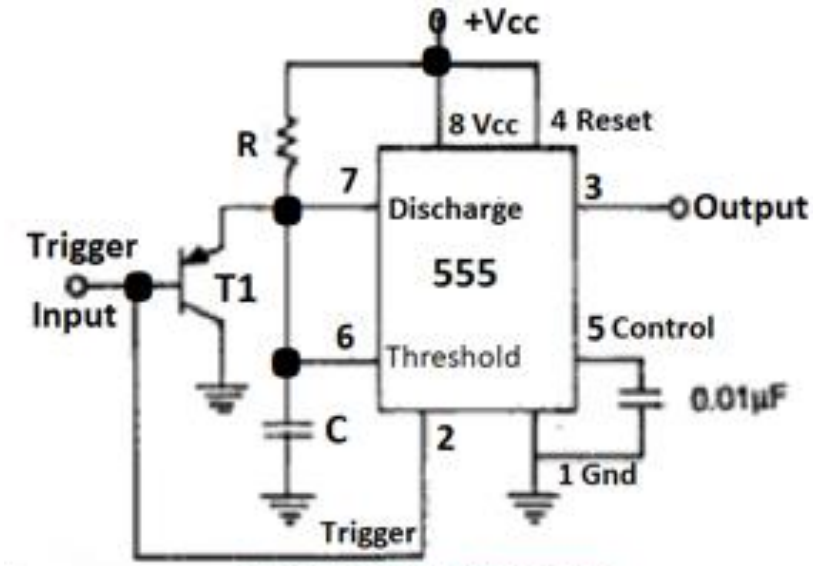
Q 6. List the applications of monostable multivibrator using 555

IC 555 APPLICATIONS IN MONOSTABLE MODE:

- 1. Missing pulse detector
- 2. PWM: Pulse Width Modulator
- 3. Frequency Divider
- 4. Linear Ramp generator

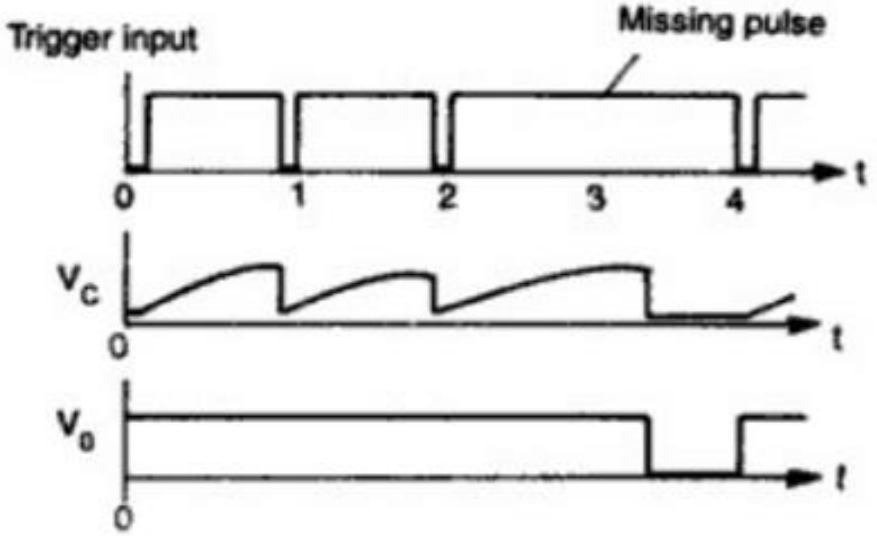
1. MISSING PULSE DETECTOR:

- Timer IC can detect a missing pulse or abnormally long period between two consecutive pulses in a train of pulses.
- Such circuits can be used to monitor the heart-beat of a sick patient, or to detect the intermittent firing of the spark plug of an automobile
- The signal from the pick-up transducer is shaped to form a negative going pulse and is applied to pin 2 of the IC which is connected as a Mono stable. Same signal also is connected to base of transistor T1



MISSING PULSE DETECTOR

- As long as the spacing between the triggering pulses is less than the timing interval the timing cycle is continuously SET by the input trigger pulses and the capacitor is not allowed to reach 2/3 Vcc and is discharged via transistor T1. A missing pulse permits completion of time interval which causes a change in the output level from HIGH to LOW



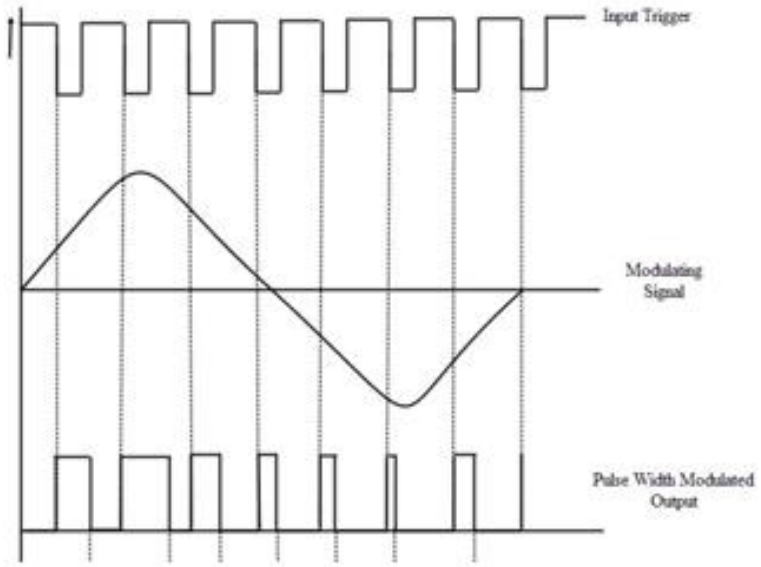
- R and C are chosen such that the timing of pulse width of Monostable is slightly higher (say 20%) than the timing between the trigger pulses
- The continuous negative (low) going pulses of the period whose timing is less than the timing of pulse width, do not allow capacitor C to charge upto 2/3 Vcc. With every trigger pulse the capacitor C is discharged by the Transistor T1. Because of this the output voltage remains HIGH.
- In case there is a missing pulse (pulse 3) Capacitor charges upto 2/3 Vcc and forces output voltage to its LOW state in its normal way. Until the next trigger pulse comes the output voltage remain LOW
- **Example:** If the timing between pulses is 10 msec. Design the R and C values such that the timing pulse width is slightly more than 12 msec (20%)

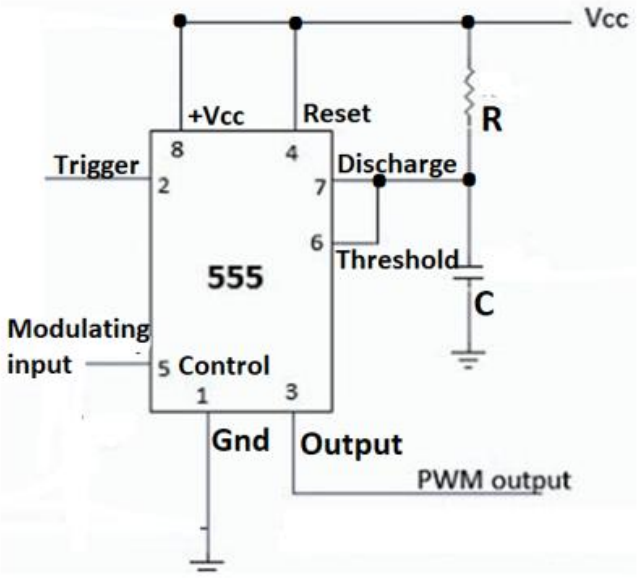
2. PULSE WIDTH MODULATOR: (PWM)

- PWM is widely used for i) motor controlling ii) light controlling
- What is PWM ?
- The output pulse width is proportional to the voltage level of modulating signal

OPERATION OF PWM CIRCUIT:

- Trigger is applied to pin 2 . Whenever trigger pulse goes below 1/3 Vcc , Output at pin goes HIGH. Short across the capacitor C is removed. C starts charging through R .
- Pin 5 which is the control, is connected to the modulating voltage input
- The modulating signal applied at pin 5 gets superimposed upon the already existing 2/3 Vcc at the inverting input terminal of Upper Comparator.





- The time period required to charge the capacitor C upto threshold voltage level changes because of the modulating signal. The pulse width of the output pulse changes as per the voltage level of modulating signal

3. FREQUENCY DIVISION :

- It is a circuit that divides the given frequency by a factor 'n' where 'n' is an integer

$$f_{out} = \frac{f_{in}}{n}$$

- Let us assume the monostable is triggered by the first negative going trigger input (less than 1/3 Vcc). This makes the output (pin 3) go into High state.
- The output remains in this state until 'C' charges to 2/3 Vcc. The output now becomes LOW until a second trigger pulse is applied. This is the normal operation of a monostable
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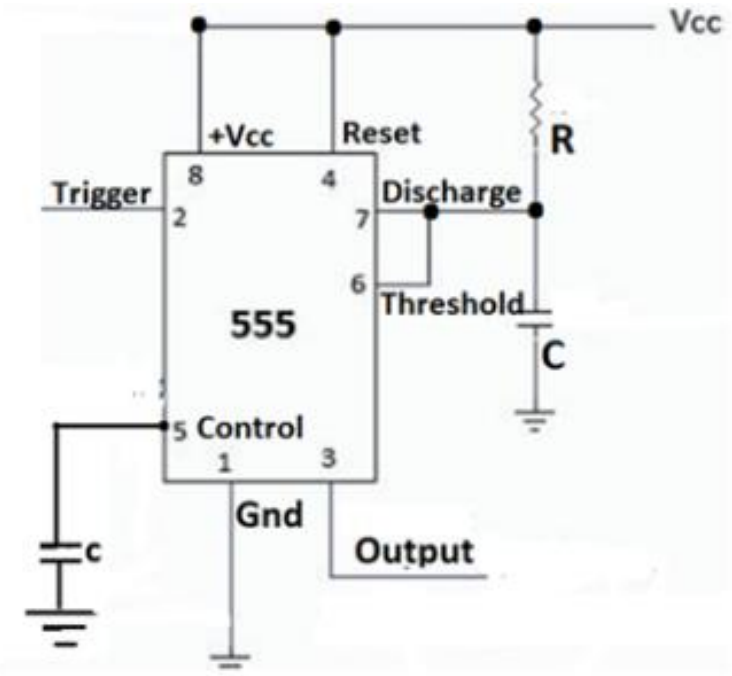

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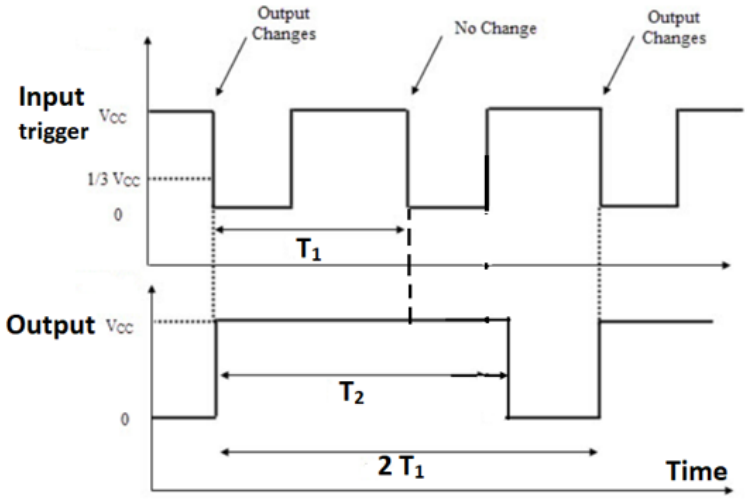
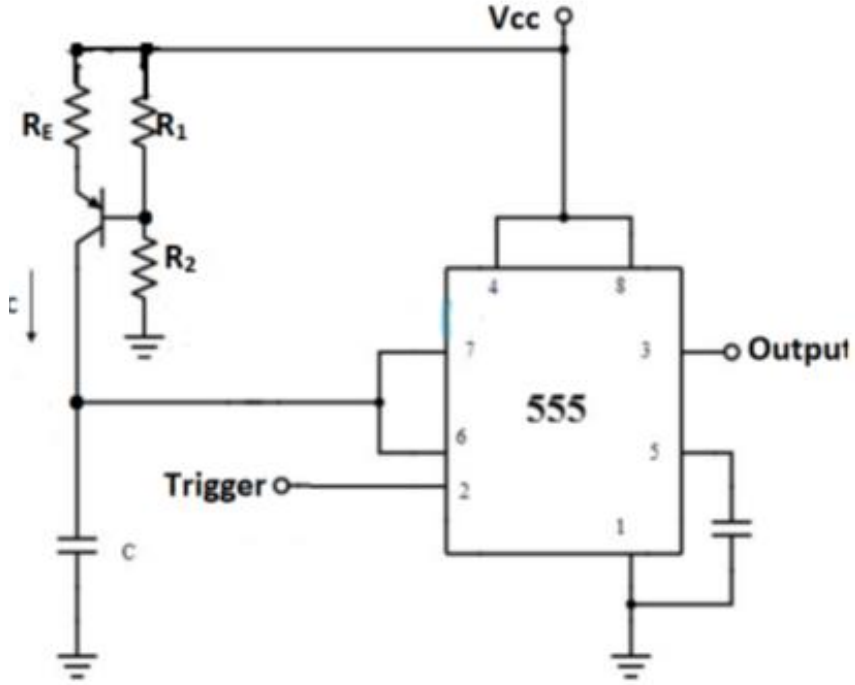


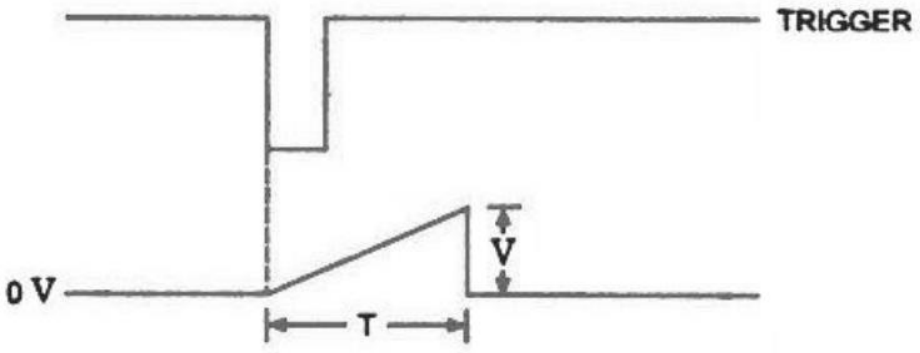
OPERATION FOR DIVISION BY 2:

- However in the Frequency Division configuration, the timing interval (pulse width) of monostable is made slightly more than the period between the input signals (triggers)
- Timing interval (pulse width) T_2 is kept more than the time period T_1 between input pulses (trigger)

- The first negative going input less than 1/3 Vcc generate the SET signal , FF is set and output goes to HIGH
- When the second negative going input (trigger) pulse arrives at pin 2 , the output voltage is still HIGH since 'C' has not crossed 2/3 Vcc. So the second trigger pulse does not have any effect on the output. This way the second input (trigger) fails to affect output
- However output becomes LOW at T_2 time once charge on 'C' crosses 2/3 Vcc. A reset pulse is generated to FF and the FF is reset.
- So the circuit gets triggered on every other pulse of the input (trigger) pulse. There is only one output for every two input (trigger) pulses.

4. LINEAR RAMP GENERATION:





- The resistor R of the monostable is replaced by a constant current source formed by the transistor Q3. The capacitor voltage V_c

- $v_c = \frac{1}{C} \int_0^t i\, dt$ where i = current supplied by the constant current source
- $v_C = \frac{1}{C}\, i\, t$
- Using KVL equations

$$\frac{R_1}{R_1+R_2} V_{CC} - V_{BE} = (\beta + 1)\, I_B\, R_E$$

$$\approx \beta\, I_B\, R_E = I_C\, R_E = i\, R_E$$

- i_B = base current and i_C = collector current

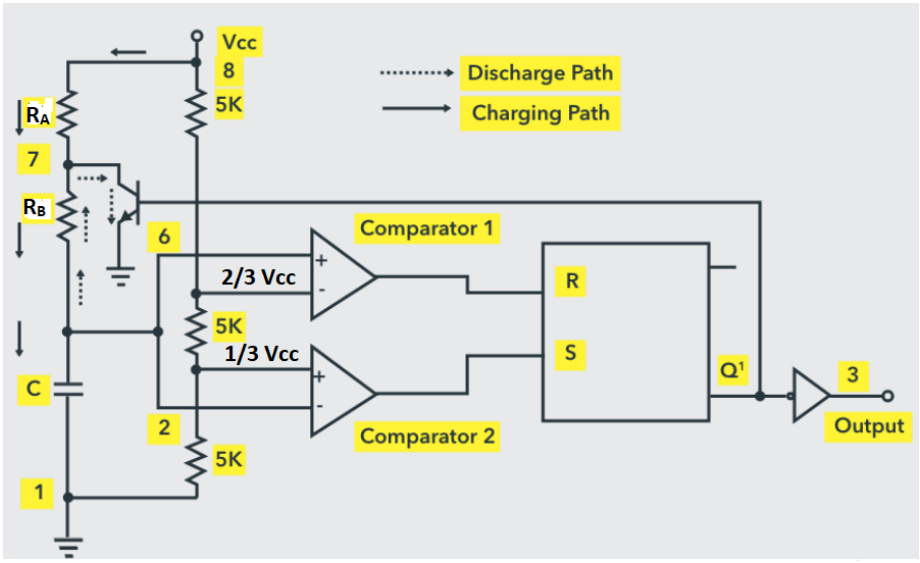
$$i = \frac{R_1\, V_{CC} - V_{BE}\,(R_1+R_2)}{R_E\,(R_1+R_2)}$$

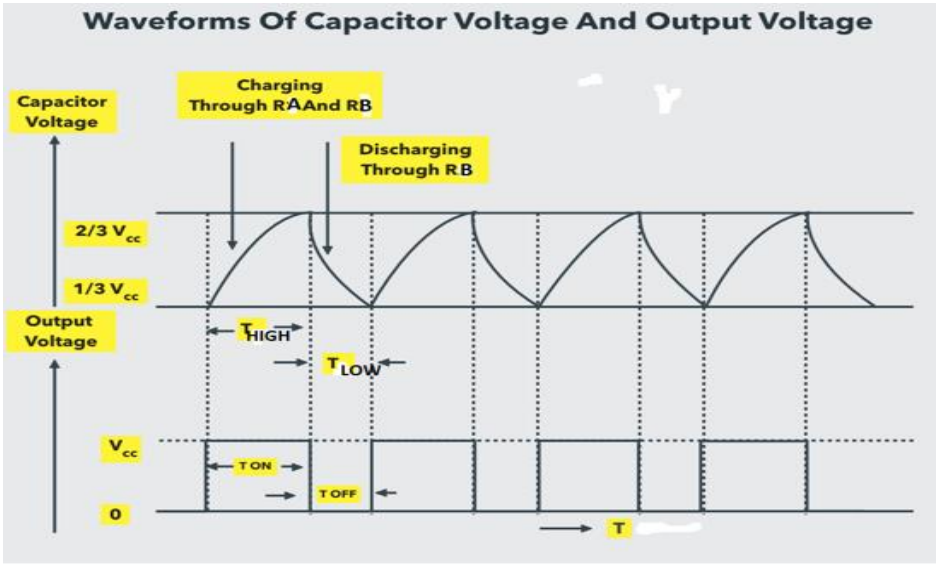
- $v_C = \frac{1}{C}\, i\, t$
- $i = \frac{R_1\, V_{CC} - V_{BE}\,(R_1+R_2)}{R_E\,(R_1+R_2)}$
- $v_C = \frac{1}{C}\, i\, t = \frac{R_1\, V_{CC} - V_{BE}\,(R_1+R_2)}{R_E\,(R_1+R_2)\, C} \times t$
- At time $t = T$, $v_C = 2/3\, V_{CC} = \frac{R_1\, V_{CC} - V_{BE}\,(R_1+R_2)}{R_E\,(R_1+R_2)\, C} \times T$
- $T = \frac{\frac{2}{3} V_{CC}\, R_E\,(R_1+R_2)\, C}{R_1\, V_{CC} - V_{BE}\,(R_1+R_2)}$
- The capacitor discharges as soon as its voltage reaches $2/3\ V_{CC}$. The capacitor voltage will remain as zero until another trigger is applied.

ASTABLE MULTIVIBRATOR

Q 7. Explain the operation of IC 555 in an Astable mode

- In contrast to monostable operation, the timing resistor R is split into Resistors R_A and R_B
- The junction of R_A and R_B is connected to Discharge pin 7
- Transistor Q1 is connected internally (inside IC) to Discharge terminal
- When Vcc is switched on capacitor C is at 0 volts. This is connected to trigger pin 2 and threshold pin 6.
- At this time output of Lower comparator is HIGH. This means S=1 and R=0. the FF is set so $\overline{Q}$ = 0 . The transistor Q1 is OFF. This unclamps 'C'
- Since $\overline{Q}$ = 0 the out put pin 3 is HIGH
- C' starts charging through (RA + RB). The time constant is (RA + RB) C





- C slowly charges to 2/3 Vcc . When the voltage crosses this , upper comparator becomes High. ie R (reset) of FF =1 and $\overline{Q}$ = 1. Transistor Q1 becomes ON (switch is closed) C starts discharging towards ground through R_B . The time constant is R_B C
- Current flows from Vcc through R_A into collector of Q1. So R_A is chosen such that the minimum value of R_A is Vcc / 0.2 (amp)
- C during the discharge reaches 1/3 Vcc and going down. At this point the lower comparator output becomes HIGH. S=1 R=0 and this sets FF. $\overline{Q}$ = 0.
- Transistor unclamps C . C starts charging through (R_A + R_B) towards 2/3 Vcc. Output becomes HIGH. The cycle repeats.

Q 8. Derive the expressions for duty cycle and time period of IC 555 in Astable mode

- C periodically charges and discharges between 2/3 Vcc and 1/3 Vcc
- VC = voltage across capacitor C = $Vcc\ (1 - e^{\frac{-t}{RC}})$
- t1 = time taken for C to charge from 0 to 2/3 Vcc

- $\frac{2}{3} Vcc = Vcc\,(1 - e^{\frac{-t1}{R\,C}})$
- From earlier derivation for mono stable t1 = 1.1 R C
- t2 = time taken for C to charge from 0 to 1/3 Vcc
- $\frac{1}{3} Vcc = Vcc\,(1 - e^{\frac{-t2}{R\,C}})$
- Simplifying in similar lines t2 = 0.405 R C
- t_{HIGH} = time to charge from 1/3 Vcc to 2/3 Vcc = t1 – t2
- t_{HIGH} = (1.1 −0.405) R C = 0.69 R C
- t_{HIGH} = (1.1 −0.405) R C = 0.69 R C
- Here R = $R_A + R_B$
- so t_{HIGH} = 0.69 ($R_A + R_B$) C
- t_{LOW} = time taken to discharge from 2/3 Vcc to 1/3 Vcc
- In a similar way t_{LOW} = 0.69 R_B C
- T = t_{HIGH} + t_{LOW} = 0.69 (R_A + 2 R_B)C
- Frequency = 1 / T = $\frac{1}{0.69}\frac{1}{(R_A+2\,R_B)C}$

Duty cycle = $\frac{t_{HIGH}}{T} \times 100 = \frac{0.69\,(R_A+R_B)\,C}{0.69\,(R_A+2\,R_B)C} = \frac{R_A+R_B}{(R_A+2\,R_B)}$

Q 9. State the applications of IC 555 in Astable mode

APPLICATIONS OF ASTABLE MULTIVIBRATOR:

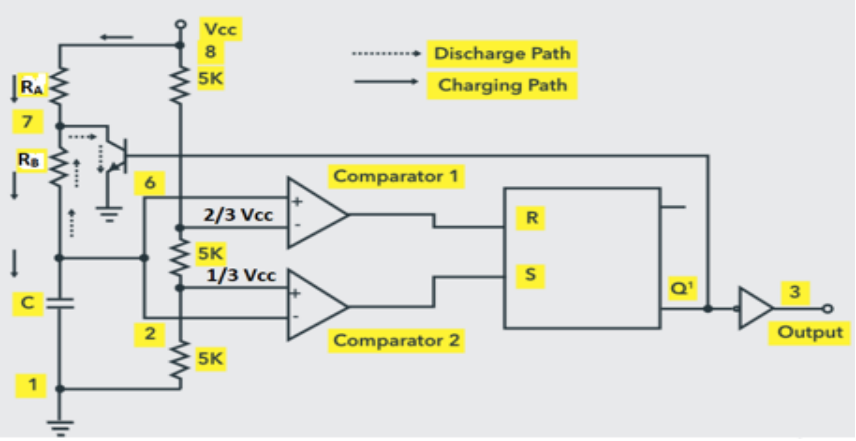
- 1. Square wave generator (50%) duty cycle
- 2. FSK generator
- 3. Voltage Controlled Oscillator

1. SQUARE WAVE 50 % DUTY CYCLE ASTABLE:

- With the circuit diagram shown below

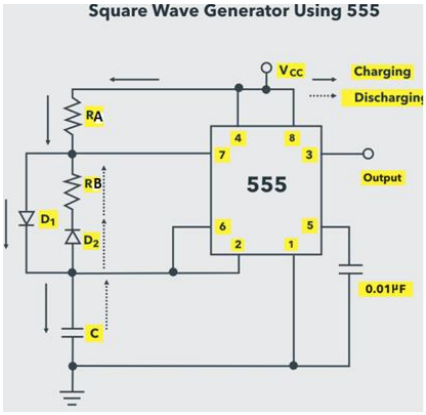
  t_{HIGH} = 0.69 (R_A + R_B) C

  t_{LOW} = 0.69 R_B C
- To make Duty cycle 50% R_A must be reduced Zero
- However since Q1(inside the IC) is connected to pin 7 when R_A =0
- large current flows and Q1 gets damaged. So this method is not feasible.



- During charging portion of the cycle diode D1 is forward biased short circuiting R_B .

  $t_{HIGH} = 0.69\ R_A\ C$
- During discharging portion Q1 (internal) becomes ON and pin 7 is grounded. D1 is reverse biased

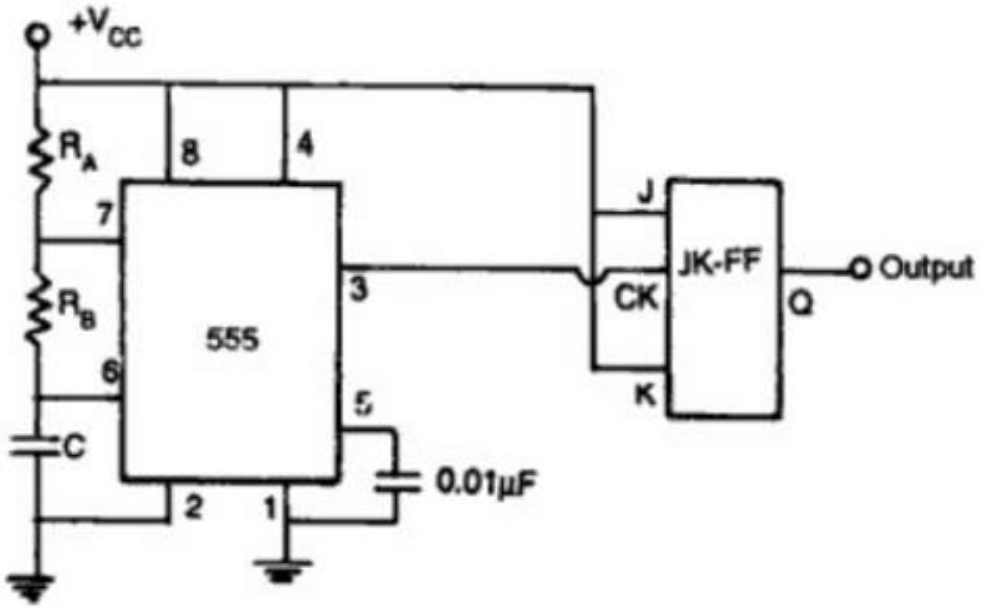


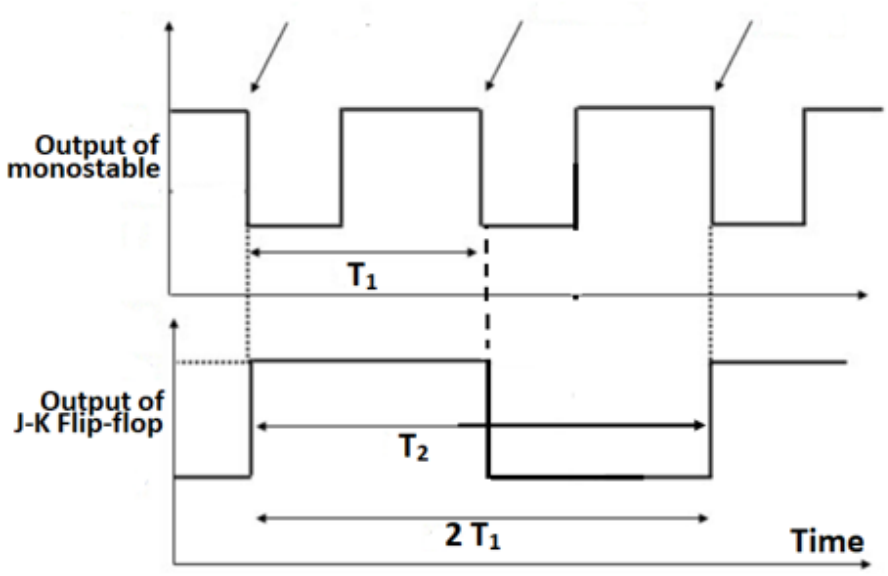
- $T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C$

  $f = \frac{1.45}{(R_A+R_B)\ C}$
- Duty Cycle = $\frac{R_A}{(R_A+R_B)}$
- If $R_A = R_B$ then Duty cycle = 50%

SECOND METHOD :

- Alternatively a clocked flipflop acts as a binary divider to the output. However the frequency will be half that of the timer output



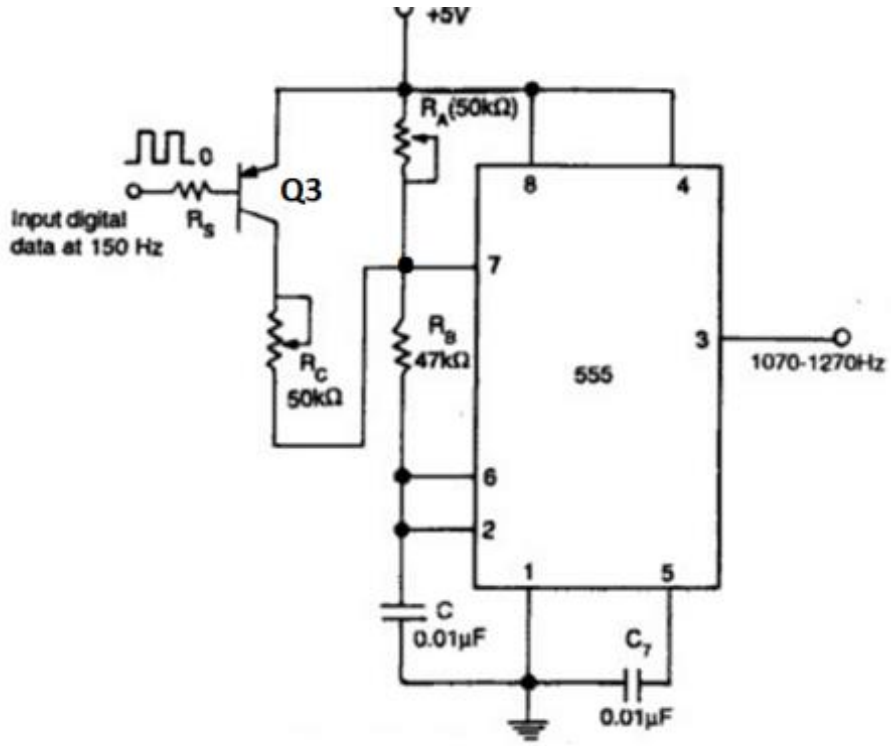


2. FREQUENCY SHIFT KEYING:

- While transmitting digital numbers 0 and 1, Frequency shift keying modulation is used
- For example if '0' is required to be transmitted frequency 'F1' is transmitted, similarly when '1' is required to be transmitted frequency 'F2' is transmitted
- Normal Astable can be used for this purpose
- When input is HIGH transistor Q3 is OFF. Timer works in normal astable mode. The timing of Output wave form
- $T1 = \frac{1.45}{(R_A + 2\,R_B)C}$
- $F1 = \frac{(R_A + 2\,R_B)\,C}{1.45}$
- When input is LOW Transistor Q3 is ON. Resistance R3 is connected in parallel to RA

The timing of Output waveform

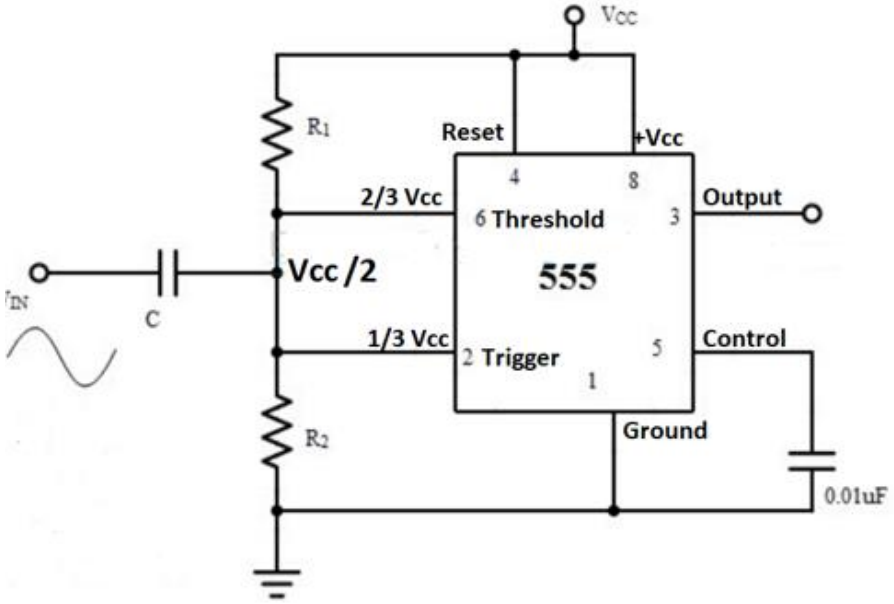
- $T2 = \frac{1.45}{(R_A \,||\, R_C + 2\,R_B)C}$
- $F2 = \frac{(R_A \,||\, R_C + 2\,R_B)\,C}{1.45}$
-



- **PRACTICAL FREQUENCIES FOR FSK:**
- Tele-type-writters use FSK. Standard frequencies are i) 1070 Hz and ii) 1270 Hz

SCHMITT TRIGGER WITH IC 555

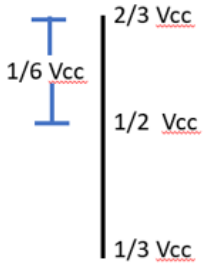
Q 10. Explain how 555 timer can be used as a Schmitt Trigger?

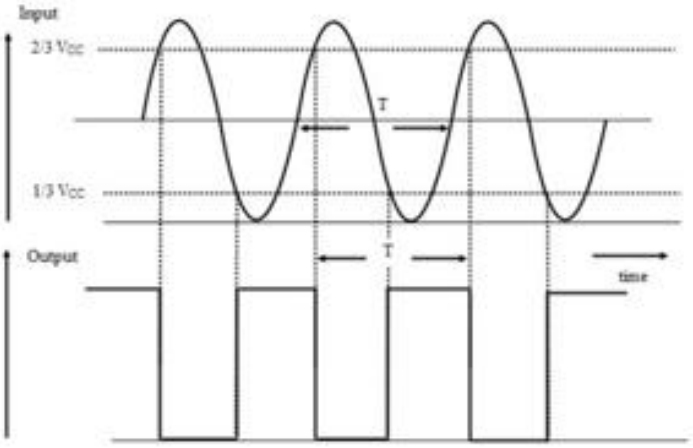


OPERATION OF CIRCUIT:

- Pins 2 and 6 are tied together. Input is given here
- Common point of Pins 2 and 6 is externally biased to get a voltage of Vcc /2 using the potential divider circuit R_1 and R_2 . To get the biasing voltage Vcc /2 , $R_1 = R_2$

- Lower comparator generates a SET signal to the internal FF ,when the input is less than 1/3 Vcc and output goes HIGH
- While Upper comparator generates a RESET signal to the internal FF when the input is greater than 2/3 Vcc and output goes LOW
- As can be seen the value 1/2 Vcc is exactly in between the values 2/3 Vcc and 1/3 Vcc . Ie., 1/3+1/2(2/3− 1/3)=1/2
- The bias provided by R1 and R2 is centered within these two thresholds
- A sine wave of sufficient amplitude greater than 1/6 Vcc 1/6 =(2/3 −1/2) causes internal FF to alternatively SET and RESET providing a square wave output.





Q 11. State the features of IC 555

FEATURES OF IC 555

- 1. IC 555 is a monolithic timer device. It is used to produce accurate and highly stable time delays or oscillations. It can be used to produce time delays ranging from few micro seconds to several hours.
- 2. The Ic 555 is available in i) 8 pin metal can ii) 8 pin mini DIP or 14 pin DIP. IC 556 consists of two 555 Ics
- 3. It has two basic operating modes i) monostable ii) astable . It can also be used in Schmitt Trigger mode
- 4. NE 555 can operate from 4.5 V and 18 V. It can source or sink output current of 200 mAs. CMOS version of IC 555 can operate with supply voltages 2v to 18v
- 5. It has a very high temperature stability and can operate in temperature range of -55^0 C to125^0 C
- 6. Output is compatible with TTL, CMOS, and Op-Amps circuits

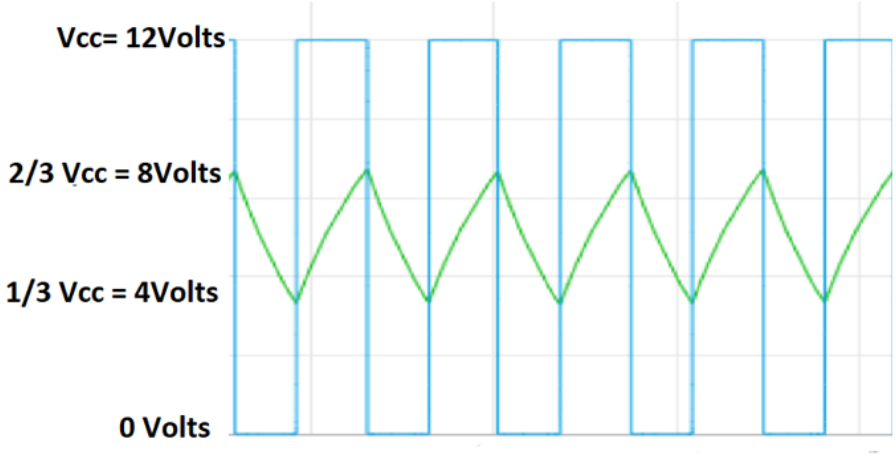
JNTUH EXAMINATION PROBLEMS ON ASTABLE MULTIVIBRATOR

PROBLEM 2. Design the astable multivibrator using 555 for a frequency of 1 Khz and duty cycle of 70% .Use C= 0.1 µF

- f = 1000 Hz , D = 70%
- f = $\frac{1.45}{(R_A+2\,R_B)\,C}$ = 1000 = $\frac{1.45}{(R_A+2\,R_B)\,(0.1)\,(10^{-6})}$
- $R_A + 2\,R_B =$ 14500
- % D = $\frac{R_A+R_B}{R_A+2\,R_B} \times 100 = 70 = \frac{R_A+R_B}{14500}$ so $R_A + R_B$= 10150
- R_A = 10150 −R_B ∴ 10150 −R_B +2 R_B = 14500
- ∴ R_B = 14500−10150 = 4350 Ω
- ∴ R_A = 10150−4350 =5800 Ω

PROBLEM 3. Design a 555 based square wave generator to produce a symmetrical square wave of 1 KHz. If Vcc= 12 V. Draw the voltage across timing capacitor and the output

- For square wave charging and discharging resistors are same
- T = t_{HIGH} + t_{LOW} = 0.69 (R_A +R_B) C
- f= 1000 Hz, T = $\frac{1}{1000}$ = .001sec
- Choose C= 0.1 ×10^{-6}
- $R_A = R_B = \frac{.001}{.69\times.1\times10^{-6}} \times \frac{1}{2} = 7246 \approx 7.3\ K\Omega$



PHASE LOCKED LOOP

Q 11. Write short note on function of Phase Locked Loop

INTRODUCTION:

- The phase locked loop or PLL is a particularly useful circuit that is widely used in radio frequency or wireless applications.

- In view of its usefulness, the phase locked loop or PLL is found in many wireless, radio, and general electronic items from mobile phones to broadcast radios, televisions to Wi-Fi routers, walkie talkie radios to professional communications systems etc.

FUNCTION OF PLL:

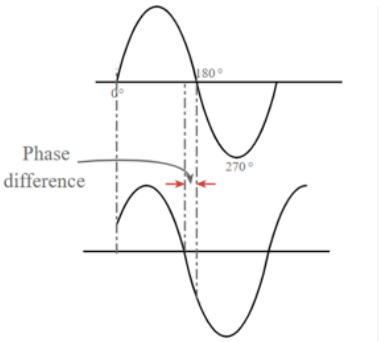
- The phase locked loop take in a signal to which it locks and can then output this signal from its own internal VCO. At first sight this may not appear particularly useful, but with a little ingenuity, it is possible to develop a large number of phase locked loop applications.

BASIC CONCEPT:

- The key to the operation of a phase locked loop, PLL, is the phase difference between two signals, and the ability to detect it. The information about the error in phase or the phase difference between the two signals is then used to control the frequency of the loop.

WHAT IS PHASE DIFFERENCE:

- When there are two signals having different frequencies it is found that the phase difference between the two signals is always varying.



- When there are two signals having exactly the same frequency the phase difference between them is constant. There may be a phase difference between the two signals. If the phase difference is fixed it means that one is lagging behind or leading the other signal by the same amount, i.e. they are on the same frequency

Q 12. What is the Phase locked loop? Briefly explain the roles of low pass filter and VCO in PLL

OR

Draw the block diagram for PLL and explain in detail its operation

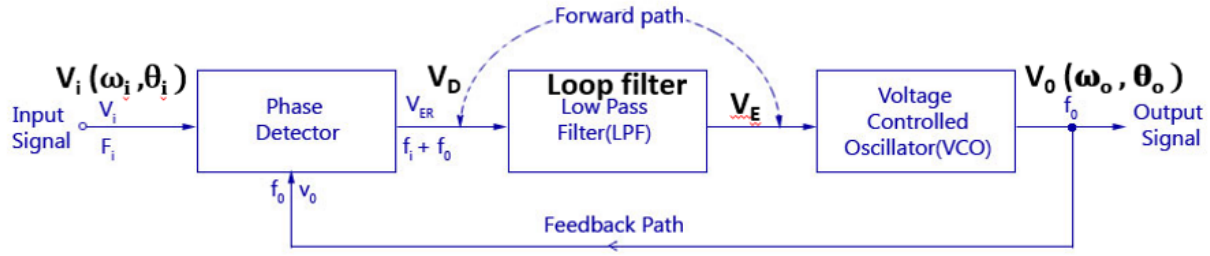
DESCRIPTION OF BLOCK DIAGRAM:

PLL consists of

i) Phase Detector

ii) Loop filter and

iii) VCO Voltage controlled oscillator



1. PHASE DETECTOR

- The phase (difference) detector circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies.
- The phase detector compares the phase θ_i of the incoming signal V_i against the phase θ^0 of the VCO output V_0 and generates a voltage $\mathbf{V_D}$ proportional to the difference $\theta_i - \theta_0$ The phase detector used in PLL may be of analog or digital type.

2. LOOP (LOW PASS) FILTER:

- The output of phase detector is applied to Low pass (loop) filter to remove high frequency ripple and noise from the dc voltage
- The output of Low pass filter without high frequency noise is called as Error voltage VE and this is the control voltage for VCO. The error voltage adjusts the VCO output frequency

3. VOLTAGE CONTROLLED OSCILLATOR:

- VCO is an oscillator whose oscillation frequency is controlled by an external voltage, in this case by the error voltage (control voltage) VE
  which is the output of Low pass filter. The VCO provides a linear relationship between the applied voltage and the oscillation frequency
- Since the control voltage is controlling the frequency of signal this is called Voltage controlled oscillator
- When Control voltage is zero, VCO is in free running mode and its output frequency is called Central frequency ω_{cf} $(2\pi f_{cf})$
- The control voltage V_E shifts the VCO frequency from ω_{cf} to ω_O
  where ω_O is the new VCO output frequency

$$\omega_O = \omega_{cf} + K_O V_E$$

- K_O is the sensitivity (gain coefficient) of the VCO and has the unit radians/second/volt

$$V_E = (\omega_O - \omega_{cf}) / K_O$$

- When a periodic input signal is applied to PLL with frequency ω_i which sufficiently close to the free running frequency ω_C , an error voltage V_E is generated. V_E will adjust ω_O until V_O becomes synchronized with V_i . For every input cycle this adjustment is done. At this instance the PLL is said to be locked on to the incoming signal. Output from VCO has a frequency $\omega_O = \omega_i$
- In locked condition Phase detector generates a constant dc level which is required to shift the free running frequency ω_{cf} to input frequency ω_i

Q 13. Define i) lock in range ii) capture range iii) pull in range

CAPTURE RANGE:

- It is the frequency range $\pm \Delta \omega_C$ centered about ω_O , over which the PLL can acquire lock with an input signal. The capture range is affected by filter characteristics

LOCK RANGE:

- When PLL is in lock, the frequency range $\pm \omega_L$, centered about ω_o , over which the loop can track the input is called Lock range. It is affected by the operating range of the phase detector and the VCO

CAPTURE TIME OR PULL IN TIME :

- The Capture of an input signal does not take place as soon as the signal is applied, but it takes finite time. The total time taken by the PLL to establish a lock is called pull in time

FREE RUNNING FREQUENCY :

- VCO is in free running mode when the control voltage is zero. The output frequency of free running VCO is called center frequency or free running frequency

Q 14. Which parameter decides the pull in time.

- 1. Initial frequency difference between the two signals
- 2. Initial phase difference between the two signals
- 3. Overall loop gain
- 4. Bandwidth of Low pass filter

UNIT 4 CONCLUDED

LINEAR INTEGRATED CIRCUIT APPLICATION
(ECE 404 PC)
UNIT – 5

D –A AND A –D CONVERTERS:

Introduction , basic DAC techniques, Weighted resistor DAC, R –2R Ladder DAC, Inverted R – 2R DAC and IC 1408 DAC, Different types of ADCs –Parallel Comparator type ADC, Counter type ADC, Successive approximation ADC, Dual slope integration type ADC, DAC and ADC specifications

Text books :

1. Linear integrated circuit by D.Roy chowdhary New Age International(P) Ltd
2. Op Amps & linear ICs Ramakanth, A,Gayakwad , PHI

Q 1. What is A/D and D/A converters ?

The circuit that converts analog signal into digital signal is called ANALOG to DIGITAL A/D Converter.

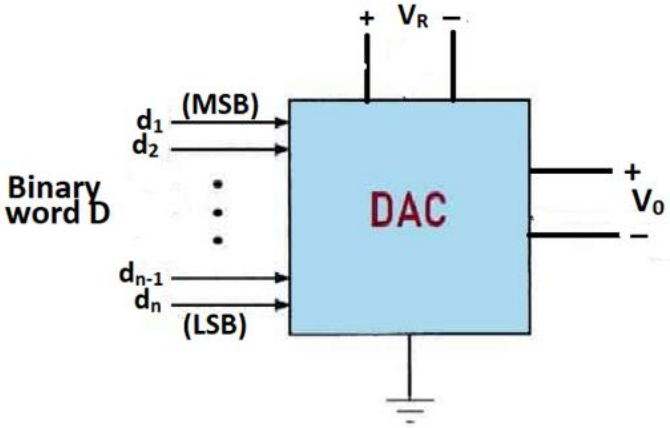
The circuit that converts digital signal into analog signal is called DIGITAL to ANALOG D/A Converter

Q 2. State the types of DAC

1. Weighted resistor DAC
2. R –2 R Ladder
3. Inverted R –2R Ladder

Q 3. Write short notes on DAC

The inputs to DAC are i) a n–bit binary word ‘D’ ii) reference voltage to give the analog signal and output is analog voltage



BINARY WEIGHTED RESISTOR DAC

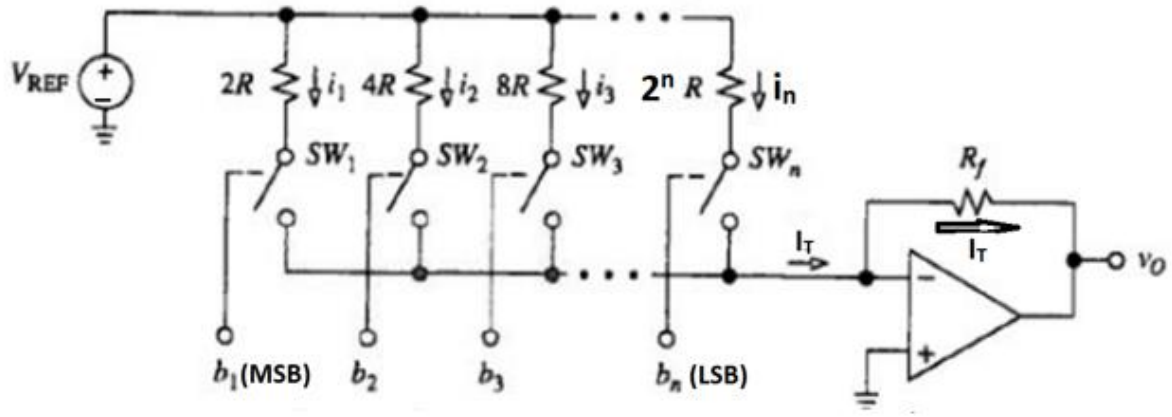
Q 4. Explain the working of weighted BINARY resistor D/A converter

OR

Draw the circuit diagram of weighted resistor digital to analog converter and find the expression of its output analog voltage

OR

Draw a schematic diagram of a D/A converter. Use resistance values whose ratios are multiples of 2. Explain the operation of the converter



BINARY WEIGHTED RESISTOR DAC:

This configuration uses one Op-Amp to sum the binary weighted currents obtained from a Voltage reference V_R . The currents are

I_1 , I_2 , I_3 , ... , I_n . I_1 is MSB 14 is LSB. The current carrying resistors are

2R , 4R, 8R, $\cdots$ 2^n R ie. 2^1 R , 2^2 R , 2^3 R , $\cdots$ 2^n R.

The individual switches connect the resistors 2R, 4R, 8R , to either INVERTING TERMINAL of Op- Amp or connect it ground. The switches are named as

b_1 , b_2 , b_3 , . . . b_n . b_1 is the MSB (Most Significant Bit) and

14 is the LSB (Least Significant Bit)

When switch control to b_1 is logic '1,' b_1 is ON, current $I_1 = \frac{V_R}{2\,R}$

when switch control is logic '0' b_1 is OFF, current $I_1 = 0$

Similarly all the other switches b_2 , b_3 , $\cdots$ b_n operate in the same way

$I_2 = \frac{V_R}{4\,R}$; $I_3 = \frac{V_R}{8\,R}$; $\cdots$ $I_n = \frac{V_R}{2^n\,R}$

All the currents are summed up at the Op-amp –ve input terminal and flows through Feedback resistor RF

The total current $I_T = I_1 + I_2 + I_3 + \cdots I_n$

Output voltage of op-amp $V_0 = -I_T R_F = -(I_1 + I_2 + I_3 + \cdots I_n) R_F$

$$= -\left[b_1 \frac{V_R}{2\,R} + b_2 \frac{V_R}{4\,R} + b_3 \frac{V_R}{8\,R} + \ldots + b_n \frac{V_R}{2^n\,R}\right] R_F$$

Switches $b_1, b_2, b_3, \ldots\ldots b_n$ can be closed or opened by the Logic '1' or Logic '0'

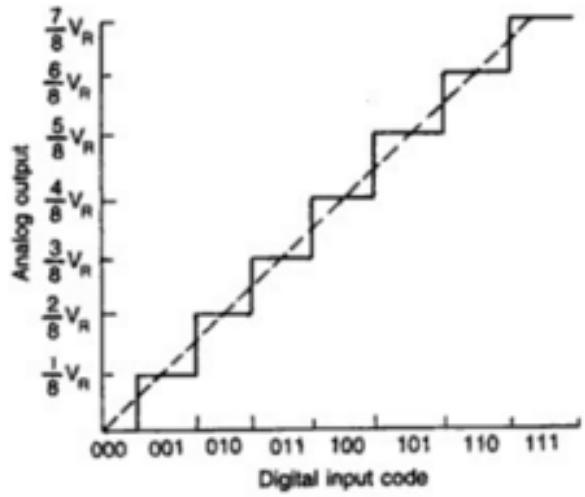
$\therefore V_0 = -\frac{V_R}{R}\left[\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \ldots \frac{b_n}{2^n}\right] R_F$ let $R = R_F$

$$V_0 = -V_R\,[b_1\,2^{-1} + b_2\,2^{-2} + b_3\,2^{-3} + \cdots b_n\,2^{-n}]$$

$$V_0 = -V_R\,[b_1\,2^{-1} + b_2\,2^{-2} + b_3\,2^{-3} + \cdots b_n\,2^{-n}]$$

The above equation shows that the output is analog voltage and is proportional to the input Digital word.

TRANSFER CHARACTERISTICS OF 3 BIT DAC:



Q 5. State the advantages and disadvantages of binary weighted resistor D/A Converter

ADVANTAGES:

The circuit is very simple to realize

DISADVANTAGES:

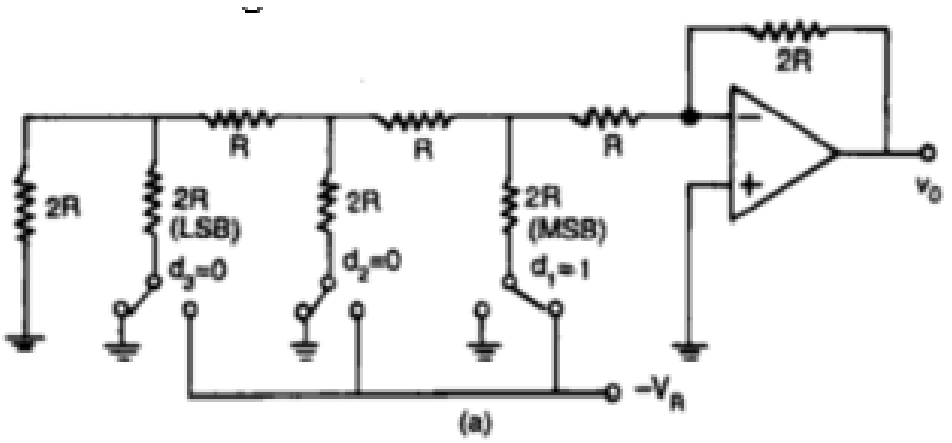
1. The values of resistors required are very wide. For example the circuit requires 2R, 4R, 8R, …….2^n R.
2. If 8 bit DAC is to be built and if R=10K (to minimize loading effect), the largest value of resistor is 2^8 =256 times R ie., 2560K Ω = 2.56 M Ω. To realize such a large resistor in monolithic form will be impracticable
3. The switches have finite resistance. In case of MSB it has the lowest resistance they may form considerable portion of resistance. In case of LSB where highest resistor is used switch resistance may not have much effect. This non linearity affects the accuracy.

R-2R LADDER DAC

Q 6. Draw the circuit diagram of a R-2R ladder type DAC Explain its operation

R-2R Ladder DAC:

It is seen that in the case of Binary weighted resistor type DAC wide range of resistors are required ie from 2R , 4R, 8R,….. 2^n R. To avoid this R -2R ladder type DAC is devised. This requires only two resistors. Practical values range are from 2.5 KΩ to 10 KΩ

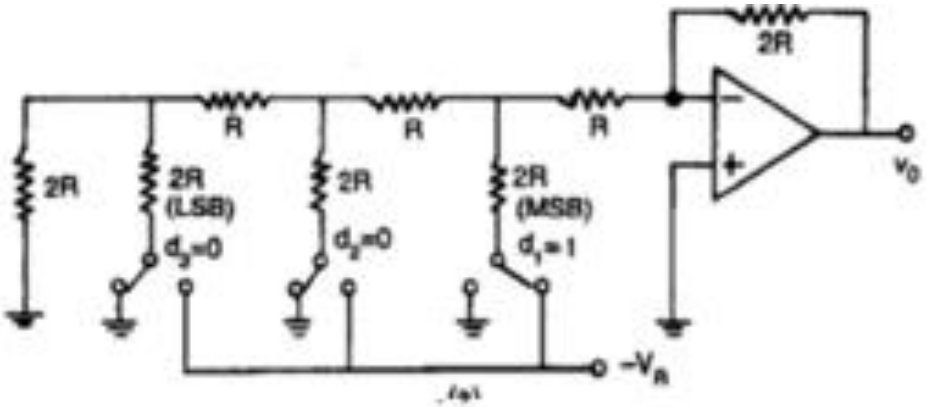


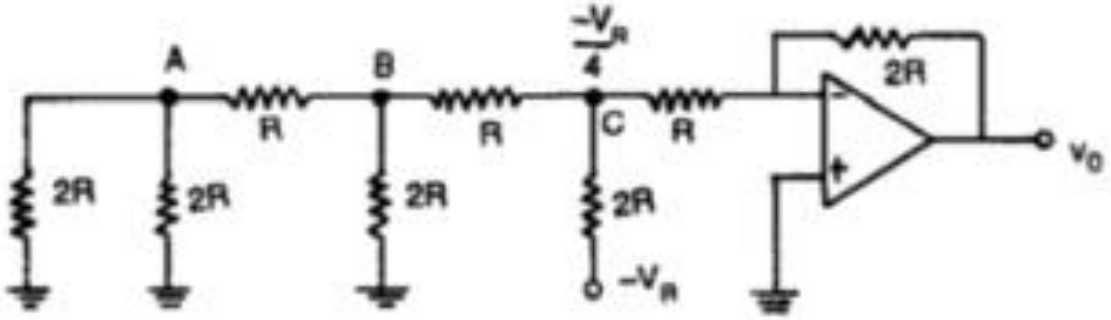
In general the voltage is given by

$$V_0 = V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4} + \ldots\ldots\ldots\ldots + b_n 2^{-n})$$

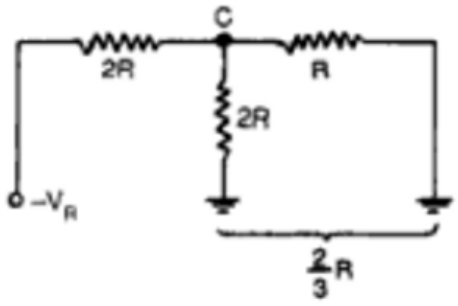
Where b_1 , b_2 , b_3 , b_4 ,……. bn are switch positions and they will be either logic 0 or 1
To confirm the equation belongs to the diagram ,check the above equation with the switch positions 1 0 0 and 0 0 1 for a 3 bit DAC

i) For Switch positions d_1 ,d_2 , d_3 as 1 0 0





$V_0 = V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}) = V_R (b_1 2^{-1}) = V_R (1\times 2^{-1}) = \frac{V_R}{2}$



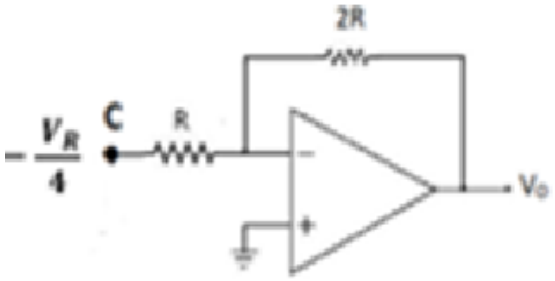
$$\frac{R \times 2R}{R + 2R} = \frac{2}{3} R$$

Voltage at node C =

$$\frac{-V_R \left(\frac{2}{3} R\right)}{2R + \frac{2}{3} R} = -\frac{V_R}{4}$$

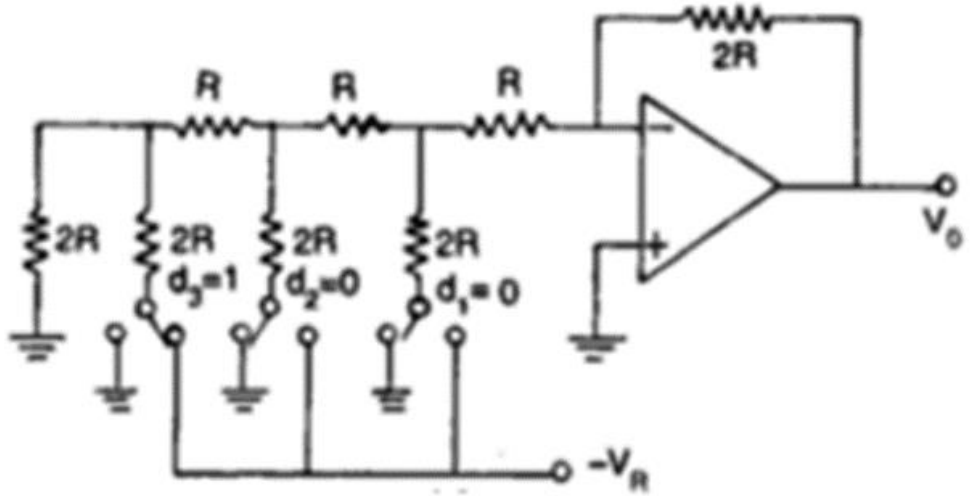
The output voltage

$$V_0 \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2}$$



ii) For switch positions d1 d2 d3 0 0 1

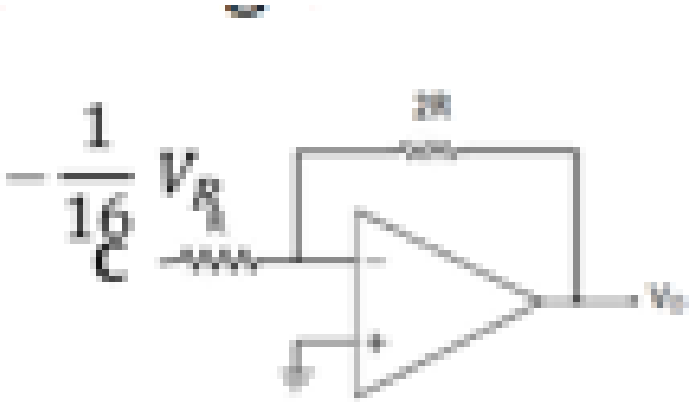
$V_0 = V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}) = V_R (b_3 2^{-3}) = V_R (1\times 2^{-3}) = \frac{V_R}{8}$



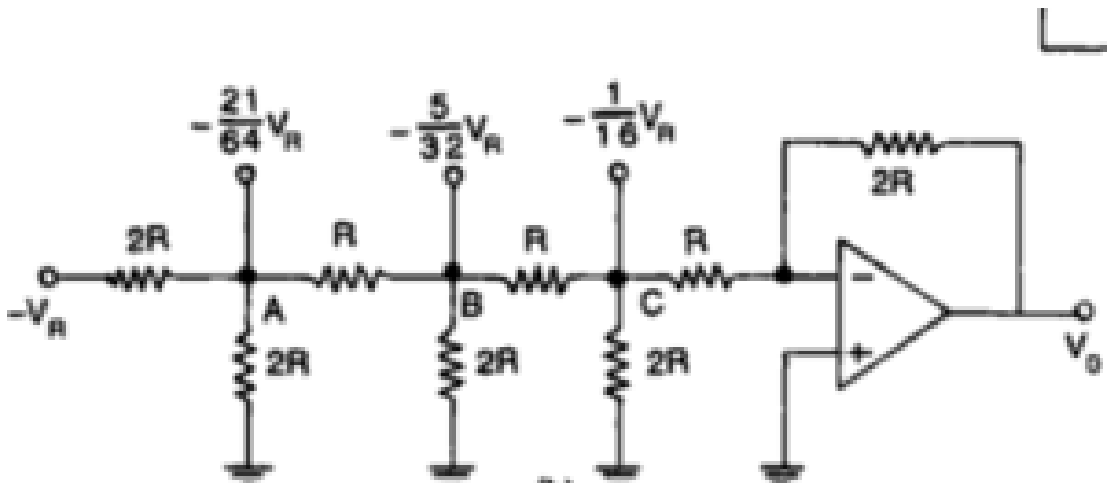
The output voltage =

$$V_0 = -V_R \left(\frac{-1}{16}\right) \frac{2R}{R} = \frac{V_R}{8}$$

∴ The checking with switch positions 1 0 0 and 0 0 1 shows the voltages obtained are as per the equation



So $V_0 = V_R$ ($b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4}$ …….. + $b_n 2^{-n}$) is valid for the diagram
Where b_1 , b_2 , b_3 , b_4 ,……. b_n are switch positions and they will be either logic 0 or 1



INVERTED R-2R LADDER DAC

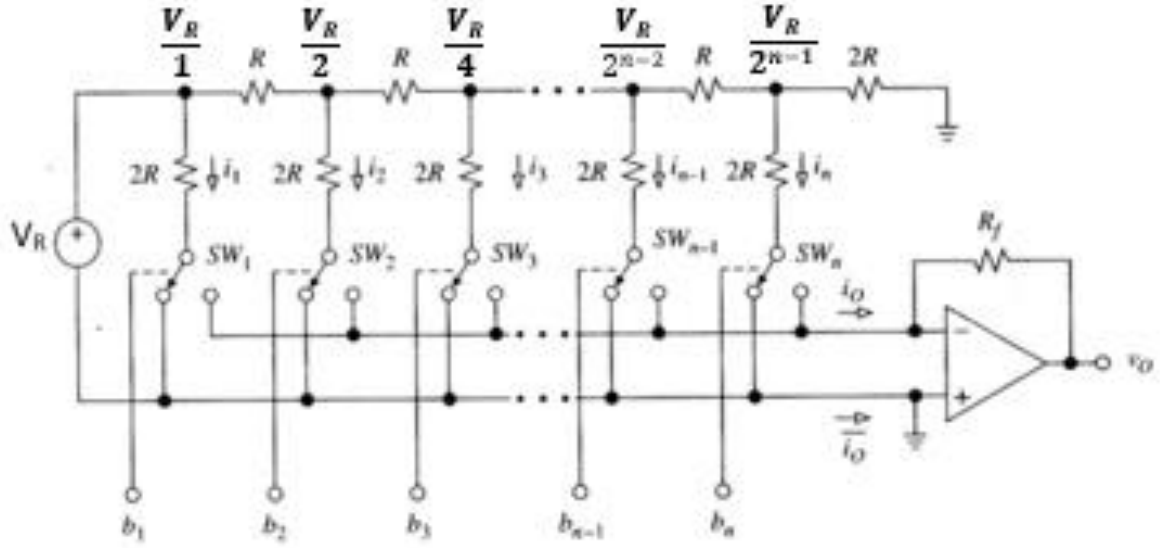
Q 7. Draw the circuit drawing of an Inverted R-2R Ladder type DAC . Explain the operation

Disadvantages of Weighted Resistor type DAC

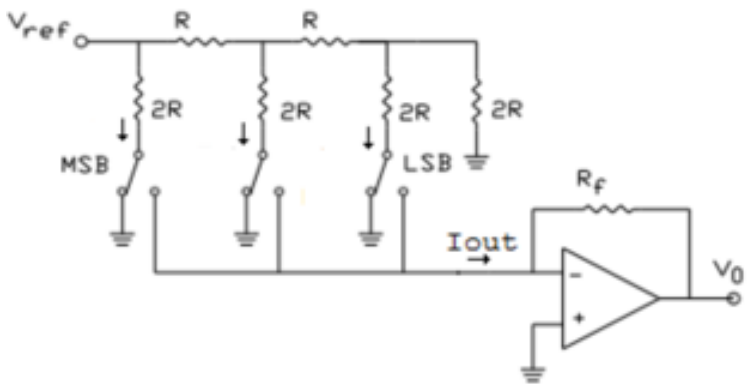
1. As the switches change their position from '0' to '1' or vice versa, current flowing in the resistors changes. This create nonlinearity in DAC.
2. Because of change in currents heating problems crop up.

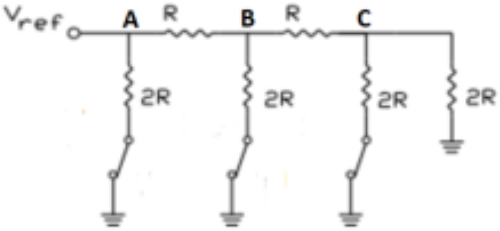
The above serious problems are avoided by using Inverted R-2R Ladder DAC.

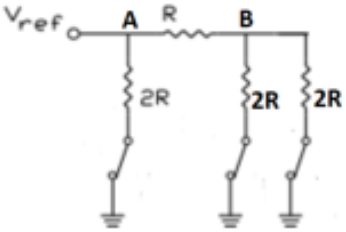
The switches used are either connected to real Ground or to Virtual Ground (because of Op-Amp configuration). So in both positions of switches the current flowing remains constant. The total current is remains same irrespective of the digital word.

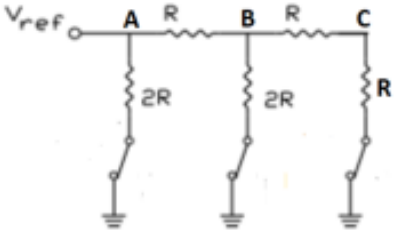


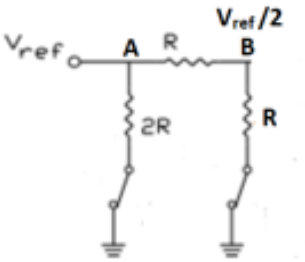
Consider a 3 bit DAC

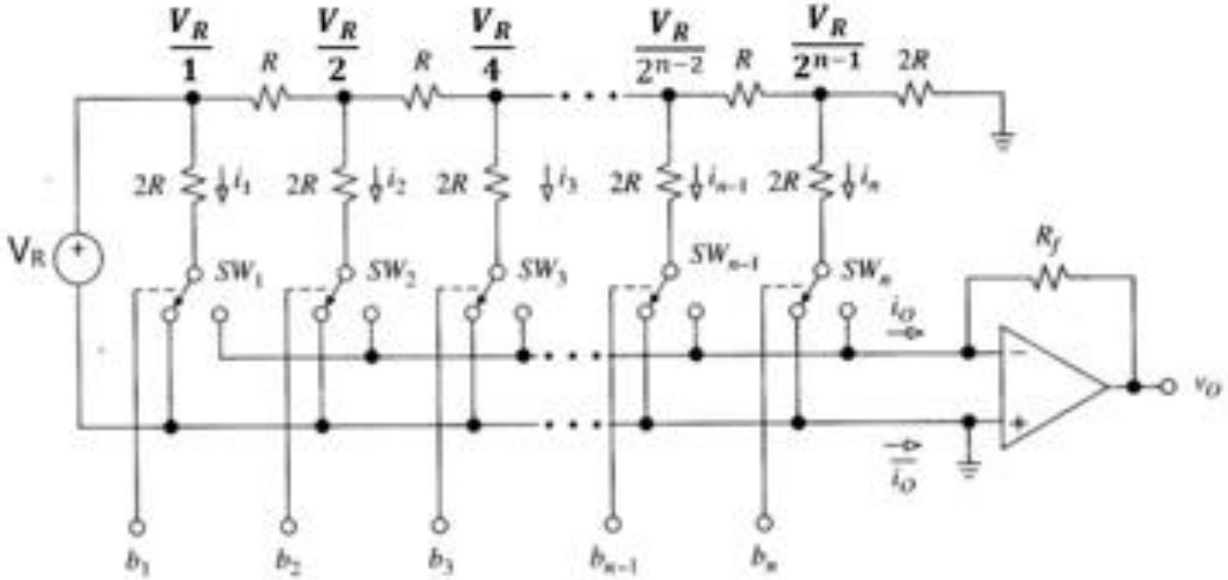








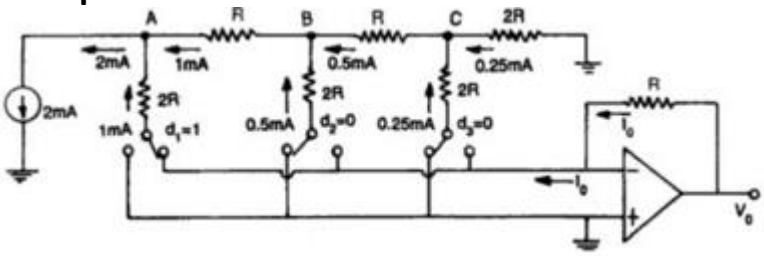




- $i_1 = \frac{V_R}{2R}$
- $i_2 = \frac{V_R}{(2R)(2)} = \frac{V_R}{(4R)} = \frac{i_1}{2}$
- $i_3 = \frac{V_R}{(2R)(4)} = \frac{V_R}{8R} = \frac{i_1}{4}$
- $\mathbf{i_n = \frac{V_R}{(2R)(2^{n-1})} = \frac{i_1}{2^{n-1}}}$
- But $V_o = -I_T \; R_f = -R_f \; (i_1 + i_1 + i_3 + \ldots + i_n)$
- $V_o = -R_f \; (b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \ldots + b_n \frac{V_R}{2^n R})$
- $V_o = -\frac{V_R \; R_f}{R} \; (b_1 2^{-1} + b_2 \; 2^{-2} + b_3 \; 2^{-3} + \ldots + b_n \; 2^{-n})$

The same circuit also can be drawn by taking 2 mA as the current in place of VR

Switch position 1 0 0



2 mA reference input current divides equally to 1 mA at node A.

Right of Node B the equivalent resistance is 2R. So 1 mA further divides to a value of O.5mA at node B

At node C the current divides to 0.25 mA.

Since the circuit works based on summing currents this is also called Current mode DAC

Q 8. What are the specifications of D/A converter

SPECIFICATIONS OF DAC:

1. Accuracy	2. Resolution	3. Offset
4. Linearity error	5. Conversion time	4. Monotonicity

RESOLUTION: It is the number of different analog output values that can be provided by a DAC

Resolution is the smallest change in output voltage which is produced

N bit DAC resolution = 2^n

Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs.

For a N bit DAC it can be given as Resolution = $\frac{V_{OFS}}{2^{n-1}}$

Resolution of a 12 bit DAC is $2^n = 2^{12} = 4096$

ACCURACY : it is defined as the comparison of actual output voltage with expected output voltage. Worst accuracy is $\mp \frac{1}{2} LSB$

MONOTONICITY: DAC is considered as having good monotonicity if it does not miss any step backward when stepped through its entire range of input digital word.

CONVERSION TIME: Time taken by DAC to convert digital signal into digital equivalent

SETTLING TIME: Time required for the output voltage to settle to within ± ½ LSB of the final value for a given digital input

Q 9. State the advantages of R-2R ladder DAC over the binary weighted resistor DAC

OR

Compare and contrast binary weighted resistor type DAC with R- 2R Ladder type DAC

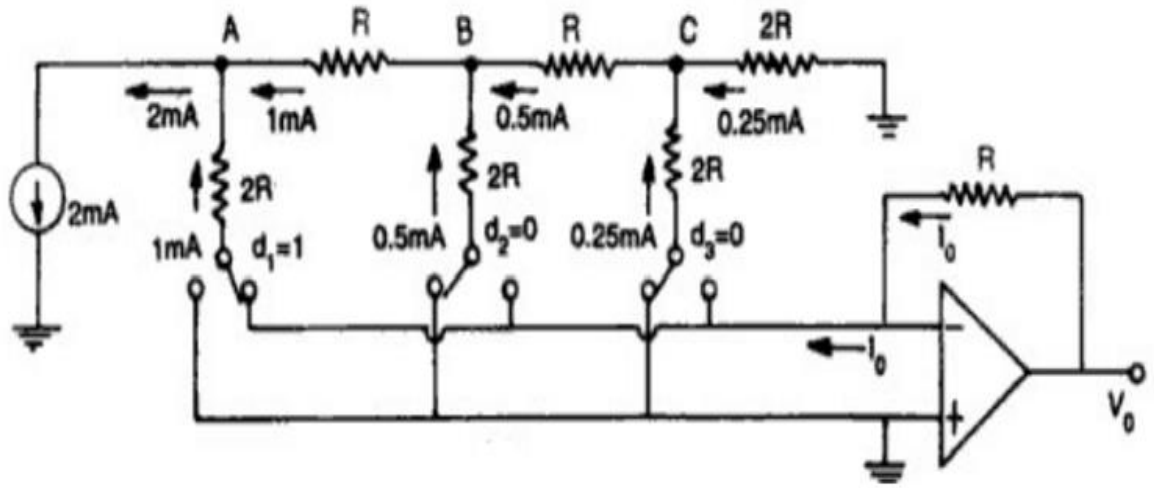
- COMPARISON:

BINARY WEIGHTED RESISTOR TYPE DAC	R-2R LADDER TYPE DAC
1. Binary resistor scaling is used. This requires large range of resistors. Example 2^1 R, 2^2 R, 2^3 R, ... 2^n R For 8 bits DAC the largest value is 256 times the smallest value	Requires only R and 2R resistors Because of this accuracy is more
2. It is impractical to fabricate large values of resistors in IC forms . Use of smaller values of resistors will load and consume more power. It is difficult to fabricate large number of resistor with different values. It affects the accuracy.	Since this type of DAC uses only two resistors, It is easier for fabrication
3. Expansion to more number of bits involve addition of larger values of resistors	Expansion is easier since one more set of same two resistors is necessary
4. Switching currents are different for different digital words. This creates unbalance in temperature gradients and lead to nonlinearities	In Inverted R-2R Ladder configuration switching currents remain same. As such power consumption is same for different digital words

Prof. G.KUMARASWAMY RAO EX DIRECTOR DLRL DRDO

Q 10. What are Current driven DACs?

The Current driven DACS uses the current scaling property of Inverted R-2R ladder type DACs. The currents have weighted binary values.



Q 11. Define i) linear error ii) offset error and iii) gain error

LINEAR ERROR:

This is defined as the amount by which the actual output differs from the ideal straight line output characteristics of DAC

OFFSET ERROR:

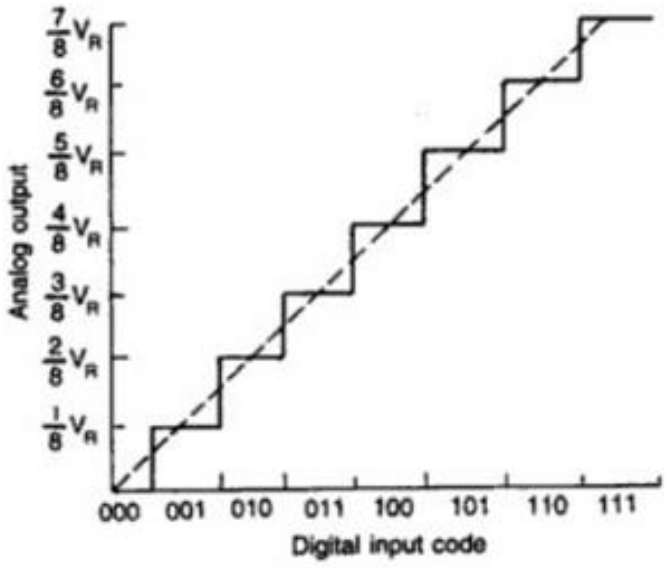
This is the nonzero level of output voltage when all inputs are zero

GAIN ERROR:

The difference between the calculated gain of the current to voltage converter and the actual gain achieved.

JNTUH PROBLEMS ON DAC

- **FORMULAE TO REMEMBER:**
- LSB = $\frac{V_{ref}}{2^N}$
- $V_{FS} = Vr_{ef} - LSB = V_{ref} - \frac{V_{ref}}{2^N} = \frac{V_{ref}(2^N - 1)}{2^N}$
- $V_{ref} = V_{FS} \frac{2^N}{(2^N - 1)}$
- $V_{ref} = 2^N$ LSB
- LSB $= \frac{V_{ref}}{2^N} = \frac{(V_{FS})}{2^N - 1} \times \frac{2^N}{2^N} = \frac{V_{Fs}}{(2^N - 1)}$
- RESOLUTION = LSB



- **10 BITS DAC**
- RESOLUTION= $\frac{V_{FS}}{(2^N - 1)}$ where V_{FS} = Full scale voltage and n = number of bits

BIT POSITION	VALUE	BIT NO.
0	2^0 =1	10(LSB)
1	2^1 =2	9
2	2^2 =4	8
3	2^3 =8	7
4	2^4 =16	6
5	2^5 =32	5
6	2^6 =64	4
7	2^7 =128	3
8	2^8 =256	2
9	2^9 =512	1 (MSB)

PROBLEM 1. The LSB of 6 bit DAC represents 0.1 V. What voltage value will be represented by the following binary words. i) 10 10 10 ii) 11 01 10

- Solution:
- $(10\ 10\ 10)_2 = 1\times2^5 + 1\times2^3 + 1\times2^1 = 42$
- Voltage value = $42 \times 0.1 = 4.2$ V
- $(11\ 01\ 10)_2 = 1\times2^5 + 1\times2^4 + 1\times2^2 + 1\times2^1 = 54$
- Voltage value = $54 \times 0.1 = 5.4\ V$

PROBLEM 2. The LSB of a 10 bit DAC is 20 mvolts. i) What is its percentage resolution? ii) What is its full scale range? iii) What is the output voltage for an input 10111 01101?

- i) Percentage resolution $20 \times 10^{-3} \times 100 = 2\%$
- ii) V_0 FS = $(2^N - 1) \times$ Resolution = $(1024-1)\times 20 \times 10^{-3} = 20.46$ V
- ii) $(10111\ 01101)_2 = 512\ (2^9) + 128\ (2^7) + 64\ (2^6) + 8\ (2^3) + 4\ (2^2) + 1\ (2^0) = 717$

  Output voltage = $717 \times 20 \times 10^{-3} = 14.34$ V
- **10 BITS DAC**
- RESOLUTION= $\frac{V_{FS}}{(2^N - 1)}$ where V_{FS} = Full scale voltage and n = number of bits

VALUE	BIT NO.
$2^0 = 1$	10(LSB)
$2^1 = 2$	9
$2^2 = 4$	8
$2^3 = 8$	7
$2^4 = 16$	6
$2^5 = 32$	5
$2^6 = 64$	4
$2^7 = 128$	3
$2^8 = 256$	2
$2^9 = 512$	1 (MSB)

PROBLEM 3: LSB OF 9 bit DAC is represented by 19.6 mVolts. If an input of 9 zero bits is represented by 0 volts. i) Find the output of DAC 10110 1101 and 01101 1011 iii) what is the Full scale reading (FSR) of this DAC

- i) $(10\ 11\ 01\ 10\ 1) = 256\ (2^8) + 64\ (2^6) + 32\ ((2^5) + 8\ (2^3) + 4\ (2^2) + 1\ (2^0) = 365$

  Output voltage = $365 \times 19.6 \times 10^{-3} = 7.154$ Volts
- ii) $(01\ 10\ 1\ 10\ 11) = 128(2^7) + 64(2^6) + 16((2^4) + 8(2^3) + 2(2^1) + 1(2^0) = 219$

  Output voltage = $219 \times 19.6 \times 10^{-3} = 4.2924$ Volts

- iii) V_{FS} = $(2^N - 1)$ × Resolution = $(2^9 - 1)$ × 19.6 ×10-3 = 10 Volts

PROBLEM 4. Calculate the number of bits required to represent a full scale voltage of 10 V with a resolution of 5 mV approximately

- Resolution =$\frac{V_{FS}}{(2^N - 1)}$
- $(2^N - 1)$ = $\frac{V_{FS}}{Resolution} = \frac{10}{5 \times 10^{-3}} = 2000$
- 2^N = 2000+1 =2001
- 2^{10} = 1024 similarly 2^{11} = 2048
- So 10 bit is not sufficient
- Minimum of 11 bits are required

PROBLEM 5. Calculate the values of the LSB and MSB and full output for a 8 bit DAC for the 0 to 10 V range

- LSB = $\frac{\mathbf{1}}{\mathbf{2^8}} = \frac{\mathbf{1}}{\mathbf{256}}$
- For 10 volts range $\frac{10}{256} = 39\ mV$
- MSB= $\frac{1}{2}$
- For 10 volts range $\frac{10}{2} = 5\ V$
- V_{FS}Full scale output = V_{ref} −1 = 10 −1 LSB = 10 −0.039=9.961V

PROBLEM 6. What output voltage will be produced by a DAC whose output range is 0 to 10 volts and whose binary number is i) 10 for a 2 bit DAC ii) 01 10 for a 4 bit DAC iii) 10 1111 00 for a 8 bit DAC

- i) LSB = $\frac{10}{2^2} = 2.5\ V$; 10 means $1\times2^1 + 0\times2^0 = 2$
- Voltage output = $2 \times 2.5 = 5V$
- ii) LSB = $\frac{10}{2^4} = 0.625$; 01 10 means $1\times2^2 + 1\times2^1 = 6$
- Voltage output = 6 ×0.625 = 3.75 V
- iii) LSB = $\frac{10}{2^8} = 0.03906$; 10 1111 00 $means$ $1\times2^7 + 1\times2^5 + 1\times2^4 + 1\times2^3 + 1\times2^2 = 188$ ∴ Voltage output = 188 × .03906= 7.34 V

MONOLITHIC DAC 1408 L

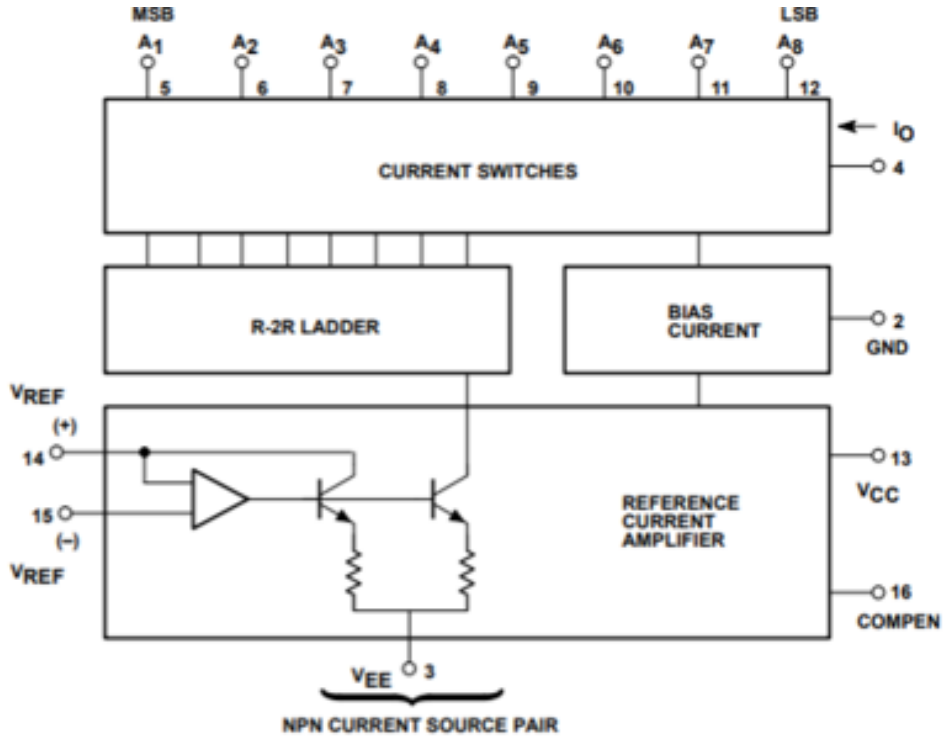
Q 12. Write note on IC 1408 DAC

8 Bit DAC MC 1498 L:

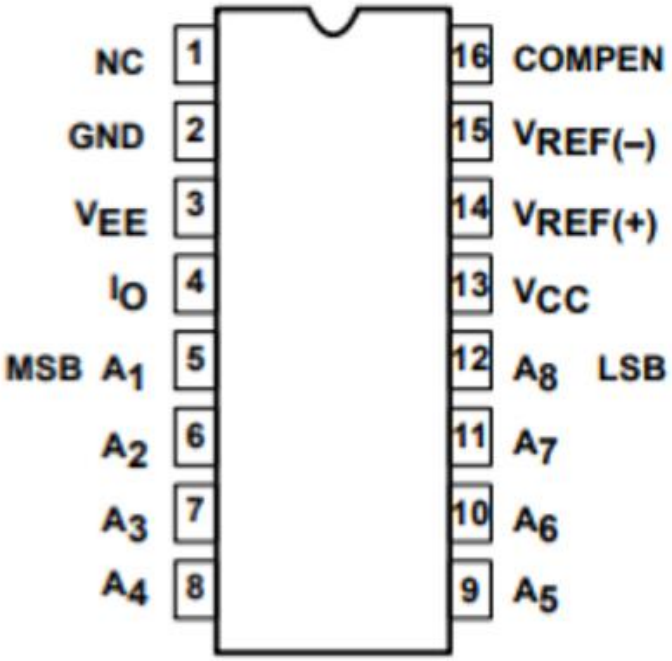
This commercial IC consists of a i) reference current amplifier ii) a R-2R ladder iii) 8 bit high speed switches. It has 8 input data lines

A_1 (MSB) ,A_2, A_3, ……(LSB). These control the positions of current switches

BLOCK DIAGRAM:

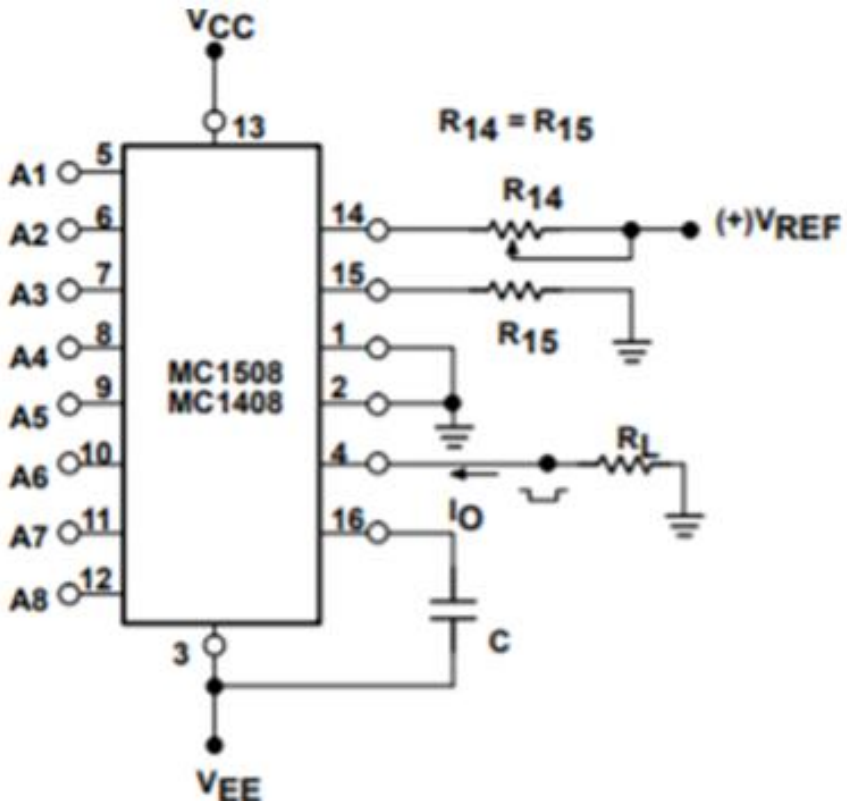


PIN DIAGRAM:



DESCRIPTION OF IC 1408 L:

The IC requires 2 mA reference current for full scale input and two power supplies VCC = + 5 V and VEE = − 5 V to – 15 V



CIRCUIT DESCRIPTION:

IC 1408 DAC requires 2 ma reference current for full scale input and two power supplies (V_{EE} range is from –5 volts to –15 Volts)

V_{ref} and resistor R_{14} determines the total reference current source and R_{15} is equal to R_{14} to match the input impedance of the reference current amplifier

Output current $I_0 = \frac{V_{ref}}{R_{14}}\left[\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right]$

Q 13. Draw and explain the typical circuit for IC 1408 DAC

Reference current = $\frac{\boldsymbol{V_{ref}}}{\boldsymbol{R_{14}}} = \frac{\mathbf{5}}{\mathbf{2.5\,K}}$

= 2 mA

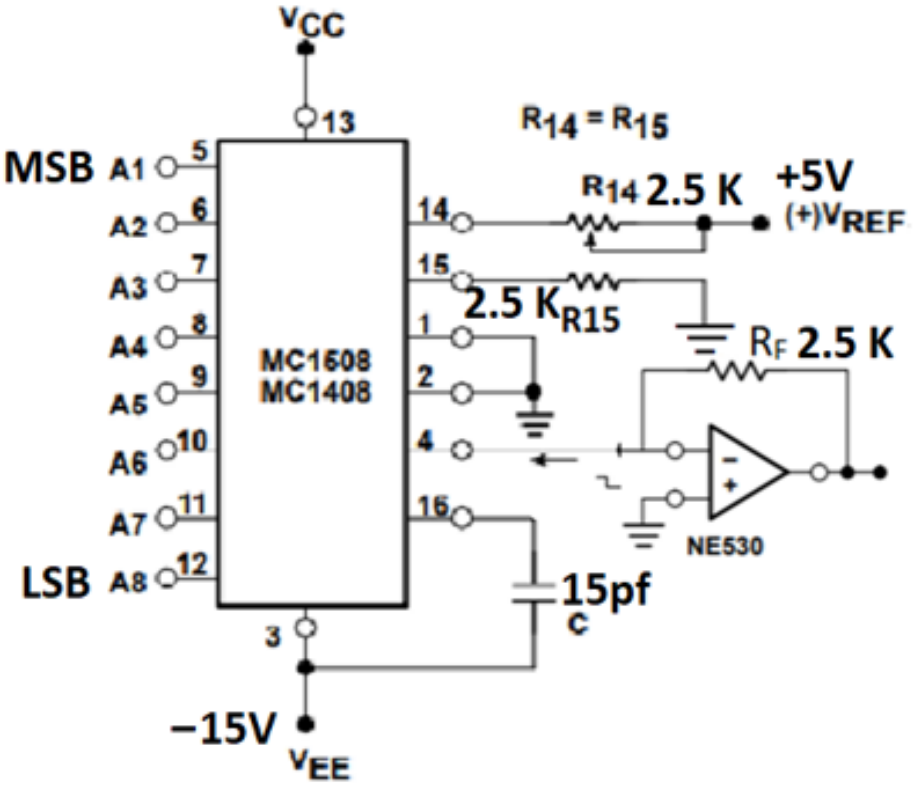
Full scale current is obtained

when A_1 through A_8 are all logic 1

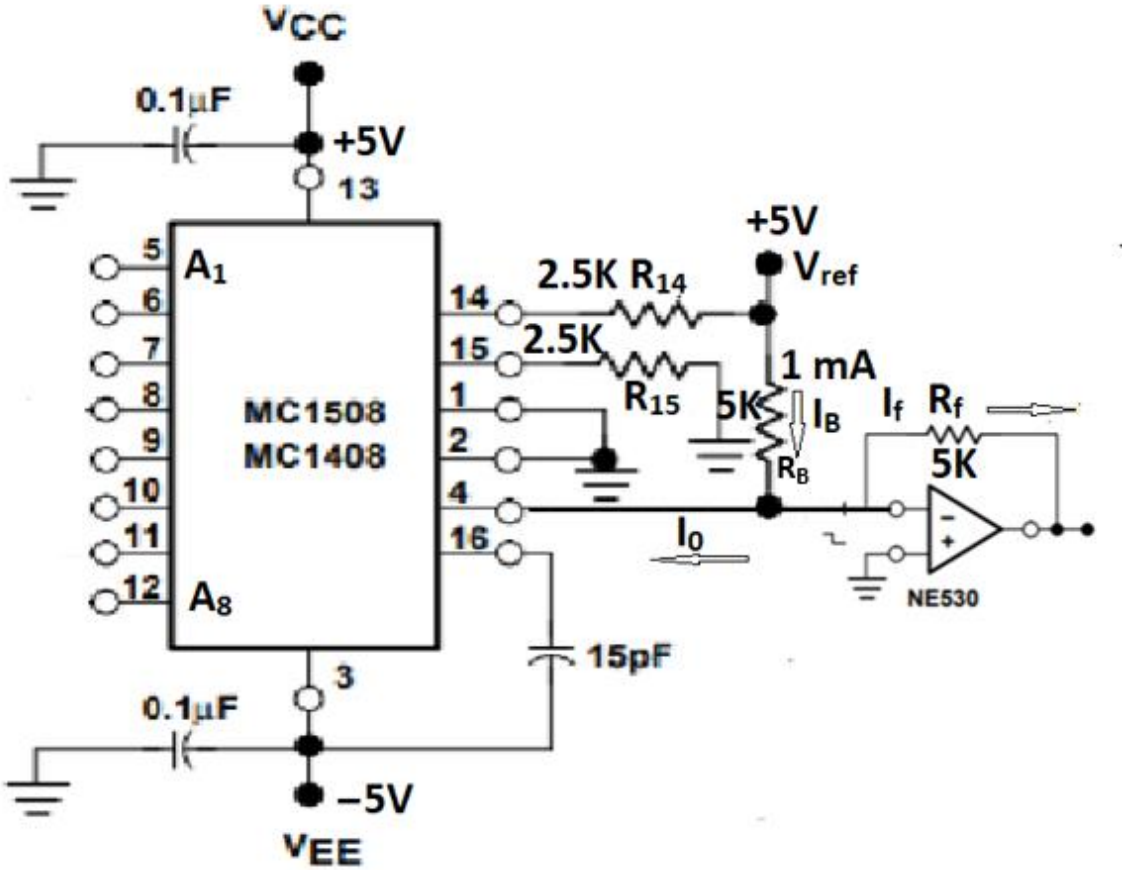
$$I_0 = \frac{5}{(2.5)(10^3)}\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}\cdots \frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$= \frac{\mathbf{2\,mA\times 255}}{\mathbf{256}} = 1.992\,mA$

Output voltage V_0 = 1.992mA×2.5 K = 4.98 V



DUAL POLARITY DAC



PROBLEM 7.

- Binary input to DAC= 0000 0000 (00H)
- Output current I_0 at pin 4 =0
- I_B Current flowing through R_B = 1 mA

All this current flows through R_f $\therefore$ $V_o = -I_f R_f = (1)(10^{-3})(5)(10^3) = -5V$

PROBLEM 8.

- Binary input to DAC = 1000 0000 (10H)
- Output current I_0 at pin 4 = 1 mA
- Using KCL $-I_B + I_0 + I_f = 0$
- $-(1mA) + (1mA) + I_f = 0$
- $I_f = 0$ $V_o = I_f R_f = -(0)(10^{-3})(5)(10^3) = 0V$

PROBLEM 9.

- Binary input to DAC = 1111 1111 (FFH)
- Output current I_0 at pin 4 = 2 mA
- Using KCL $-I_B + I_0 + I_f = 0$
- $-(1mA) + (2mA) + I_f = 0$
- $I_f = -1$ mA $V_o = I_f R_f = -(-1)(10^{-3})(5)(10^3) = +5V$

ADC INTRODUCTION

Q 14. What is ADC ?

An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.
Analog signals are directly measurable quantities.
Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1 (HIGH or LOW)

Q 15. Why ADC is needed?

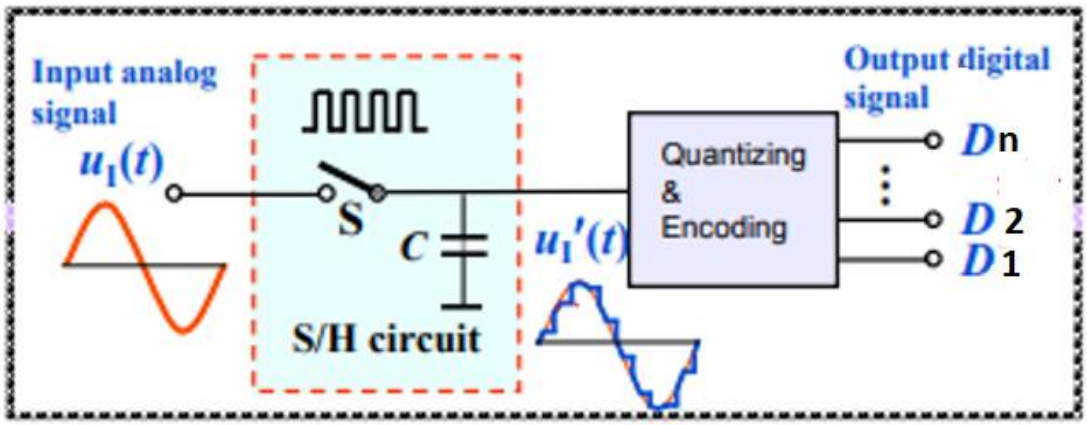
Microprocessors can only perform complex processing on digitized signals.
When signals are in digital form they are less susceptible to the effects of additive noise.
ADC Provides a link between the analog world of transducers and the digital world of signal processing and data handling.

Q 16. What are the applications of ADC :

ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form.
Some examples of ADC usage are digital volt meters, cell phones, thermocouples, and digital oscilloscopes.
Microprocessors commonly use 8, 10, 12, or 16 bit ADCs. Micro controller uses an 8 or 10 bit ADC.

Q 17. What is the process of A to D conversion?

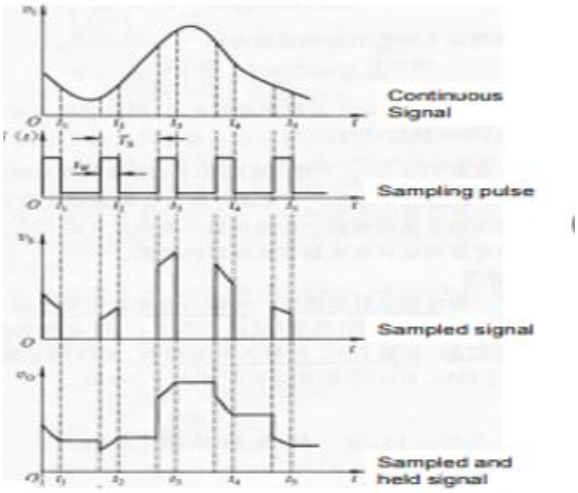
i) Sampling and Holding (S/H)
ii) Quantizing and Encoding (Q/E)



Q 18. What is Sample and Hold?

Holding signal benefits the accuracy of the ADC

Minimum sampling rate should be at least twice the highest data frequency of analog signal as per the Nyquist rate



Q 19. What is quantizing and encoding ?

RESOLUTION:

The smallest change in analog signal that will result in the digital word

$$\Delta V = \frac{V_r}{2^N}$$

V = Reference voltage range

N = Number of bits in digital output.

2^N = Number of states.

ΔV = Resolution

QUANTIZING:

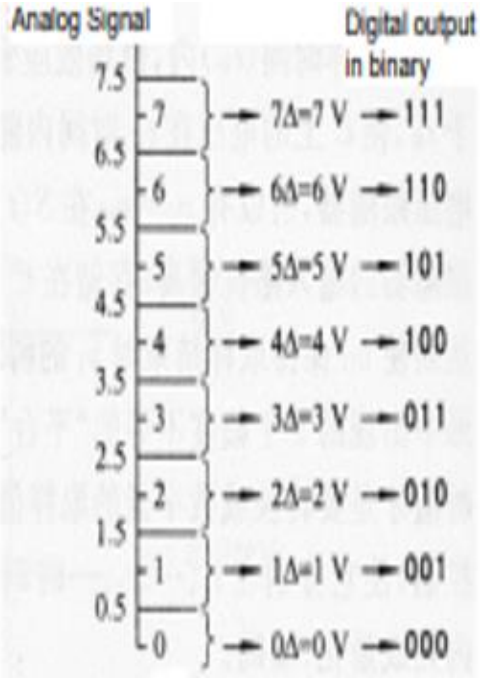
Partitioning the reference signal range into a number of discrete quanta, then matching the input signal to the correct quantum.

ENCODING:

Assigning a unique digital code to each quantum , then allocating the digital code to the input signal

$$\Delta V = 1V$$

$$\text{Maximum Quantization error} = \pm\frac{1}{2}\Delta V = \pm 0.5V$$

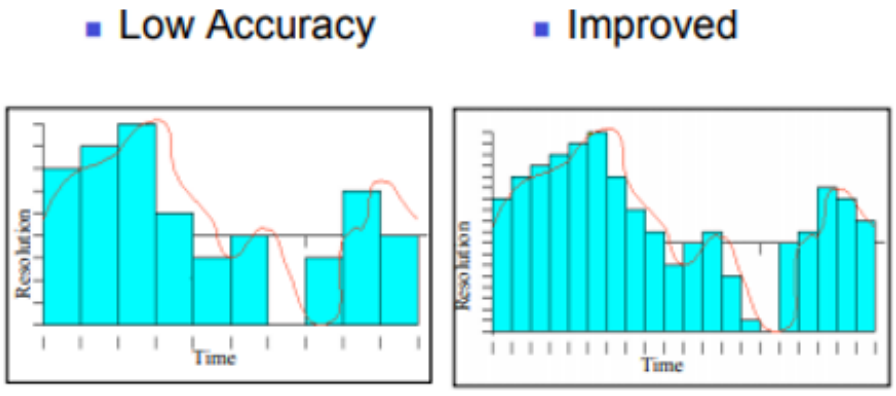


Q 20. Define Accuracy of ADC

ACCURACY OF ADC:

i) Increase the resolution . This improves the accuracy in measuring the amplitude of the analog signal

ii) Increase the sampling rate . This improves the maximum frequency that can be measured



Q 21. Write a short note on ADC

ADC is a quantization process. Analog signal is converted into equivalent binary word

1. Function of ADC is exactly opposite to the function of DAC. It converts analog input voltage and produces an output binary word 'D'

D = d_1 d_2 d_3 d_4 ….. d_n where d_1 is MSB and d_n is LSB

D = $d_1\ 2^{-1} + d_2\ 2^{-2} + d_3\ 2^{-3} + d_4\ 2^{-4} + \ldots\ldots\ldots + d_n\ 2^{-n}$

2. ADC has 2 control lines i) START input: this tells the ADC to start the conversion and ii) End of conversion (EOC) this is the output signal. This announces that the conversion is over.
3. ADC are designed for microprocessor interfacing or directly driving LCD or LEDs

CATEGORIZATION OF ADCs:

ADCs are categorized into 2 categories based on the types of Conversion techniques a) Direct type : they compare the given analog signal with the internally generated equivalent signal b)Integrating type : first change the analog signal to a linear function of time or frequency and then change it into a digital code

A. Direct type:

1, Flash or comparator type –very fast but expensive
2. Counter type
3. Tracking or Servo Converter
4. Successive Approximation –mostly used in Data loggers and instrumentation- they are faster but less accurate

B. Integrating type: generally used in digital meters, panel meters

1. Charge balancing
2. Dual Slope

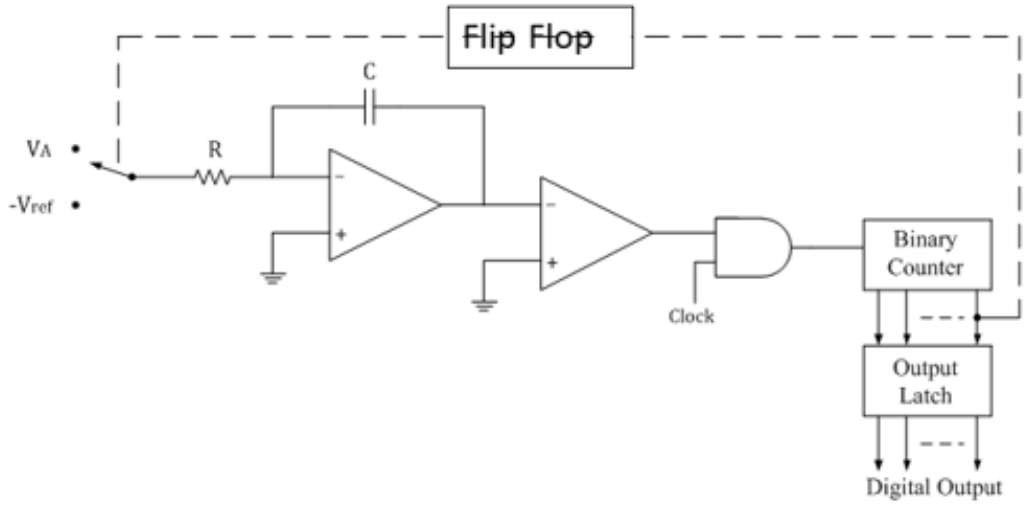
CLASSIFICATION BASED ON CONVERSION TECHNIQUES:

ADCs are also classified into 2 categories based on conversion techniques
a) Compare given analog signal with the internally generated reference voltages Ex: i) Successive approximation and ii) Flash type
b) Change the given analog signal into time or frequency and compare these values against known values Ex: i) Integrator converters and ii) Voltage to frequency converters

DIFFERENT TYPES OF ADCs

DUAL SLOPE TYPE OF ADC

Q 22. Write short note on Dual slope ADC



In this type of ADC the integrator generates 2 different ramps. i) one ramp with input voltage V_A and ii) another ramp with a known —V_{ref} . Hence it is called Dual slope ADC

1. The binary counter is initially RESET to 0000. The output of integrator also RESET to 0 V
2. The integrator switch is connected to V_A. Since V_A is positive a negative ramp is produced at the output of Integrator. It is applied to Comparator
3. The output of Comparator is High (positive). The clock is passed through AND gate. The binary counter starts counting the clock pulses and increases its count.
4. The analog switch is controlled by the MSB of the counter. As long as the MSB is LOW, the analog switch is connected to V_A. When MSB becomes logic high, the switch connects the integrator to $-V_{ref}$ through the flipflop FF. At the same time the binary counter resets to 0000. The time for which the clock pulses are applied to the counter is fixed and can be denoted as t_1.
5. Since the analog switch is now connected to $-V_{ref}$ the integrator start charging in the negative direction , a negative ramp is generated
6. When integrator output reaches zero volts, the Comparator goes LOW. The AND gate stops the clock pulses going to the Binary counter. The counter stops after a time t_2.
7. The negative going ramp voltage of integrator in time t_1 is given as

$$Vi = -\frac{1}{R_1C_1}\int_0^{t_1} V_A\, dt = \frac{-V_A\, t_1}{R_1C_1}$$

8. The positive going ramp output voltage of integrator in time t_2 is given as

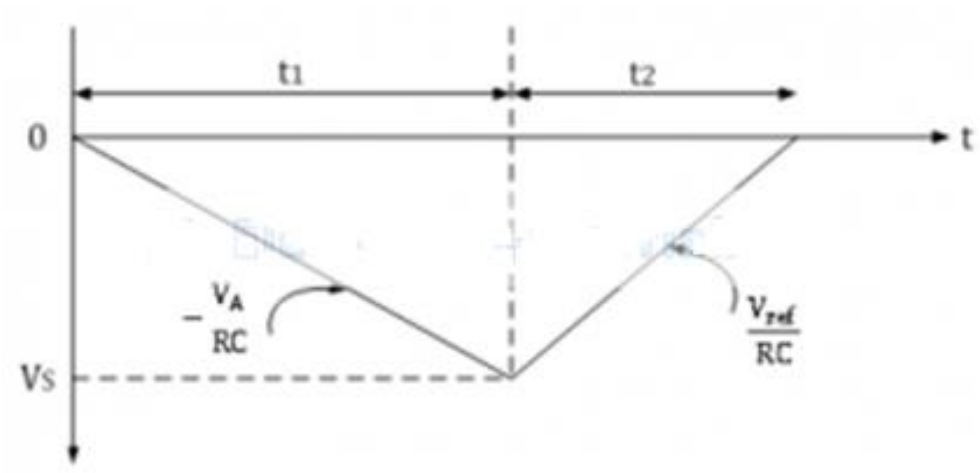
$$Vi = +\frac{1}{R_1C_1}\int_0^{t_1} V_{ref}\, dt = \frac{+V_{ref}\, t_2}{R_1C_1}$$

9. The integrator ramp up from o volts in time t_1 and ramp down to 0 volts in time $t2$. so the charge voltage is equal to discharge voltage

$$\frac{V_A\, t_1}{R_1\, C_1} = \frac{V_{ref}\, t_2}{R_1\, C_1}$$

$V_A\, t_1 = V_{ref}\, t_2$ So $t_2 = \frac{V_A\, t_1}{V_{ref}}$

∴ t_2 is directly proportional to V_A because t_1, V_{ref} are constants.



10. The contents of binary counter indicates the time t_2 .
11. Digital output = (count/sec) t_2 = (counts/sec) $t_1 \frac{V_A}{V_{ref}}$

PROBLEM 10. For a particular dual slope ADC , t1 is 83.33 ms and reference voltage is 100 mV. Calculate t2 if i) VA is 100 mV and ii) 200 Mv

i) $t_2 = \left(\frac{V_A}{V_R}\right) t_1 = \frac{100(10^{-3})}{100(10^{-3})} (83.33)(10^{-3})$= 83.33 ms

If the clock is 1msec . The number of clock pulses 83.33/1 =83

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
128	64	32	16	8	4	2	1
0	1	0	1	0	0	1	1

Check : 64 + 16+ 2 +1 =83 The binary word is 0 1 0 1 0 0 1

ii) $t_2 = \left(\frac{V_A}{V_R}\right) t_1 = \frac{200(10^{-3})}{100(106^{-3})} (83.33)(10^{-3})$= 166.6 ms

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
128	64	32	16	8	4	2	1
1	0	1	0	0	1	1	0

Check : 128 + 32 + 4 + 2 = 166 . The binary word is 1 0 1 0 0 1 1 0

Q 23. State the advantages and disadvantages of dual slope ADC

Advantages:

i) accurate
ii) cost low cost
iii) immune to temperature because of R and C since t2 is independent of R and C

Disadvantage :

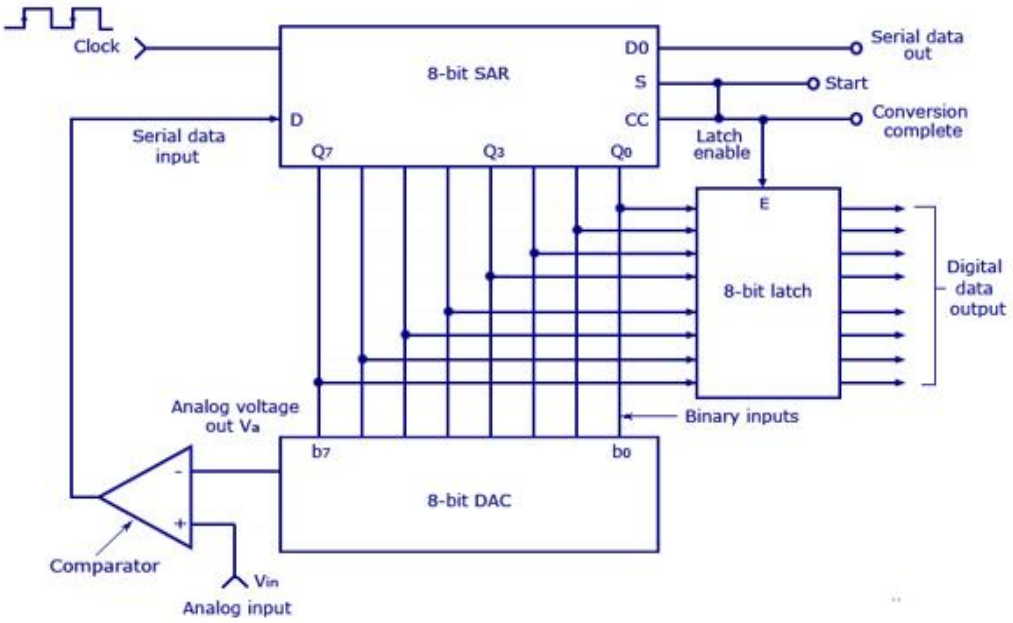
Speed is low since t1 and t2 takes time

SUCCESSIVE APPROXIMATION ADC

Q 24. Explain Successive Approximation type ADC with neat block diagram

CIRCUIT DIAGRAM:

This type of ADC consists of
i) Successive Approximation Register (SAR)
ii) Comparator
iii) DAC
iV) Output Latches



Successive Approximation Type Analog to Digital Converter

SALIENT FEATURES:

1. This ADC uses binary search technique. An 8 bit Converter requires 8 clock pulses to obtain the digital output
2. The output of 8 bit SAR is given to the 8 bit DAC. Analog signal input is denoted as V_A. The analog output of DAC is denoted as V_D
3. V_D is compared with V_A in the comparator. The output of the Comparator is a serial data input to the SAR.
4. Till the digital output (converted into V_D by DAC) from SAR is equivalent to the Analog signal input V_A, the SAR adjusts itself.
5. When $V_D = V_A$ the updating of SAR stops and EOC (End Of Conversion) is generated. The SAR output is latched in to the 8 bit Latch and the value is held until the next EOC signal is generated

OPERATION OF THE CIRCUIT:

1. When the START command is applied, the SAR sets the MSB $d_1 = 1$. All other bits are set to LOW. The trial code is 1 0 0 0 0 0 0 0. This digital word is applied to DAC. The output of DAC is Vd and it is compared with V_A in the comparator
2. Case (i) V_A is greater than V_D. This means digital 1 0 0 0 0 0 0 0 is less than V_A. The MSB is left at '1' . The next lower bit (MSB –1) is made '1'. This new trial code 11 0 0 0 0 0 0 is tested like the above.
3. Case (ii) VA is less than VD. This means 1 0 0 0 0 0 0 0 is more than VA. So MSB is reset to '0'. The next lower bIt (MSB –1) is made '1'.
The new trial code 0 1 0 0 0 0 0 0 is tested like the above
4. This procedure is repeated for subsequent bits one by one, until all bits are tested
5. After testing of all 8 bits are completed the SAR makes the END OF CONVERSION signal (EOC) . EOC signal become HIGH to show that the parallel output lines contain valid data. The EOC signal in turn enables the latch. Digital data appear at the output of the latch.

TIME FOR ONE ANALOG CONVERSION T_C

TC = T (N +1) where T = clock period and N = number of bits

OPERATION OF SAR

Correct digital representation	*Successive approximation register output V_d at different stages in the conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Successive approximation conversion sequence for a typical analog input

Q 26. How many clock periods are required for an 8 bit successive ADC for a single conversion?

Nine clock periods

FLASH ADC

Q 27. Write short note on FLASH ADC

FLASH ADC:

This is the fastest , simplest and most expensive ADC. Since it consists of large number of Comparators.

For a 3bit flash ADC 2^3 = 8 comparators are required. For a 10 bit ADC the number of comparators required are 2^{10} =1024

The circuit for a 3 bit ADC consists of

i) resistive divider network,

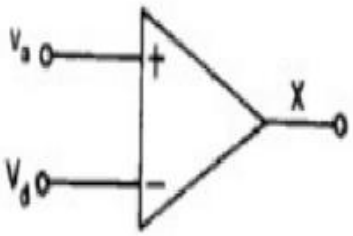
ii) 8 Op-amp comparators and iii) 8 line to 3 line encoder (3-bit priority encoder) .

Small amount of hysteresis is built into the comparators to resolve any problems that may occur if both inputs are of equal values

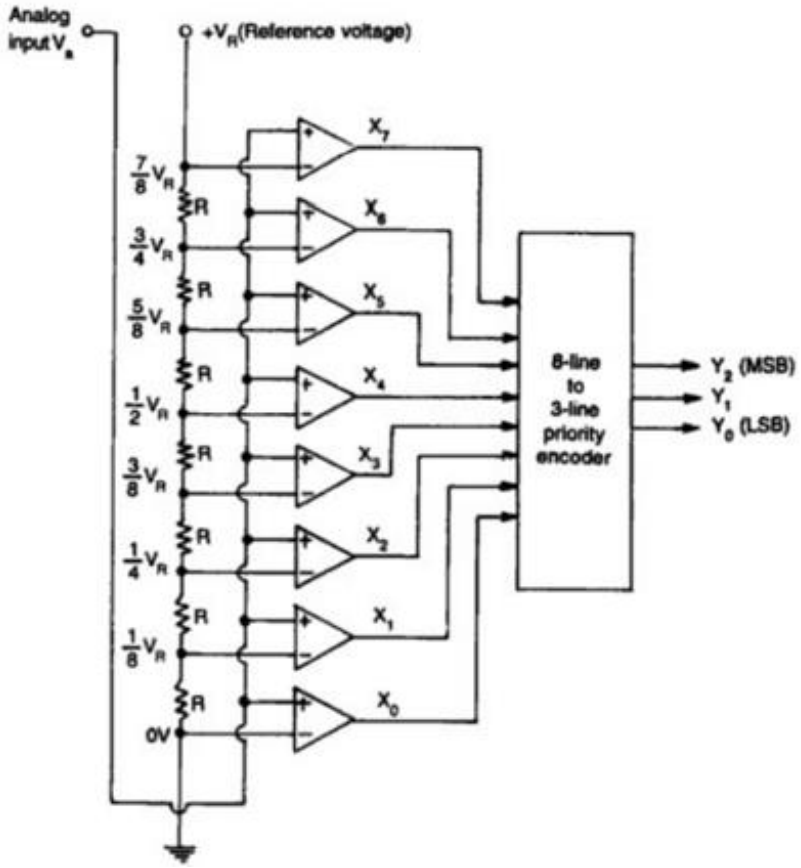
All the resistors are of equal value. The voltages at each of the node is set by the reference voltage V_R The circuit compares the analog input voltage V_a with each of the node voltages.

The circuit has high speed since all the comparators operate simultaneously.

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value



Comparator and its truth table



3 BIT PRIORITY ENCODER

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Q 28. Write the advantages and disadvantages of FLASH ADC

DISADVANTAGE OF FLASH ADC:

1. Number of converters required are large. For example 10 bit Flash ADC requires 2^{10} = 1024 Comparators.
2. Large number of comparators required as N increases.
3. Cost is more
4. Less accurate

ADVANTAGE:

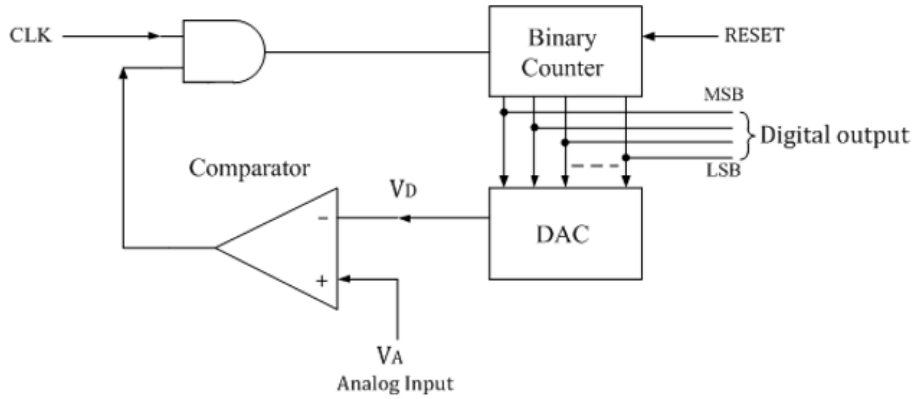
Flash ADC is the fastest ADC. All comparators operate simultaneously. The delay in output is equal to the propagation delay of one comparator

COUNTER TYPE ADC

Q29. Explain the working of Counter type ADC

FEATURES:

This uses DAC for A to D conversion. The output of DAC V_D is continuously compared with analog input V_A. When V_D becomes greater than V_A the digital input to the DAC is noted. This represents the analog input V_A in digital format.



This ADC consists of i) Binary counter ii) DAC iii) Comparator and iv) AND gate

OPERATION:

1. Initially the Counter is RESET. All its digital bits LOW . This is applied to DAC. Output of DAC V_D is zero.
2. V_A and V_D are given to a Comparator. Since V_A is higher than V_D the comparator output is HIGH
3. One input to AND gate is the Clock pulses and the other end is from the Comparator. Since comparator is HIGH the AND gate allows the clock pulses. They are applied to the Binary counter
5. The counter starts counting these clock pulses. The digital output of the counter keep increasing . This increases the DAC analog output $\mathbf{V_D}$.
6. The counter keep up counting until V_D just becomes more than V_A. At this instant comparator output becomes LOW. The AND gate stops passing the clock pulses. The binary counter is stopped since no clock pulses are applied.
7. The output of Binary counter which is in digital form represents the equivalent of V_A
8. The next cycle of binary counting starts by applying the second RESET pulse. The above cycle of operation repeats for the changed V_A

Q 30. State the disadvantages of Counter type of ADC.

1. DAC and comparator take specific time to complete its operation. This restricts the frequency of clock pulses. If clock frequency is low, speed of conversion becomes less.
2. Conversion time is not constant . When V_A is high the conversion time is more

PROBLEM 11. Calculate the Conversion time for a full scale input in case of a 12-bit counter type ADC driven by 2 MHz clock

T = $\frac{1}{(2)(10^6)} = 0.5\ \mu sec$

The total time for a full scale input in case of a 12-bit counter type ADC
= $(2^N - 1)$ (T) = $(2^{12} - 1)$ (0.5)(10^{-6})= 2.047×10^{-3} = 2.047 msec

PROBLEM 12. Determine the resolution of an 8 bit ADC for a 10 V input range

V_{FS} = 10 V

Resolution = $\frac{V_{FS}}{2^N - 1} = \frac{10}{2^8 - 1} = \frac{10}{255} = 39.215\ mV$

PROBLEM 13. An 8 bit ADC is capable of accepting an input unipolar (positive values only) 0 to 10 V. What is the minimum value of 1 LSB. What is the digital output code if the applied input voltage is 5.4 V

LSB = $\frac{V_{FS}}{2^N - 1} = \frac{10}{2^8 - 1} = \frac{10}{255} = 39.215\ mV$

Digital output code for Vi = (5.4 V) = $\frac{5.4}{39.215 \times \times 10^{-3}} = 138 = 10001010$

PROBLEM 14. What is the conversion time of a 10 bit successive approximation ADC if its input clock is 5 MHz

T = $\frac{1}{f} = \frac{1}{5 \times 10^6} = 0.2\ \mu sec$

N = 10

Tc = T (N+1) = 0.2 (10+1) = 2.2 μsec

Q 30. Compare three ADC types

PARAMETER	DUAL SLOPE	SUCCESSIVE APPROXIMATION	FLASH
SPEED	SLOW	FAST	FASTEST
RESOLUTION	2^{16} OR MORE	UPTO 2^{16}	NOT MORE THAN 2^8
ACCURACY	GOOD	MEDIUM	LOW
INPUT HOLD TIME	VERY HIGH. SO SAMPLE & HOLD CIRCUIT IS REQUIRED	DEPENDS ON NUMBER OF BITS	VERY LESS SINCE ALL COMPARATORS OPERATE SIMULTANEOUSLY

PARAMETER	DUAL SLOPE	SUCCESSIVE APPROXIMATION	FLASH
UPGRADE TO NEXT HIGHER BIT	CAN BE DONE	CAN BE DONE	REQUIRES DOUBLE THE NUMBER OF COMPARATORS. PRIORITY ENCODER BECOMES COMPLEX
COST	LESS	MODERATE	VERY COSTLY
APPLICATION	USED WHEN HIGH ACCURACY AND RESOLUTION IS REQUIRED. SPEED IS NOT IMPORTANT	HIGH SPEED WITH EXCELLENT RESOLUTION. USED IN DATA ACQUISITION APPLICATIONS. BUT REQUIRES A DAC	BECAUSE OF HIGH SPEED USED IN FIBER OPTIC COMMUNICATION. USED IN IMAGE PROCESSING. USED IN HIGH SPEED DATA TRANSMISSION

UNIT 5 CONCLUDED