BHARAT INSTITUTE OF ENGINEERING & TECHNOLOGY

MANGANPALLY 501510

IBRAHIMPATNAM RR DISTRICT

ECE DEPARTMENT

AS PER : R18 B.TECH. ECE SYLLABUS

EC 407 PC : LINEAR IC APPLICATIONS LAB B.Tech. II YEAR II SEM

LAB MANUAL

PREPARED BY

Prof. G.KUMARASWAMY RAO

ECE DEPARTMENT

(JULY 2022)

(FORMER DIRECTOR DLRL DRDO MINISTRY OF DEFENCE)

LIST OF EXPERIMENTS

1. Inverting and Non Inverting Amplifiers using Op-Amps
2. Adders and Subtractors using Op-Amps
3. Comparators using Op-Amps
4. Integrator circuit using IC 741
5. Differentiator circuit using O-Amp
6. Active Filter Applications LPF , HPF (First Order)
7. IC 741 waveform generators- Sine, Square wave, and Triangular waves
8. Monostable Multivibrator using IC 555
9. Astable Multivibrator using IC 555
10. Schmitt Trigger circuits using IC 741
11. IC 565 PLL Applications
12. Voltage Regulator using IC 723
13. Three terminal voltage regulator 7805, 7809, 7912

BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

Ibrahimpatnam - 501 510

VISION OF THE INSTITUTION

To achieve the autonomous and university status and spread universal education by inculcating discipline, character and knowledge into the young minds and mould them into enlightened citizens.

MISSION OF THE INSTITUTION

Our mission is to impart education, in a conducive ambience, as comprehensive as possible, with the support of all the modern technologies and make the students acquire the ability and passion to work wisely, creatively and effectively for the betterment of our society.

VISION OF DEPARTMENT OF ECE

The vision of the Department of Electronics and Communication Engineering is to effectively serve the educational needs of local and rura students within the core area of electronics and communication engineering and develop high quality engineers and responsible citizens

MISSION OF DEPARTMENT OF ECE

The mission of the Department of Electronics and Communication Engineering is to work closely with industry, research organizations to provide high quality education in both theoretical and practical applications of electronics and communication engineering.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Domain knowledge: Graduates will be able to synthesize mathematics, science, engineering fundamentals, laboratory and work-based experiences to formulate and solve engineering problems in Electronics and Communication Engineering domains and shall have proficiency in Computer-based engineering and the use of computational tools.

PEO2: Professional Employment: Graduates will succeed in entry-level engineering positions within the core Electronics and Communication Engineering, computational or manufacturing firms in regional, national, or international industries and with government agencies.

PEO3: Higher Degrees: Graduates will succeed in the pursuit of advanced degrees in Engineering or other fields where a solid foundation in mathematics, science, and engineering fundamentals is required.

PEO4: Engineering Citizenship: Graduates will be prepared to communicate and work effectively on team based engineering projects and will practice the ethics of their profession consistent with a sense of social responsibility.

PEO5: Research and Development: To undertake Research and Development works in the areas of Electronics and Communication fields.

PROGRAMME OUTCOMES (POs):

PO1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/Development of Solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct Investigations of Complex Problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern Tool Usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The Engineer and Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and Sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project Management and Finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-Long Learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs):

PSO1: Professional Skills: An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.

PSO2: Problem-Solving Skills: An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.

PSO3: Successful Career and Entrepreneurship: An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources.

CODE OF CONDUCT FOR THE LABORATORY

- All students must observe the Dress Code while in the laboratory.
- Sandals or open-toed shoes are NOT allowed.
- Foods, drinks and smoking are NOT allowed.
- All bags must be left at the indicated place.
- The lab timetable must be strictly followed.
- Be PUNCTUAL for your laboratory session.
- Experiment must be completed within the given time.
- Noise must be kept to a minimum.
- Workspace must be kept clean and tidy at all time.
- Handle all equipments and components with care.
- All students are liable to pay for any damage to the equipment, accessories, tools, or components due to their own negligence.
- All equipment, apparatus, tools and components must be RETURNED to their original place after use.
- Students are strictly PROHIBITED from taking out any items from the laboratory.
- Students are NOT allowed to work alone in the laboratory without the Lab Supervisor
- Report immediately to the Lab Supervisor if any injury occurred.
- Report immediately to the Lab Supervisor any damages to equipment.

Before leaving the lab

- Place the stools under the lab bench.
- Turn off the power to all instruments.
- Turn off the main power switch to the lab bench.
- Please check the laboratory notice board regularly for updates.

GENERAL LABORATORY INSTRUCTIONS

- You should be punctual for your laboratory session and should not leave the lab without the permission of the teacher.
- Each student is expected to have his/ her own lab book where they will take notes on the experiments as they are completed. The lab books will be checked at the end of each lab session. Lab notes are a primary source from which you will write your lab reports.
- You and your partner will work closely on the experiments together. One partner doing all the work will not be tolerated. Both partners should be able to explain the purpose of the experiment and the underlying concepts.
- Please report immediately to the member of staff or lab assistant present in the laboratory; if any equipment is faulty.

LIST OF EXPERIMENTS

1. Inverting and Non Inverting Amplifiers using Op-Amps
2. Adders and Subtractors using Op-Amps
3. Comparators using Op-Amps
4. Integrator circuit using IC 741
5. Differentiator circuit using O-Amp
6. Active Filter Applications LPF , HPF (First Order)
7. IC 741 waveform generators- Sine, Square wave, and Triangular waves
8. Monostable Multivibrator using IC 555
9. Astable Multivibrator using IC 555
10. Schmitt Trigger circuits using IC 741
11. IC 565 PLL Applications
12. Voltage Regulator using IC 723
13. Three terminal voltage regulator 7805, 7809, 7912

IC APPLICATIONS LAB (EC407PC)

Objectives:

- To introduce the practical knowledge of the basic building blocks and their pin out and usage of linear integrated circuits.
- To design and study the characteristics, linear and non-linear applications of OP-AMPs and the practical usage in the real world.
- To analyze and design various types of filter circuits using OP-AMPs and obtain their frequency response.
- To study the internal functional blocks and to implement the applications of special ICs like IC 555 timers, PLL circuits, VCO, voltage regulator IC

Hardware Requirements:

- Cathode Ray Oscilloscope
- Regulated Power Supply
- Fixed Power Supply
- Function Generator
- Components(Resistors, Capacitors, ICs) •

Course Outcomes:

1. Design and analyze the basic OP-AMP applications such as inverting amplifier, non-inverting amplifier, adder, subtractor and comparator circuits using OP-AMP IC 741.
2. Verify the functionality of OP-AMP applications such as integrator, differentiator circuits using OP-AMP IC 741.
3. Design and analyze and Schmitt Trigger circuit and waveform generators using OP-AMP IC 741.
4. Analyze the performance of OP-AMP applications in filters using OP-AMP IC 741.
5. Verify the functionality of IC 555 based applications in multivibrator circuits and IC 565 – PLL applications.
6. Analyze the general purpose voltage regulator using IC 723 and fixed voltage regulators using IC 7805, IC 7809

Mapping of Course Outcomes leading to the achievement of POs and PSOs:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	2	2	1	1	-	-	-	-	2	2	2	-	3	3	3
CO2	2	2	1	1	-	-	-	-	2	2	2	-	3	3	3
CO3	2	3	1	1	-	-	-	-	2	2	2	-	2	2	2
CO4	2	3	1	1	-	-	-	-	2	3	2	-	3	2	2
CO5	2	2	1	2	-	-	-	-	2	2	2	-	2	2	2
CO6	2	2	1	1	-	-	-	-	2	3	2	-	3	3	2
Average	2	2	1	1	-	-	-	-	2	2	2	-	3	3	2

1-Low, 2-Supportive. 3-Highly related, - None

Attainment of Program outcomes & Program Specific oucomes

Sl.No.	Name of Experiment	Program Outcomes (POs) attained	Program Specific Outcomes (PSOs) attained
1	Inverting and Non Inverting Amplifiers using Op-Amps	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
1C	** Voltage Follower	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
2	Adders and Subtractors using Op-Amps	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
3	Comparators using Op-Amps	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
4	Integrator circuit using IC 741	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
5	Differentiator circuit using Op-Amp	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
6	Active Filter Applications LPF, HPF (First Order)	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
7	IC 741 waveform generators-Sine, Square wave, and Triangular waves	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
8	Monostable Multivibrator using IC 555	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
9	Astable Multivibrator using IC 555	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
10	Schmitt Trigger circuits using IC 741	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
11	IC 565 PLL Applications	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
12	Voltage Regulator using IC 723	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
13	Three terminal voltage regulator 7805, 7809, 7912	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3
14	**Wein bridge Oscilator	PO1,PO2.PO3,PO4, PO9,PO10,PO11	PSO1,PSO2,PSO3

** Beyond syllabus

Mapping of Experiments leading to the achievement of POs and PSOs:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
Exp 1	2	2	1	2	-	-	-	-	2	2	2	-	3	3	1
Exp 2	2	2	1	2	-	-	-	-	2	2	2	-	3	3	1
Exp 3	2	2	1	1	-	-	-	-	2	1	1	-	3	3	1
Exp 4	2	2	1	1	-	-	-	-	2	1	2	-	3	3	1
Exp 5	2	2	1	1	-	-	-	-	2	2	1	-	3	3	2
Exp 6	2	3	1	1	-	-	-	-	1	1	2	-	3	3	2
Exp 7	2	3	1	1	-	-	-	-	2	2	1	-	3	3	2
Exp 8	2	2	1	1	-	-	-	-	1	2	2	-	3	3	2
Exp 9	2	2	1	1	-	-	-	-	1	1	2	-	3	3	1
Exp 10	2	2	1	2	-	-	-	-	2	2	2	-	3	3	1
Exp 11	2	2	1	2	-	-	-	-	2	2	2	-	3	3	1
Exp 12	2	2	1	1	-	-	-	-	1	1	1	-	3	3	2
Exp 13	2	2	1	1	-	-	-	-	1	2	2	-	3	3	2
Exp 14	2	2	1	1	-	-	-	-	1	2	1	-	3	3	2
Exp 15	2	2	1	1	-	-	-	-	1	1	1	-	3	3	2
Ave	2	2	1	1	-	-	-	-	2	2	2	-	3	3	2

1-Low, 2-Supportive. 3-Highly related, - None

EXPERIMENT NO.1A
INVERTING AMPLIFIER USING OP-AMP

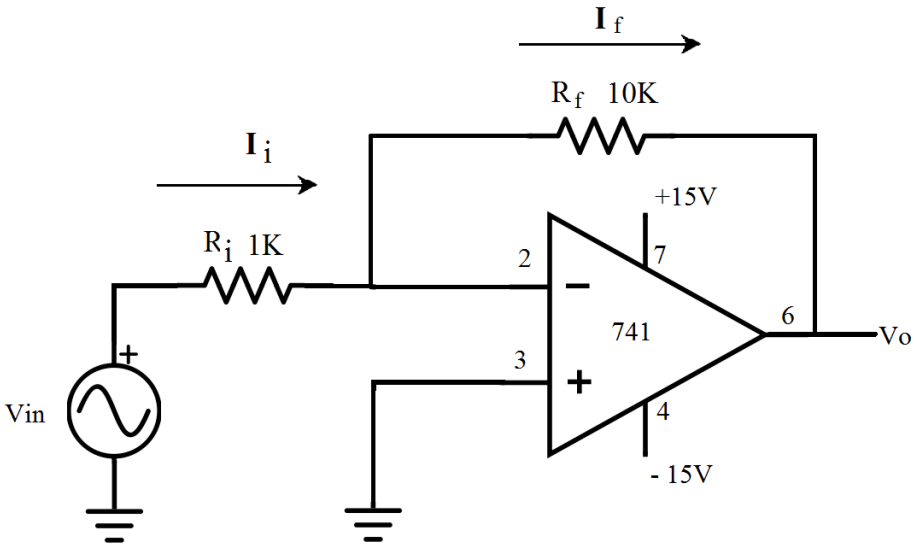
AIM: To design and setup an inverting amplifier circuit with OP AMP 741C for a gain of 10, plot the waveforms, observe the phase reversal, measure the gain.

OBJECTIVES: After completion of this experiment, one should be able to design and setup an inverting amplifier using OP AMP type no.741. for various gains.

EQUIPMENT /COMPONENTS

Sl.No.	Name and Specification	Quantity
1	Dual Power Supply +/−15 V	1
2	Function Generator (0 – 1 MHz)	1
3	Oscilloscope 10 MHz	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors	3
7	Probes and Connected wires	As required
8	Multimeter	1

THEORY BEHIND THE DESIGN



➢ The circuit employs negative feedback. The Rf is feedback resistance and Ri is the input resistance of the circuit

➢ The input terminals of the op-amp draws no current because of the large differential input impedance.

➢ The potential difference across the input terminals of an op-amp is zero because of the large open loop gain. $\Delta V = \frac{V_0}{G_a} = 0$ since $G_a \to \infty$

➢ Due to these two conditions, the inverting terminal is at virtual ground potential. Same as the non inverting terminal (which is connected to ground)

➢ So the current flowing through Ri and Rf are the same.

$I_i = -I_f$

That is $\frac{V_{in}}{R_i} = \frac{(0 - V_0)}{R_f} = -\frac{V_0}{R_f}$

Therefore $\frac{V_0}{V_{in}} = A_v = -\frac{R_f}{R_i}$

Here the –Ve sign indicates that the output will be an amplified wave with 180 degrees phase shift (inverted output). By varying the Rf or Ri, the gain of the amplifier can be varied to any desired value.

Gain of an inverting amplifier $\boldsymbol{A_v = \frac{V_0}{V_{in}} = -\frac{R_f}{R_i}}$

Let us say the required gain = −10,

That is $\boldsymbol{A_v = -\frac{R_f}{R_i} = -10}$

Let Ri = 1KΩ, Then Rf = 10KΩ

OBSERVATION1:

Vin = 0.25 v

Vo=?

Gain = $\boldsymbol{A_v = \frac{V_0}{V_{in}}}$

Record values in Table after connecting the components

Sl.No	Vi (volts)	Vo (volts)	Gain =A $-\frac{V_0}{V_{in}}$	Theoretical Gain =B	Percentage error $\frac{A-B}{B}$
1	0.25 v				
2	0.5v				
3	0.75v				
4	1.0v				

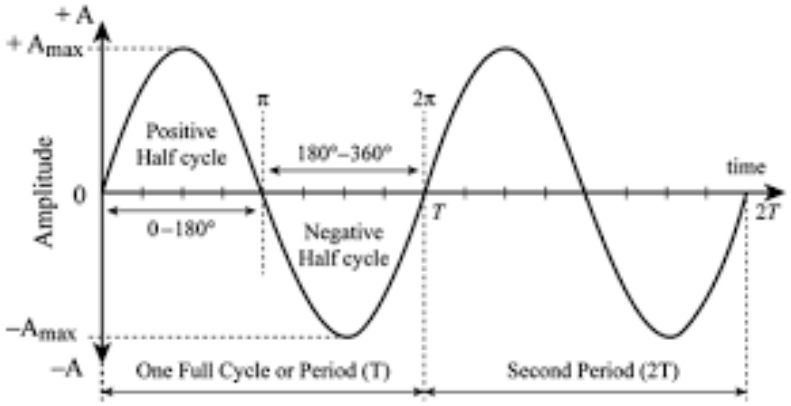
OBSERVATION2:

Change Rf from 10 k to 1k

Apply 1000Hz. Sine wave from function generator with 1 V peak to peak

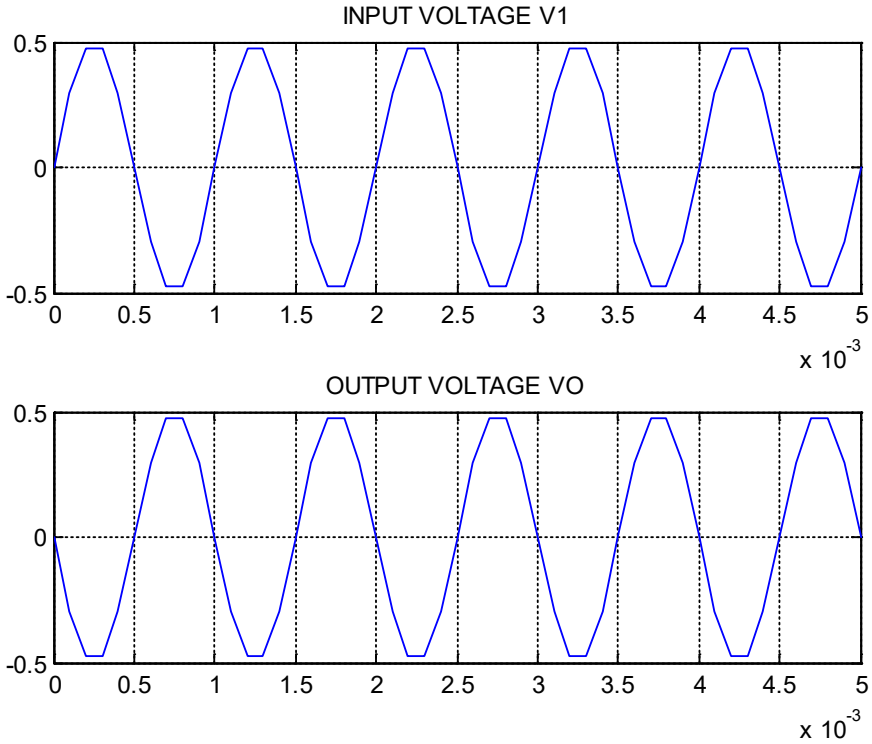
Observe phase difference between the input and the output on the CRO and draw the input and output diagram one below the other. What is the gain. Why it is now 1 ?

INPUT SINE WAVE



Output sine wave = ?

Plot the input and output graph from CRO and observe the 180 degrees phase shift (reversal of phase)



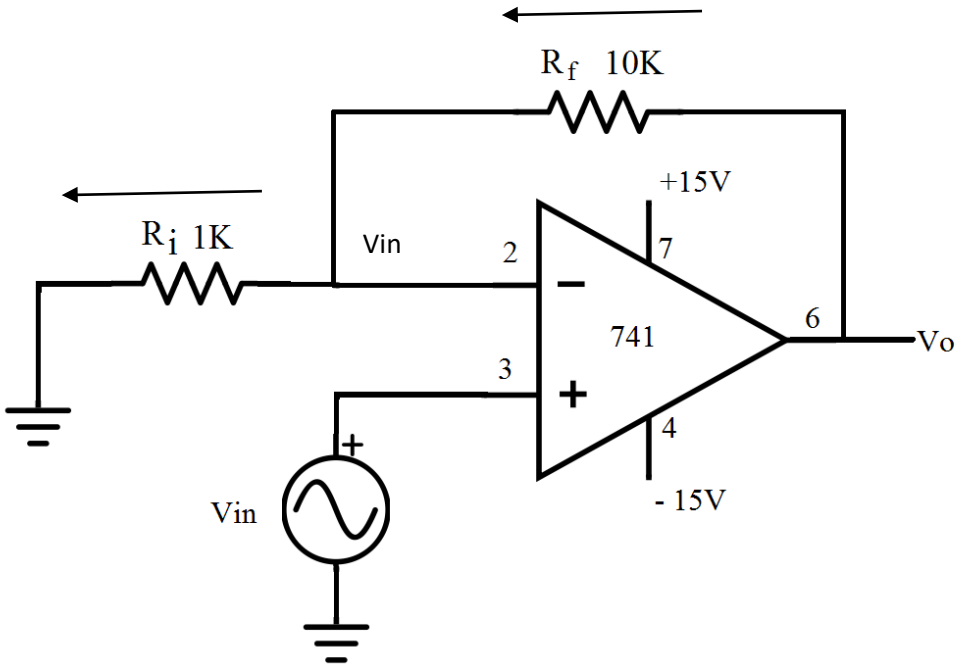
EXPERIMENT NO.1B
NONINVERTING AMPLIFIER USING OP-AMP

AIM: To design and setup a Non-inverting amplifier circuit with OP AMP 741C for a gain of 11, plot the waveforms, observe the no phase change, measure the gain.

OBJECTIVES: After completion of this experiment, one should be able to design and setup a Non-inverting amplifier using OP AMP type No.741. for various gains.

EQUIPMENNT/COMPONENTS REQUIRED:

Sl.No.	Name and Specification	Quantity
1	Dual power supply +/− 15 V	1
2	Function Generator (0–1 MHz)	1
3	Oscilloscope (10 MHz)	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors	3
7	Probes and Connecting wires	As required
8	Multimeter	1



THEORY BEHIND THE DESIGN

- The circuit employs negative feedback. The Rf is feedback resistance and Ri is the input resistance and connected to ground.

- The input terminals of the op-amp draws no current because of the large differential input impedance.

- The potential difference across the input terminals of an op-amp is zero because of the large open loop gain. $\Delta v = \frac{V_0}{G} = 0$ since $G \rightarrow \infty$

- Due to these above two conditions, the inverting terminal is at Vin potential, same as the non-inverting terminal (which is connected to Vin)

- So the current flowing through Ri and Rf are the same.

The directions of current are shown in figure (Vin is taken as + positive)

$$I_i = I_f$$

$$I_i = \frac{\text{Vin} - 0}{\text{Ri}} = \frac{\text{Vi}}{\text{Ri}}$$

$$I_f = \frac{\text{Vo} - \text{Vin}}{\text{Rf}}$$

But

$$I_i = I_f$$

$$\frac{\text{Vin}}{\text{Ri}} = \frac{\text{Vo} - \text{Vin}}{\text{Rf}}$$

$$\text{Vin}\left(\frac{1}{\text{Ri}} + \frac{1}{\text{Rf}}\right) = \frac{\text{Vo}}{\text{Rf}}$$

$$\text{Vin}\left(\frac{\text{Rf} + \text{Ri}}{\text{Ri}\ \cancel{\text{Rf}}}\right) = \frac{\text{Vo}}{\cancel{\text{Rf}}}$$

$$\text{Vin}\left(1 + \frac{\text{Rf}}{\text{Ri}}\right) = \text{Vo}$$

DESIGN :

Gain of an inverting amplifier

$$A_V = \frac{V_0}{V_{in}} = 1 + \frac{R_f}{R_i}$$

Let the required gain be 11,

Therefore $A_V = 1 + \frac{R_f}{R_i} = 11$

$\frac{\text{R}_\text{f}}{\text{R}_\text{i}}$ = 10

Take Ri= 1KΩ, Then Rf = 10KΩ

OBSERVATION1:

Vin = 0.25 v

Vo=?

Gain, $Av = \frac{V_0}{V_{in}}$ =?

RECORD VALUES IN TABLE

Sl.No	Vi (volts)	Vo (volts)	Practical GAIN = A $\frac{V_0}{V_{in}}$	Theoretical Gain = B	Percentage error $=\frac{(A-B)}{B} \times 100$
1	0.25 v			11	
2	0.5v			11	
3	0.75v			11	
4	1.0v			11	

OBSERVATION2:

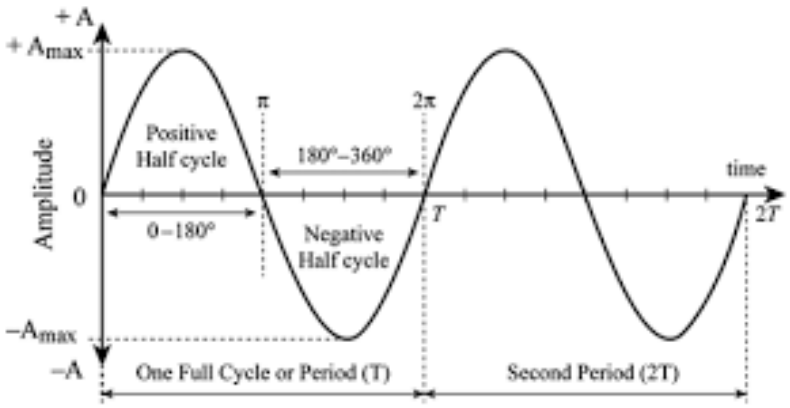
Change Rf from 10 k to 1k

Apply 1000Hz. Sine wave from function generator with 1 V peak to peak

Observe phase difference between the input and the output on the CRO and draw the input and output diagram one below the other. What is the gain?

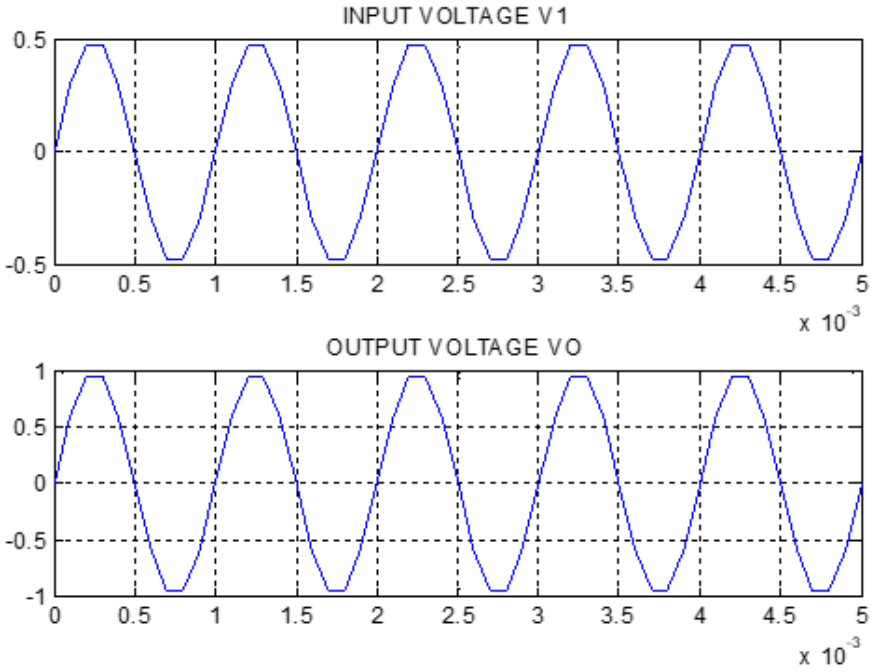
Why is it now 2 ?

INPUT SINE WAVE



OUTPUT SINE WAVE = ?

Plot the input and output graph from CRO and observe the 0 degrees phase shift (no phase shift)



EXPERIMENT NO.1C
BUFFER AMPLIFIER USING OP-AMP

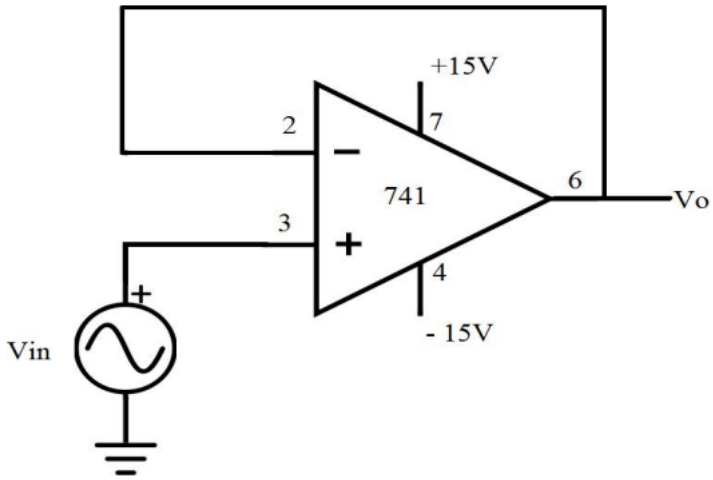
AIM: To design and setup a voltage follower circuit with OP-AMP IC 741 and observe the waveform

OBJECTIVE: After completion of this experiment, one should be able to design and setup a Voltage follower circuit using OP AMP type No.741. for unity gain.

EQUIPMENNT/COMPONENTS REQUIRED:

SL.NO.	Name and Specification	Quantity
1	Dual power supply +/− 15 V	1
2	Function Generator (0–1 MHz)	1
3	Oscilloscope (10 MHz)	1
4	Bread Board	1
5	IC 741 C	1
6	Probes and Connecting wires	As required
7	Multimeter	1

CIRCUIT DIAGRAM



THEORY BEHIND THE DESIGN:

A voltage follower is also called a unity-gain amplifier or buffer amplifier or isolation amplifier.
It has a voltage gain of 1. This means that the op amp does not provide any amplification to the signal.
It is called a voltage follower because the output voltage follows the input voltage which means the output voltage is same as the input voltage.
Though the gain is unity, this circuit offers high input impedance and low output impedance and hence it is used as buffer. This is used to isolate a low impedance load from a voltage source to eliminate any loading that might occur
Pin No.3 is at potential V_{in}
Pin No.2 is also at the same potential as pin no.3 ie V_{in} because of the concept that ΔV = 0 (Voltage at pin no.3 –Voltage at pin no.2) because of open-loop gain of Op-Amp → ∞
Voltage at pin no.3 = Voltage at pin no 2 = Vin
But Pin no.2 is directly connected to the output
Hence $V_0 = V_{in}$. The output voltage is equal to input voltage. The gain is unity.

DESIGN :
Gain of Buffer amplifier = 1

Observation1:

Vin = 0.25 v

Vo=?

Gain, $\mathrm{Av} = \frac{\mathrm{V_0}}{\mathrm{V_{in}}}$ =?

RECORD VALUES IN TABLE BELOW

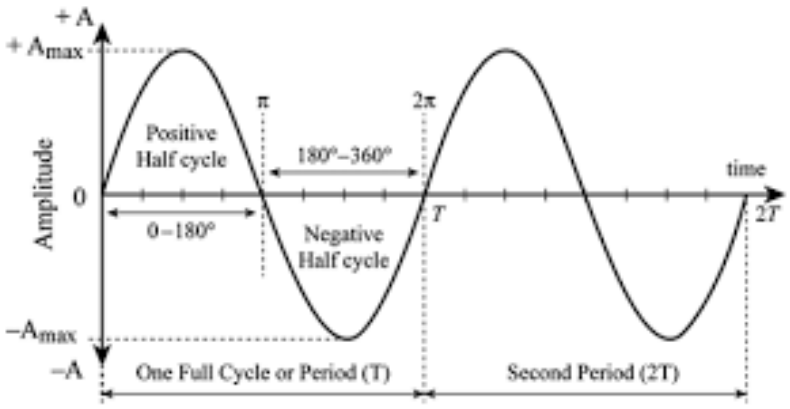
Sl.No	Vi (volts)	Vo (volts)	Practical GAIN = A	Theoretical Gain = B	Percentage error

			$\frac{V_0}{V_{in}}$		$=\frac{(A-B)}{B} \times 100$
1	0.25 v			1	
2	0.5 v			1	
3	0.75 v			1	
4	1.0 v			1	
5	2.0 v			1	
6	4.0 v			1	
7	8.0 v			1	
8	10.0 v			1	

OBSERVATION2:

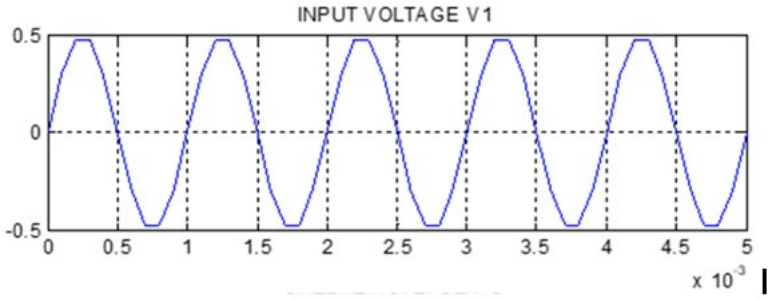
Apply 1000Hz. Sine wave from function generator with 1 V peak to peak Observe phase difference between the input and the output on the CRO and draw the input and output diagram one below the other. What is the gain?

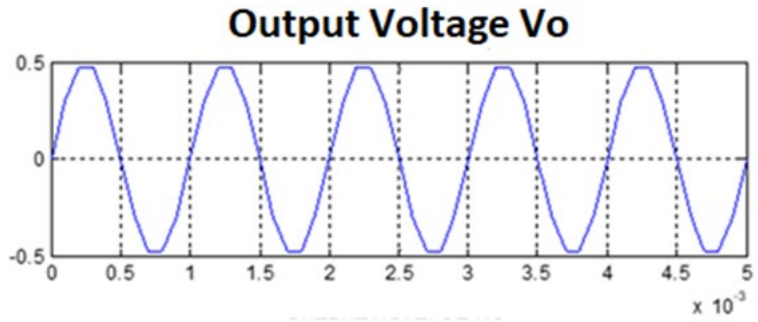
INPUT SINE WAVE



OUTPUT SINE WAVE = ?

Plot the input and output voltage graph from CRO and observe the 0 degrees phase shift (no phase shift) and unity gain





QUESTIONS FOR VIVA-VOCE IN LESSONS 1A, 1B, 1C (Answers are given in a separate file)

1. What is an Operational Amplifier?
2. What are the ideal characteristics of an Operational amplifier?
3. What is meant by CMRR?

4. What is meant by Slew rate?
5. What is meant by maximum output swing?
6. What is meant by Inverting operational amplifier?
7. What is the gain of Inverting operational amplifier?
8. What is meant by Non-Inverting operational amplifier?
9. What is the gain of Non-Inverting operational amplifier?
10. What is meant by voltage follower with op-amp?
11. What is the gain of voltage follower with op-amp?
12. List the applications of voltage follower with op-amp

EXPERIMENT NO 2A:

ADDER USING OP-AMP

In this lesion we will be using the following properties:-

1) **OP AMP PROPERTIES:-**

a)The impedance of inputs (positive and negative terminals) are ideally infinite (very large)

b)The current that goes into the positive and negative input terminals is zero (very small)

c) The voltage between positive and negative input terminal is zero

2) Kirchhoff's current law:-

This **law** states that, for any node (junction) in an electrical circuit, the sum of currents flowing into that node is equal to the sum of currents flowing out of that node.

EXPERIMENT NO 2A:

ADDER/ SUMMING AMPLIFIER USING OP-AMP

A. INVERTING ADDER/SUMMER

AIM: To design and setup a summing amplifier (adder) circuit with OP AMP 741C for a gain of 2 and verify the output**.**

OBJECTIVES: After completion of this experiment, student will be able to design and setup a summing amplifier using OP AMP

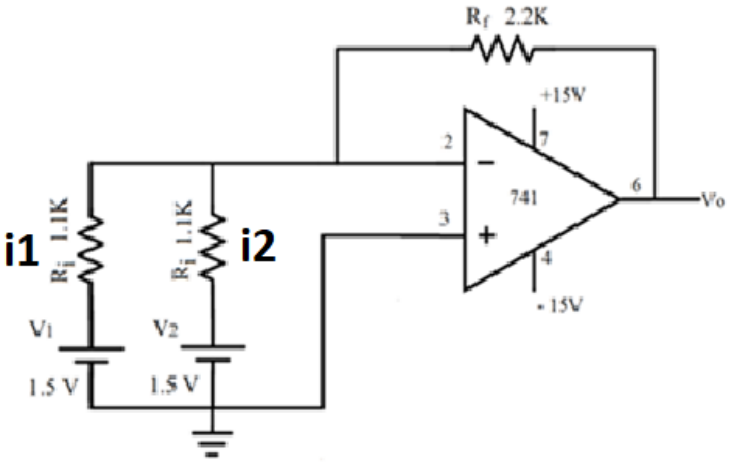
EQUIPMENT/COMPONENTS REQUIRED

Sl.No.	Name and Specification	Quantity
1	Dual power supply +/− 15 V	1
2	Function Generator (0–1 MHz)	1
3	Oscilloscope (10 MHz)	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors	3
7	Probes and Connecting wires	As required
8	Multimeter	1
9	Variable power supplies	2

PRINCIPLE:

Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder . Summing amplifier can be classified as inverting & non-inverting summer depending on the input applied to inverting or non-inverting terminals respectively. Circuit Diagram shows an inverting summing amplifier with 2 inputs.

Here the output will be amplified version of the sum of the two input voltages with 180 degree phase reversal.



Voltage at terminal 2 and 3 are same (virtual ground)

$$i1 + i2 = If$$

$$\frac{V1}{Ri} + \frac{V2}{Ri} = \frac{0 - Vo}{Rf}$$

$$\frac{V1 + V2}{Ri} = -\frac{Vo}{Rf}$$

$$Vo = -\frac{Rf}{Ri}\,(V1 + V2)$$

DESIGN:

The output voltage of an inverting summing amplifier is given by

$$V0 = -\frac{R_f}{R_i}\,(V1 + V2)$$

Let Ri = 1.1KΩ

Then Rf = 2.2KΩ

Then Vo = –2 (V1+V2)

OBSERVATION 1:

PART 1:

V1= 1.5 DC

V2= 1.5 DC

Then Vo=?

Sl.No	V1 (volts)	V2 (volts)	Vo(volts) Measured = X	Vo = – 2(V1+V2) = Y	Error Percentage 100(X– Y)/Y
1	0.25 v	0.5v		– 1.5 V	
2	0.5v	0.75v			
3	0.75v	1.0v			
4	1.0v	0.25			
5	1.5	1,5			
6	2.5	2.5			

OBSERVATION 2:

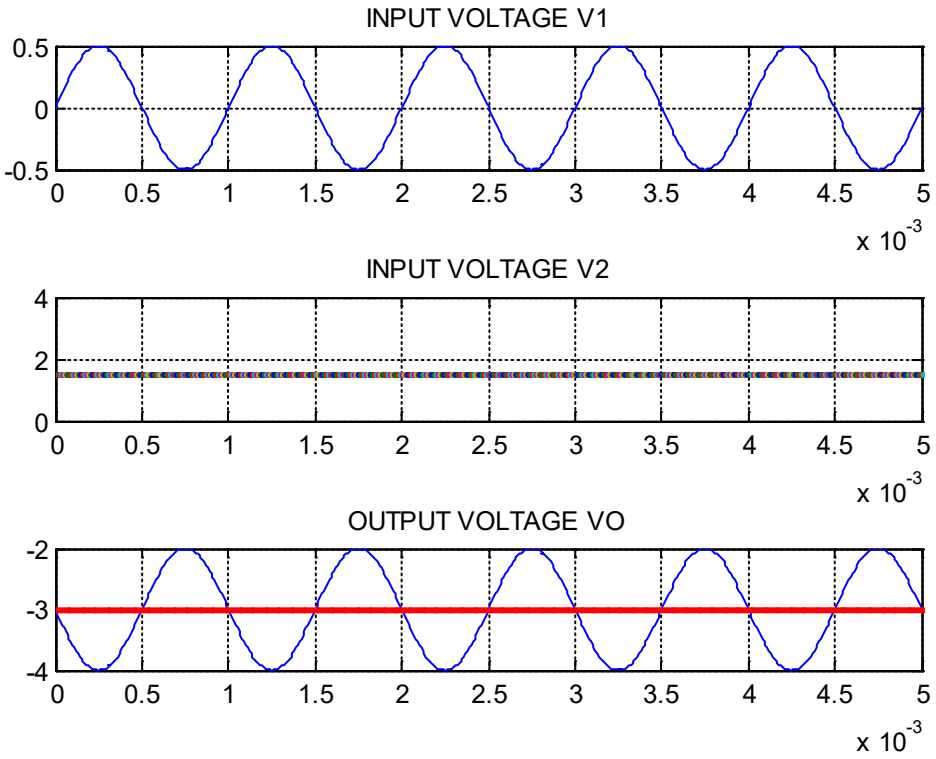
PART 2:

V1= 1Vpp sine wave

V2= 1.5 DC

Then Vo=?

GRAPH: Plot the input and output graph from CRO one below the other and observe the 180 degrees phase shift (reversal of phase)

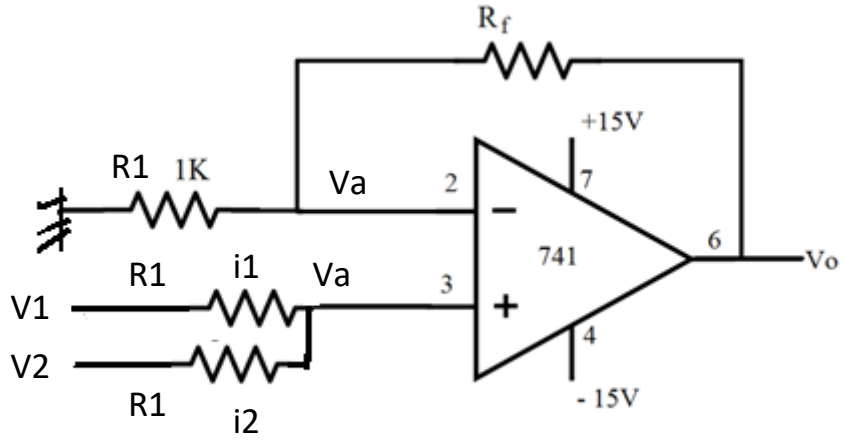


NOTE: THE ABOVE IS AN INVERTING ADDER/SUMMER

B. NON INVERTING SUMMER:

EQUIPMENT/COMPONENTS REQUIRED

Sl.No.	Name and Specification	Quantity
1	Dual power supply +/− 15 V	1
2	Function Generator (0–1 MHz)	1
3	Oscilloscope (10 MHz)	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors	4
7	Probes and Connecting wires	As required
8	Multimeter	1
9	Variable power supplies	2



i1 + i2 =0 (since terminal 3 does not draw any current)

$$\frac{Va - V1}{R1} + \frac{Va - V2}{R1} = 0$$

$$\frac{2Va - (V1 + V2)}{R1} = 0$$

$$Va = \frac{V1 + V2}{2}$$

Using the Non inverting Gain formula

$$G = 1 + \frac{Rf}{R1}$$

$$Vo = Va\,(1 + \frac{Rf}{R1})$$

Let Rf = R1

$$V0 = \frac{V1 + V2}{2}\left(1 + \frac{R1}{R1}\right) = V1 + V2$$

Therefore Output voltage is equal to sum of input voltages

OBSERVATION 1 :

V1= 1.5 DC

V2= 1.5 DC

Then Vo=?

Sl.No	**V1 (volts)**	**V2 (volts)**	**Vo(volts) Measured =X**	**Vo = (V1+V2)= Y**	**Error Percentage 100(X–Y)/Y**

1	0.25 v	0.5v			
2	0.5v	0.75v			
3	0.75v	1.0v			
4	1.0v	0.25			
5	2.5	2.5			
6	5.0	5.0			

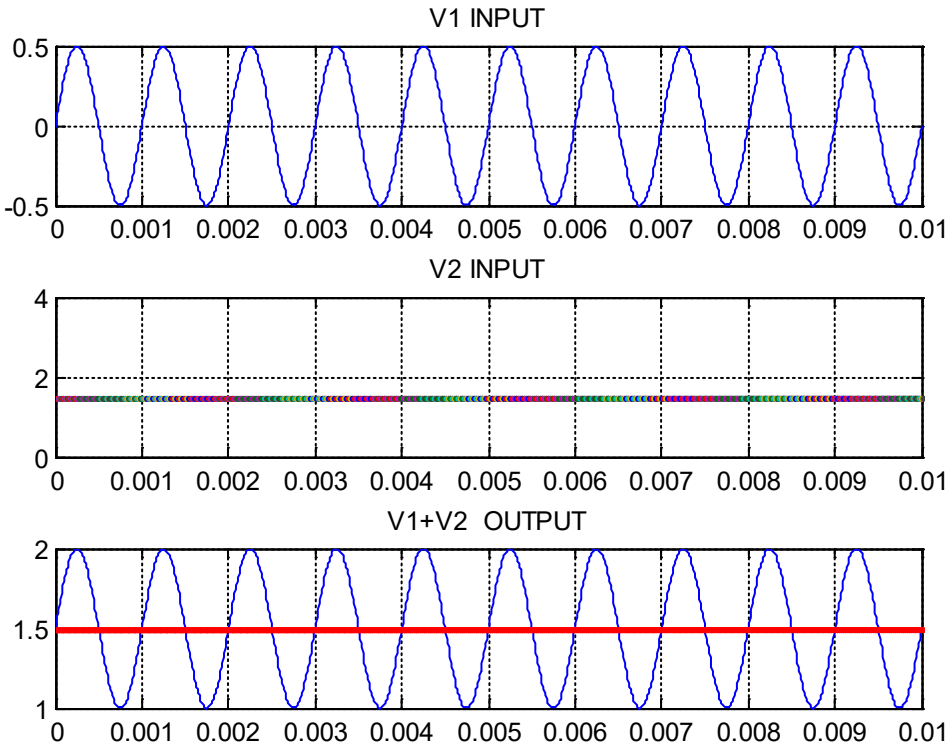
OBSERVATION 2 :

V1= 1Vpp sine wave

V2= 1.5 DC

Then Vo=?

GRAPH: Plot the input and output graph from CRO one below the other and observe the 0 degree phase shift (no phase shift)


V1 INPUT
0.5
0
-0.5
0
0.001
0.002
0.003
0.004
0.005
0.006
0.007
0.008
0.009
0.01
V2 INPUT
4
2
0
0
0.001
0.002
0.003
0.004
0.005
0.006
0.007
0.008
0.009
0.01
V1+V2 OUTPUT
2
1.5
1
0
0.001
0.002
0.003
0.004
0.005
0.006
0.007
0.008
0.009
0.01

EXPERIMENT NO 2B
SUBTRACTOR USING OP-AMP

In this lesion we will be using the following properties:-

1) OP AMP PROPERTIES:-

a)The impedance of inputs (positive and negative terminals) are ideally infinite (very large)
b)The current that goes into the positive and negative input terminals is zero (very small)

2) KIRCHHOFF'S CURRENT LAW:-

This **law** states that, for any node (junction) in an electrical circuit, the sum of currents flowing into that node is equal to the sum of currents flowing out of that node.

3) SUPERPOSITION THEOREM:-

The theorem states that in any linear, active, bilateral network having more than one voltage source, the response across any element is the sum of the responses obtained from each voltage source considered separately and all other voltage sources are replaced by their internal resistance. (for our purpose we assume internal resistance of voltage source is zero. So we can short the voltage source). The superposition theorem is used to solve the network where two or more sources are present

EXPERIMENT NO 2B
SUBTRACTOR USING OP-AMP

DIFFERENCE AMPLIFIER / SUBTRACTOR

AIM: To design and setup a difference amplifier circuit with OPAMP IC 741C for a gain of 2 and verify the output.

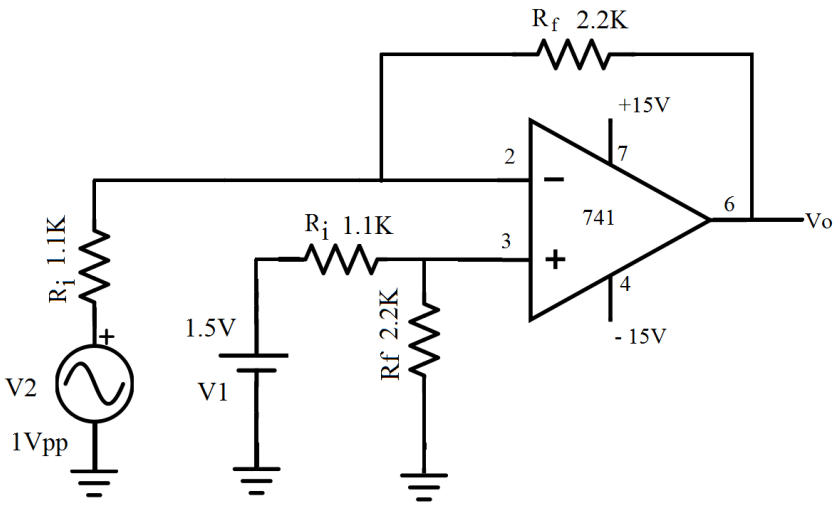
OBJECTIVES: After completion of this experiment, student will be able to design and setup a difference amplifier using OP AMP.

PRINCIPLE:

A difference amplifier is a circuit that gives the amplified version of the difference of the two inputs, Vo =A(V1–V2), where V1 and V2 are the inputs and A is the voltage gain.

Here input voltage V1 is connected to non-inverting terminal and V2 to the inverting terminal. This is also called as differential amplifier.

Output of a differential amplifier can be determined using super position theorem.



SUPERPOSITION THEOREM:

Follow these steps in order to find the response in a particular branch using superposition theorem.

STEP 1 − Find the response in a particular branch by considering one independent source and eliminating the remaining independent sources present in the network. We can eliminate the voltage sources by shorting their two terminals and similarly, the current sources by opening their two terminals.

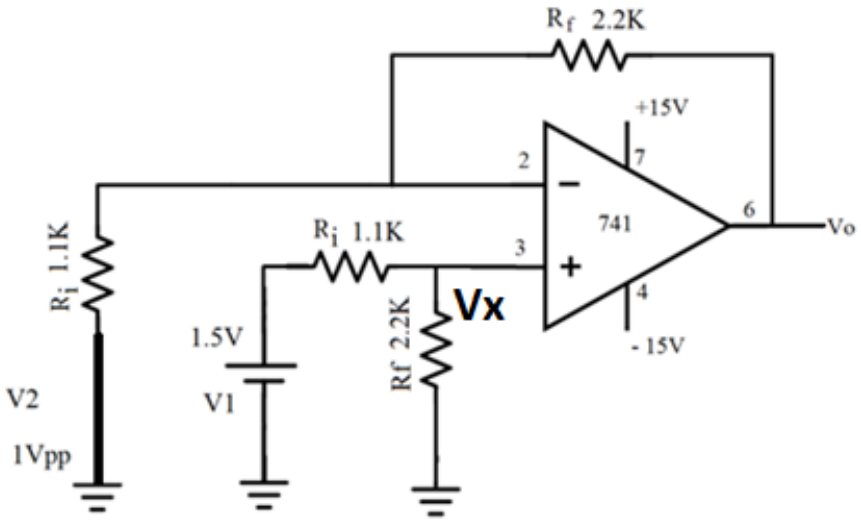
STEP 2 − Repeat Step 1 for all independent sources present in the network.

STEP 3 − Add all the responses in order to get the overall response in a particular branch when all independent sources are present in the network.

STEP NO.1: (Short V2) When V2=0, the circuit become a non-inverting amplifier with input V1

Let voltage at terminal 3(non-inverting terminal) = Vx

The resulting output is



$$V01 = Vx\,(1 + \frac{Rf}{Ri})$$

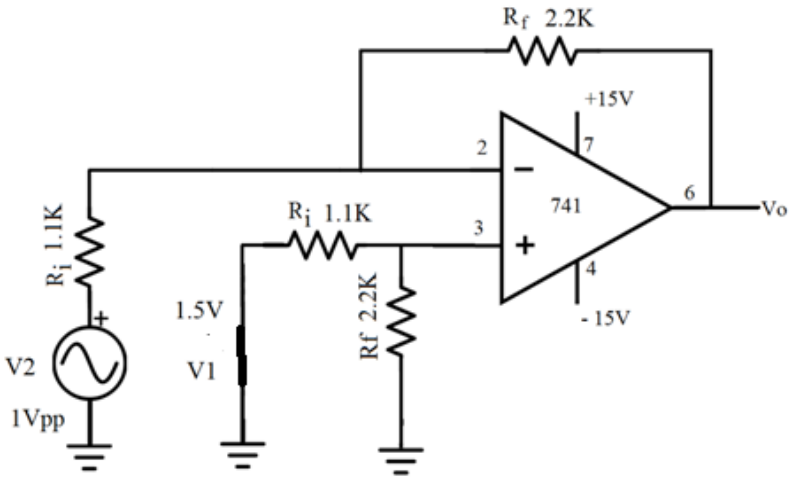
Voltage at terminal 3 (Non inverting) = (it is a voltage divider)

$$Vx = \frac{V1\ \ Rf}{Ri + Rf}$$

Output voltage V01

$$V01 = \frac{V1\ \ Rf}{Ri + Rf}\left[1 + \frac{Rf}{Ri}\right] = \frac{V1\ \ Rf}{\cancel{Ri + Rf}}\ \frac{\cancel{Ri + Rf}}{Ri}$$

$$V01 = V1\ \frac{Rf}{Ri}$$



STEP NO.2: (Short V1) When V1=0, the circuit becomes an inverting amplifier with input V2

Let the voltage at terminal 2 (inverting terminal) is Vy

But Vy = 0 because voltage at terminal 3 (noninverting terminal) is zero

$$\frac{\mathrm{V2}-\mathrm{Vy}}{Ri}=\frac{\mathrm{V}y-\mathrm{Vo2}}{Rf}$$

$$\frac{V2}{Ri}=-\frac{Vo2}{Rf}$$

since Vy = 0

$$Vo2=\ -V2\ \frac{Rf}{R1}$$

STEP NO. 3 : Therefore the resulting output according to super position theorem is Add V01 and V02

Vo = V01+ V02 =

$$\mathrm{Vo}=\mathrm{V1}\ \frac{\mathrm{Rf}}{\mathrm{R1}}-\mathrm{V2}\ \frac{\mathrm{Rf}}{\mathrm{R1}}$$

$$V0=\ \frac{Rf}{R1}\ (V1-V2)$$

So this is a Difference equation

DESIGN:

Let Ri = 1.1KΩ

Rf = 2.2KΩ the gain = $\frac{R_f}{R_i}$ = 2

Vo = V01+ V02 =

$$\frac{Rf}{Ri}(V1 - V2)$$

V0 =2 (V1 – V2)

OBSERVATION 1:

PART 1:

V1= 1.5 DC
V2= 1.5 DC
Then Vo=?

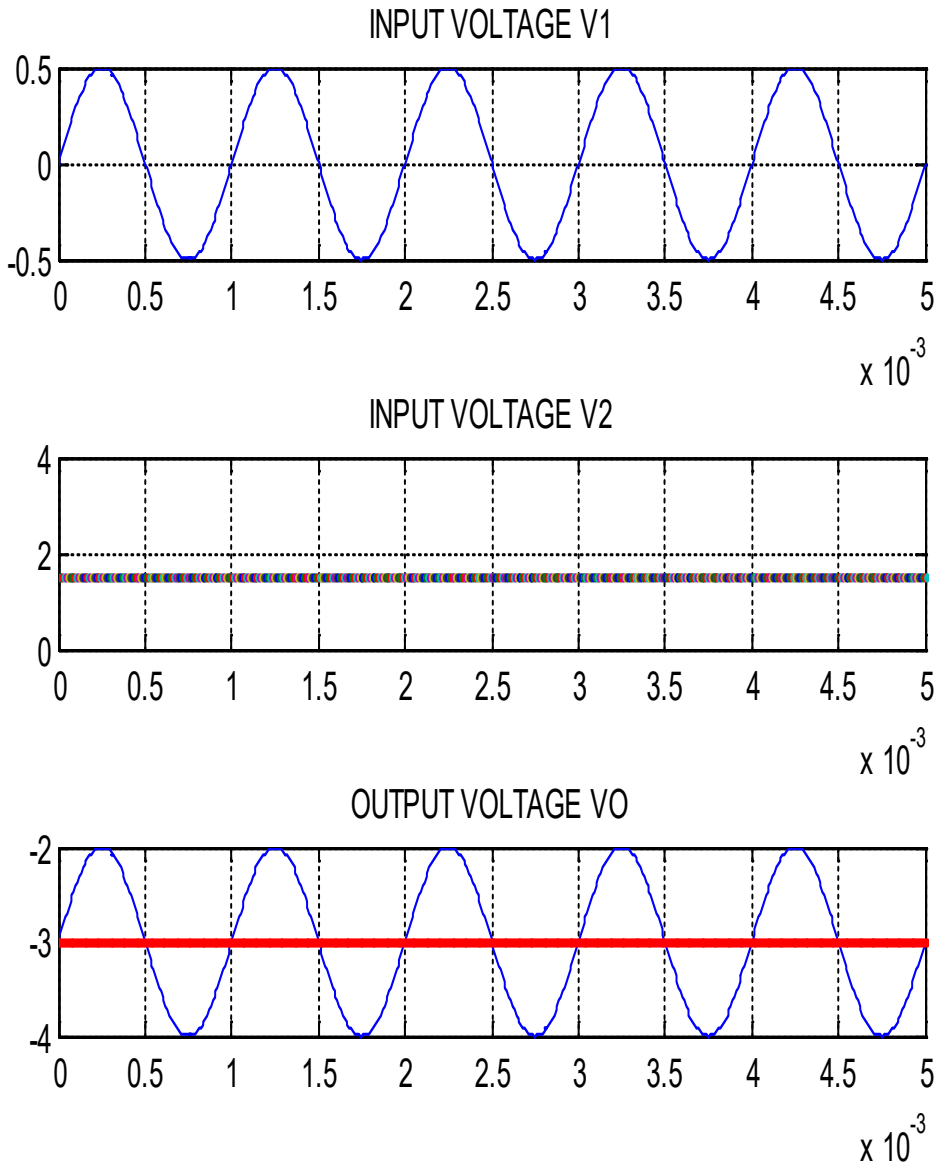
Sl.No	V1 (volts)	V2 (volts)	Vo(volts) Measured =X	Vo = 2(V1–V2) = y	Error Percentage 100(X–Y)/y
1	0.25 v	0.5v			
2	0.5v	0.75v			
3	0.75v	1.0v			
4	1.0v	0.25			

OBSERVATION 2:

PART 2:

V1= 1Vpp sine wave
V2= + 1.5 DC
Then Vo=?

GRAPH: Plot the input and output graph from CRO one below the other and observe the phase shift in sine wave



QUESTIONS FOR VIVA-VOCE IN LESSONS 2A, 2B, (Answers are given in a separate file)

1. Draw the circuit diagram of a 3 input Adder
2. What is the other name for adder?
3. Draw the circuit diagram for subtractor

EXPERIMENT NO.3:
COMPARATOR USING OP-AMP

AIM: To design and setup a Non inverting comparator with Op Amp 741C , plot waveforms for a sinewave input, observe the output waveform and plot it.

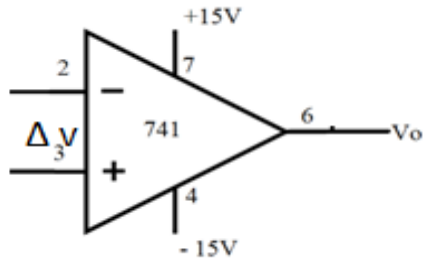
OBJECTIVES : After completion of the experiment student should be able to design and setup a Non inverting comparator

EQUIPMENT & COMPONENTS

Sl.No.	Name and Specification	Quantity
1	Dual power supply +/— 15 V	1
2	Function Generator (0–1 MHz)	1
3	Oscilloscope (10 MHz)	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors	3
7	Diodes	2
8	Potentiometer	1
9	Probes and Connecting wires	As required
10	Multimeter	1
11	Variable power supplies	2

THEORY BEHIND THE DESIGN:

1) SATURATION PHENOMENA:



$V_o = —\Delta v \times G$

$\Delta v = -\frac{V_o}{G}$ when G is large

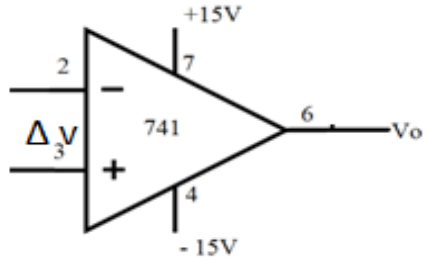
Let $G = 10^5$ and Δv (offset voltage) = + .01 v

V_o =— (+.01) x 10^5 = — 1000 V

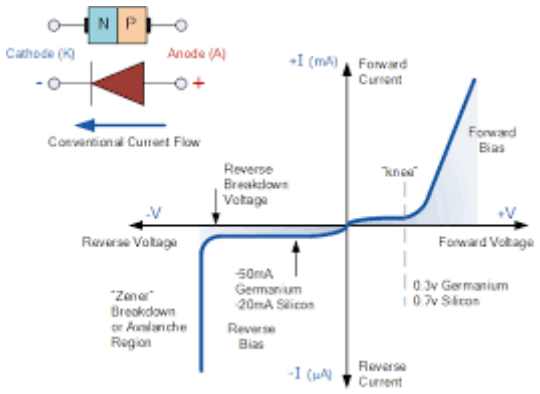
Since the power supplies are only +/— 15 the op amp saturates at —12V (15—3v)

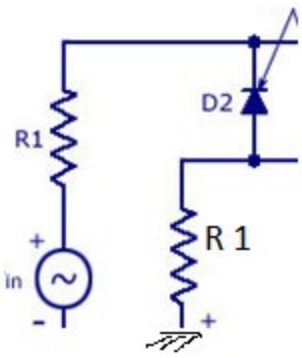
Similarly when Δv =—.01v the op amp saturates at +12 V (15—3)

2) PROTECTION OF OP AMP BY DIODES



When voltage between +ve and – ve terminal exceeds +/ - 5 volts the Op amp gets damaged. To protect we use diodes between +v and – ve terminals. For large variations in current flowing in diode the voltage drop across the diode remain constant





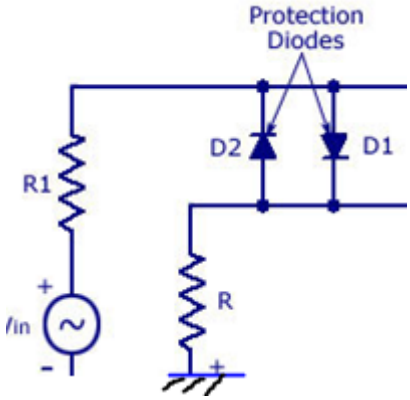
a)Let V1 = 5 v and R1= 10 k

Current in the diode = 5 / (10+10) k = 0.25 X 10^{-3} amp. Drop across diode = 0.7 v

b)Let V1 =10 v and R1= 10 k

Current in the diode = 10 / (10+10) k = 0.5 X 10^{-3} amp. Drop across diode = 0.7 v

Reverse also is also true



WHAT IS A COMPARATOR?

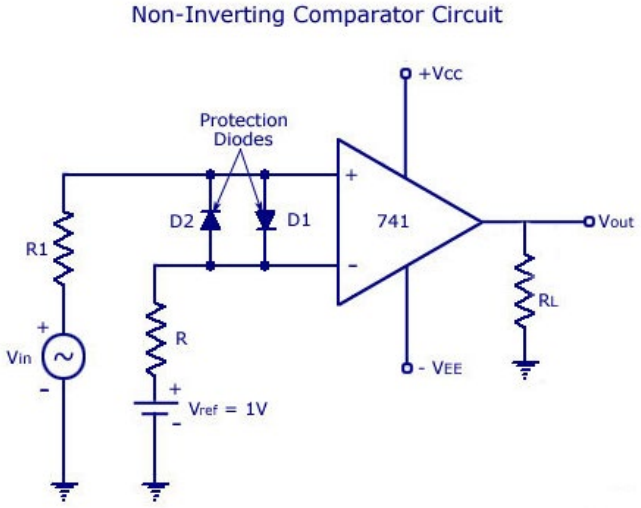
A comparator finds its importance in circuits where two voltage signals are to be compared and to be distinguished which is stronger.

- An op-amp operating in open loop configuration will have an output that goes to positive saturation or negative saturation level . The 2 inputs, out of which one is a reference voltage (Vref) is compared with each other.
- A non-inverting 741 IC op-amp comparator circuit is shown in the figure below. It is called a non-inverting comparator circuit as the sinusoidal input signal Vin is applied to the non-inverting terminal.
- The fixed reference voltage Vref is given to the inverting terminal (—) of the op-amp.
- When the value of the input voltage Vin is greater than the reference voltage Vref the output voltage Vo goes to positive saturation. This is because the voltage at the non-inverting input is greater than the voltage at the inverting input.
- When the value of the input voltage Vin is lesser than the reference voltage Vref, the output voltage Vo goes to negative saturation. This is

because the voltage at the non-inverting input is smaller than the voltage at the inverting input.

- Thus, output voltage Vo changes from positive saturation point to negative saturation point whenever the difference between Vin and Vref changes. This is shown in the waveform below. The comparator can be called a voltage level detector, as for a fixed value of Vref, the voltage level of Vin can be detected.

- The circuit diagram shows the diodes D1and D2. These two diodes are used to protect the op-amp from damage due to increase in input voltage. These diodes are called clamp diodes as they clamp the differential input voltages to either 0.7V or −0.7V.
- Resistance R1 is connected in series with input voltage Vin and R is connected between the inverting input and reference voltage Vref. R1 limits the current through the clamp diodes and R reduces the offset problem.



-

PROCEDURE:

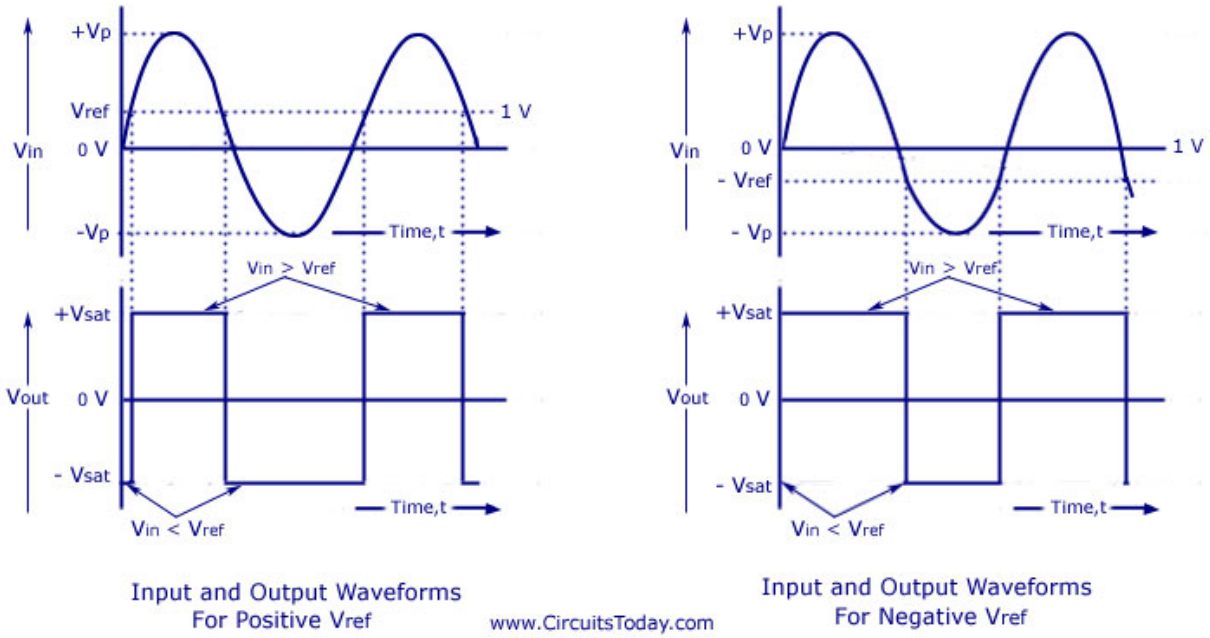
EXPERIMENT NO.1

Sl.no	Reference	vin	ΔV= Vin −Ref	Theoretical Vo	Measured Vo
1	1.0 v	0.2 v	—0.8v	—12v	
2	1.0 v	0.5 v	—0.5v	—12v	
3	1.0 v	1.1 v	+ 0.1v	+ 12v	

4	1.0 v	1.2 v	+ 0.2v	+ 12v	

EXPERIMENT No. 2:

1. Connect the components and power supply
2. Apply 1 KHz sine wave with 5 V peak to peak at the Vin terminal
3. Connect input to channel 1 and output to channel 2 of Oscilloscope
4. Observe the waveforms and note down the amplitude and time periods
5. Overlap the two waveforms and note down the voltages at position on sine wave where the output changes its state These voltages denote the reference voltage

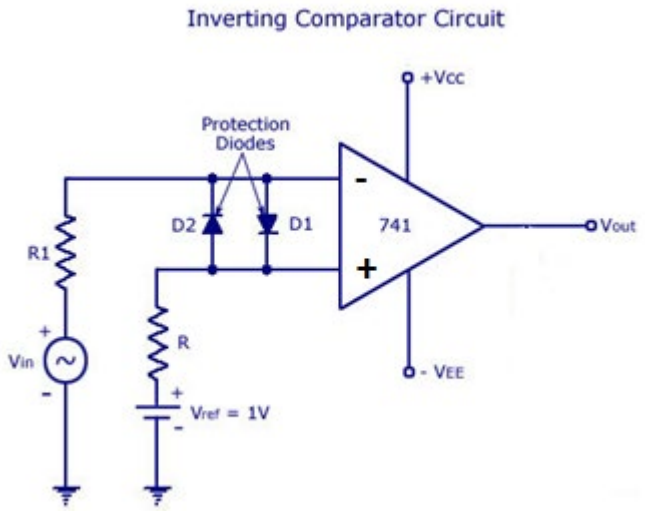


INVERTING 741 IC OP-AMP COMPARATOR CIRCUIT

➢ An inverting 741 IC op-amp comparator circuit is shown in the figure below. It is called an inverting comparator circuit as the sinusoidal input signal Vin is applied to the inverting terminal.

➢ The fixed reference voltage Vref is given to the non-inverting terminal (+) of the op-amp. A potentiometer is used as a voltage divider circuit to obtain the reference voltage in the non-inverting input terminal.(or a fixed

voltage may be used). Both the ends of the POT are connected to the dc supply voltage +VCC and —VEE. The wiper is connected to the non-inverting input terminal. When the wiper is rotated to a value near +VCC, Vref becomes more positive, and when the wiper is rotated towards -VEE, the value of Vref becomes more negative. The waveforms are shown below.

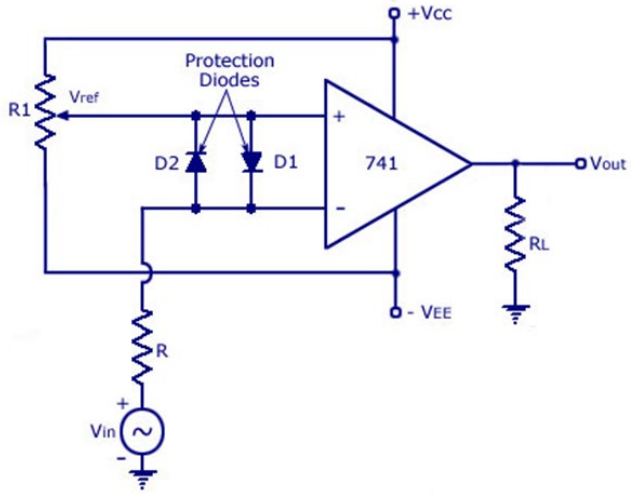


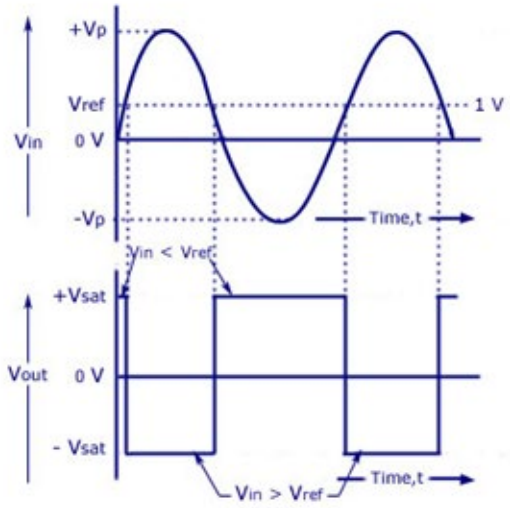
EXPERIMENT NO.1

Sl.no	Reference	vin	ΔV Vin —Ref	Theoretical Vo	Measured Vo
1	1.0 v	0.2 v	—0.8v	+ 12v	
2	1.0 v	0.5 v	—0.5v	+ 12v	
3	1.0 v	1.1 v	+ 0.1v	—12 v	
4	1.0 v	1.2 v	+ 0.2v	—12v	

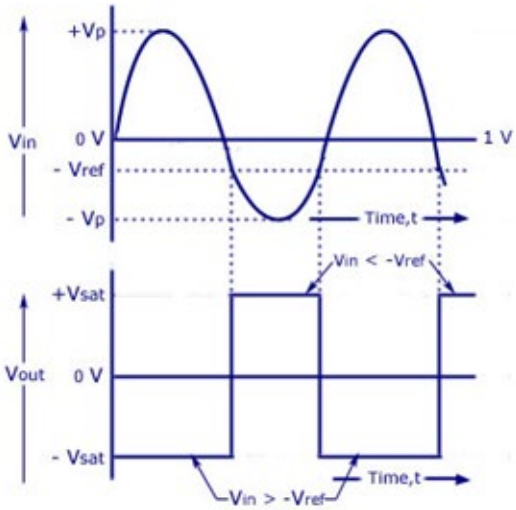
EXPERIMENT NO.2

Inverting Comparator Circuit





Input and Output Waveforms
For Positive Vref



Input and Output Waveforms
For Negative Vref

QUESTIONS FOR VIVA-VOCE IN LESSON 3 (Answers are given in a separate file)

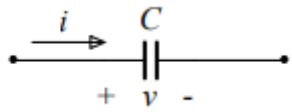
1. How many basic input parameters are required for the comparator?
2. Draw the circuit diagram of inverting and noninverting comparator
3. What is the output of a inverting and noninverting comparator if the input is sinusoidal

4. What are the differences between the inverting and noninverting comparators ?
5. What is the name of the comparator if the reference voltage is zero ?
6.Draw the circuit diagram and output wave form of inverting and noninverting zero crossing detectors
7. Discuss the characteristics of an ideal comparator.
8. List the different types of comparators.
9. What is the meaning of voltage limiting?
10. What is zero crossing detector?
11. What are the applications of comparator?
12. In which mode the operational amplifier is connected in the comparator

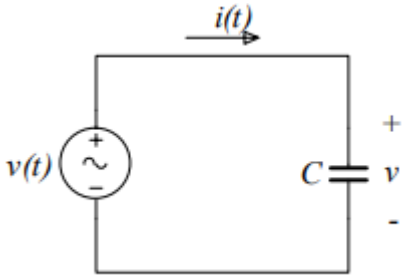
EXPERIMENT N0.4
INTEGRATOR CIRCUIT USING IC 741

INTRODUCTION:

Voltage current relationship in a Capacitor:



$$i = C\frac{dv}{dt}$$



For DC (constant in Time) $\frac{\mathrm{dv}}{\mathrm{dt}} = 0$

But i = C$\frac{\mathrm{dv}}{\mathrm{dt}}$ = C x 0 = 0 (no current flows means high impedance)

So capacitor acts as an open circuit for DC (frequency = 0)

$$\mathrm{i} = \mathrm{C}\frac{\mathrm{dv}}{\mathrm{dt}}$$

Integrate the above with respect to time 't'

$$\int i\,dt = \int \mathrm{C}\frac{\mathrm{dv}}{\mathrm{dt}}\mathrm{dt}$$

$$\int i\,dt = \mathrm{C\,V}$$

$$\mathrm{V} = \frac{1}{C}\int i\,dt + \mathrm{v(0)}$$

v(o) represents the voltage at the time =0 and is called the initial condition)

For our analysis we will assume v(o) to be zero

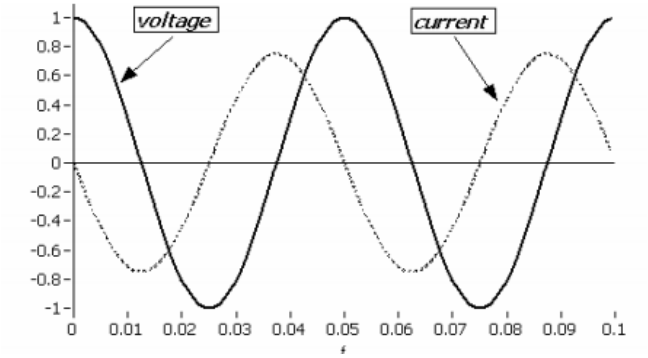
Let V(t) = cos ωt

But i (t) $= C\frac{dv}{dt} = C\frac{d(\cos \omega t)}{dt}$

$= -C\omega \sin \omega t$

$= C\omega \cos(\omega t + \pi/2)$

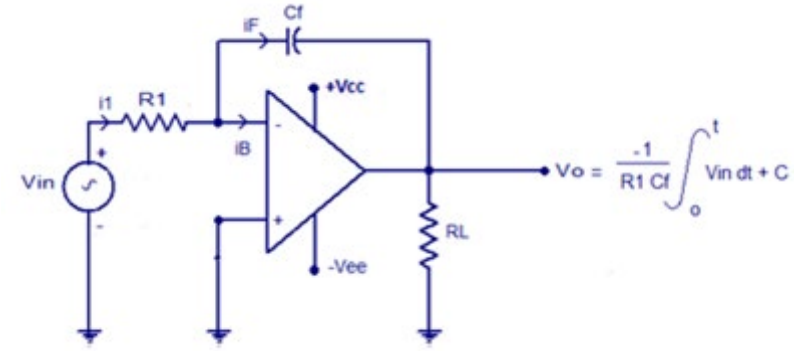
Therefore current through a Capacitor and voltage across a capacitor are 90^0 out of phase. Current leads the voltage by 90^0



THE IDEAL INTEGRATOR:

$V = \frac{1}{C}\int i\, dt$

A circuit in which the output is the integral of current is called INTEGRATOR. Integrator is obtained by replacing the feedback resistor in a Inverting op amp circuit with a Capacitor



Let at node B (–ve teriminal) voltage is v_x

From Kirchhoff 's law $I_1 = I_f$

Relationship between current and voltage across a capacitor is

$I_c = C \frac{dv_c}{dt}$

$$\frac{v_{in} - v_x}{R1} = C \frac{d}{dt}(v_x - v_o)$$

But v_x =0 (Voltage between + ve and – ve teriminal is zero)

$$\frac{vin}{R1} = C \frac{d}{dt}(-vo)$$

Integrating both sides with respects to time

$$\int_0^t \frac{v_{in}}{R_1} dt = \int_0^t C \frac{d}{dt}(-v_o)$$

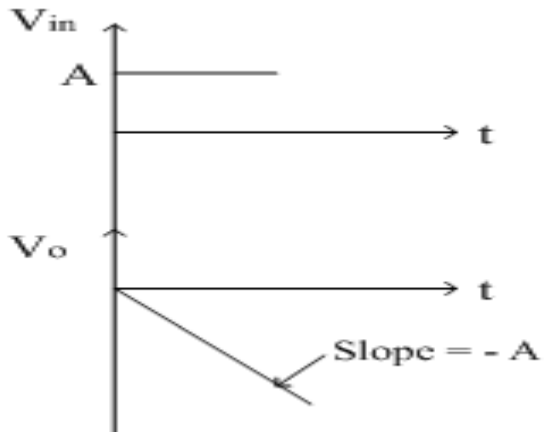
(Assume initial condition as zero)

$$\int_0^t \frac{v_{in}}{R_1} dt = C (-v_o)$$

$$v_o = -\frac{1}{R_1 C}\int_0^t v_{in} dt$$

1. VIN = STEP Y

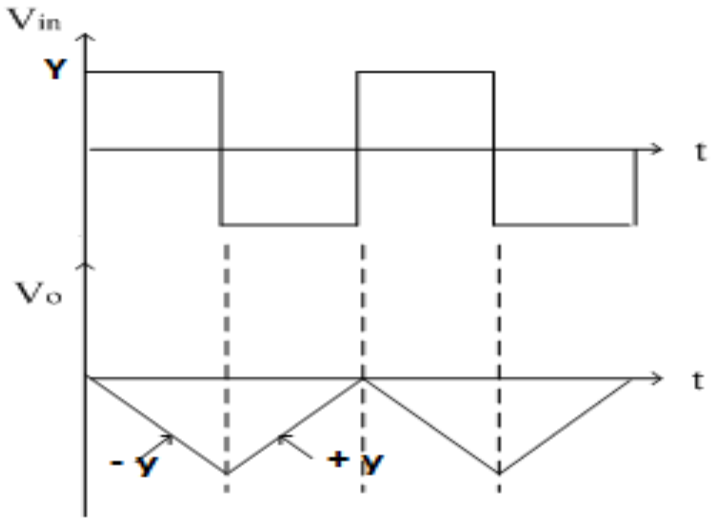
Thus for the positive step signal, output is a negative ramp signal with slope(– Y/RC). After a particular't', integrator goes into negative saturation, so continuous dc signal is avoided for integrator. The input and output waveform is shown below.



2. VIN = SQUARE WAVE

The square wave is nothing but combination of positive and negative step signals. As seen in first case, the output of step signal is a ramp signal. For positive step signal, a negative ramp and for negative step signal, a positive ramp is obtained because it is inverting integrator.

Thus for a square wave input, the output obtained is a triangular waveform as shown in figure below.



3)VIN = SINE WAVE

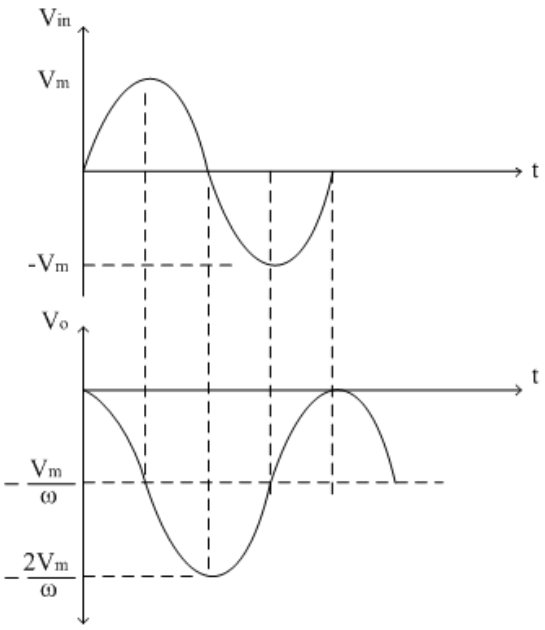
Let$V_{in} = V_m \sin \omega t$

$$V_o = -\frac{1}{RC}\int V_{in}dt$$

$$\therefore V_o = -\frac{1}{RC}\int V_m \sin\omega t dt$$

$$\therefore V = -\frac{V_m}{RC}\int V_m \sin\omega t dt$$

$$\therefore V_o = -\frac{V_m}{RC}\left[\frac{-\cos\omega t}{\omega}\right]$$



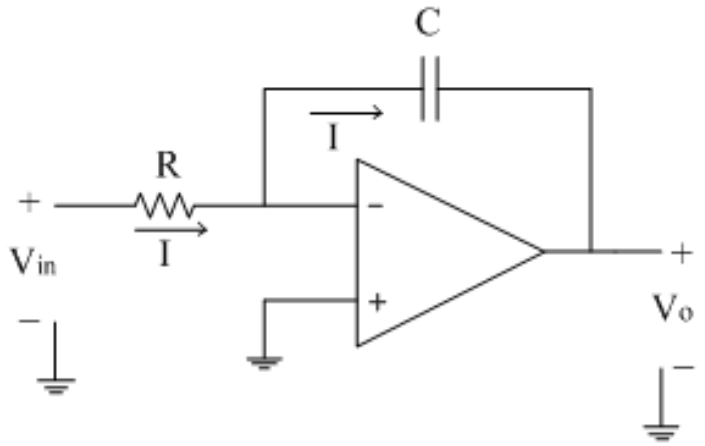
FREQUENCY RESPONSE OF IDEAL INTEGRATOR:

Ac circuits operates at different frequencies

ω = 2 π f (ω = radians /sec and f= cycles /sec =Hz)

Sl.no	Element	Impedance
1	Resistor	R
2	Inductance	JωL

3	Capicitor	$\frac{1}{J\omega\ C}$
4	Resistor + Inductor	R+ JωL
5	Resistor + Capacitor	$R + \frac{1}{J\omega C}$
6	Resistor+ Inductor + Capacitor	$R + J\omega L + \frac{1}{J\omega\ C}$



Gain = $\frac{Feed\ back\ impedance}{Input\ impedance}$

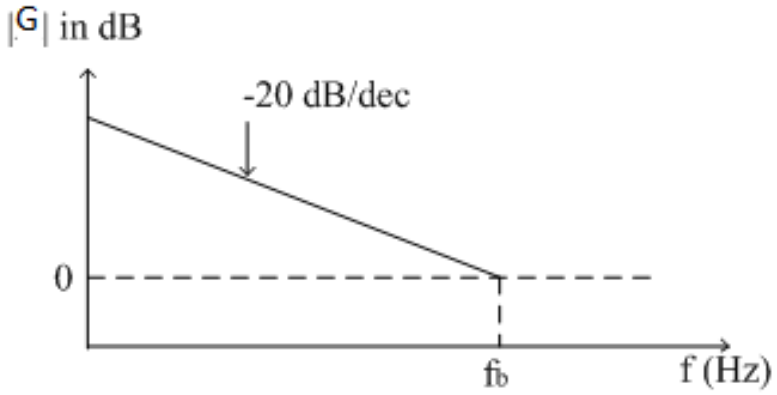
$$G = -\frac{\frac{1}{J\ \omega\ C}}{R} = -\frac{1}{J\ \omega\ C\ R} = -\frac{1}{J\ 2\pi\ f\ C\ R}$$

G = a+ Jb Magnitude |G| = $\sqrt{a^2 + b^2}$

So |G|= $\frac{1}{\sqrt{0^2+(2\ \pi\ f\ C\ R\ )^{\ 2}}} = \frac{1}{2\ \pi\ f\ C\ R}$

f = fb is frequency at which gain of the op-amp becomes unity (=1) i.e. o dB. Thus gain drops to 0 dB at a frequency **f=fb**, from its very high value at

low frequencies. The frequency response of ideal integrator is shown below

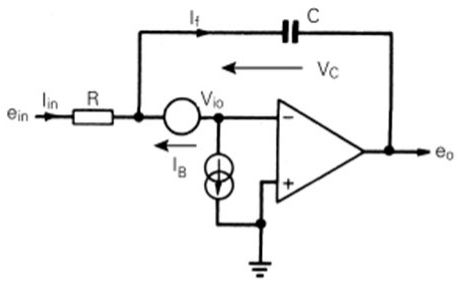


DRAWBACKS IN IDEAL INTEGRATOR:

1. Bandwidth is very small and used for only small range of input frequencies.
2. For dc input (f = 0), reactance of capacitance, Xc is infinite. Because of this op-amp goes into open loop configuration.In open loop configuration the gain is infinite and hence the small input offset voltages are also amplified and appears at output as error. This is referred as false triggering and must be avoided.

Due to all such limitations, an ideal integrator needs to be modified. Some additional components are used along with ideal integrator circuit to reduce the effect of an error voltage in practice. This modified integrator is referred as practical integrator.

Integrator errors:



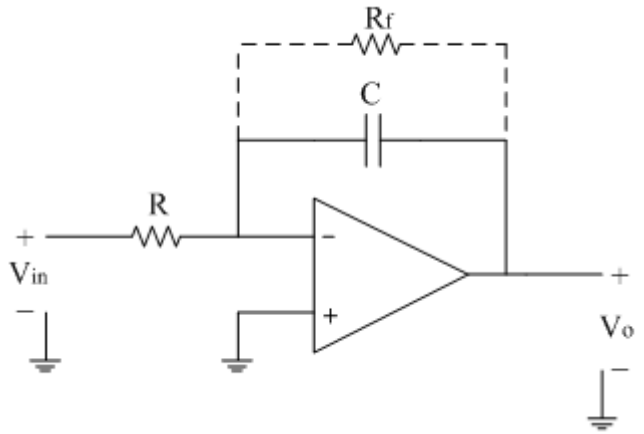
Equivalent circuit used for estimating error due to input offset voltage and bias current

$$e_o = -\frac{1}{CR}\int e_{in}\,dt + \frac{1}{CR}\int V_{io}\,dt + \frac{1}{C}\int I_B\,dt + V_{io}$$

PRACTICAL INTEGRATOR

The limitations of an ideal integrator can be minimized in the practical circuit by adding resistor Rf in parallel with capacitor C this Rf avoids op-amp going into open loop configuration at low frequencies.

The practical integrator circuit is shown below.



FREQUENCY RESPONSE OF PRACTICAL INTEGRATOR:

The voltage gain 'A' is given by the equation as follows,

$$A = \frac{R_f \| X_c}{R}$$

$$\therefore\ A = \frac{\left[\dfrac{R_f \times \dfrac{1}{j\omega C}}{R_f + \dfrac{1}{j\omega C}}\right]}{R}$$

$$\therefore\ A = \frac{\left[\dfrac{R_f}{j\omega C R_f + 1}\right]}{R}$$

$$\therefore\ A = \frac{R_f}{R(j\omega C R_f + 1)}$$

$$\therefore\ A = \frac{R_f}{R}\left[\frac{1}{(j2\pi f C R_f + 1)}\right]$$

Let $f_a=1/(2\pi R_f C)$ =Break frequency or Corner frequency

$$A=\frac{R_f}{R}\left[\frac{1}{1+\ j\left(\frac{f}{f_a}\right)}\right]$$

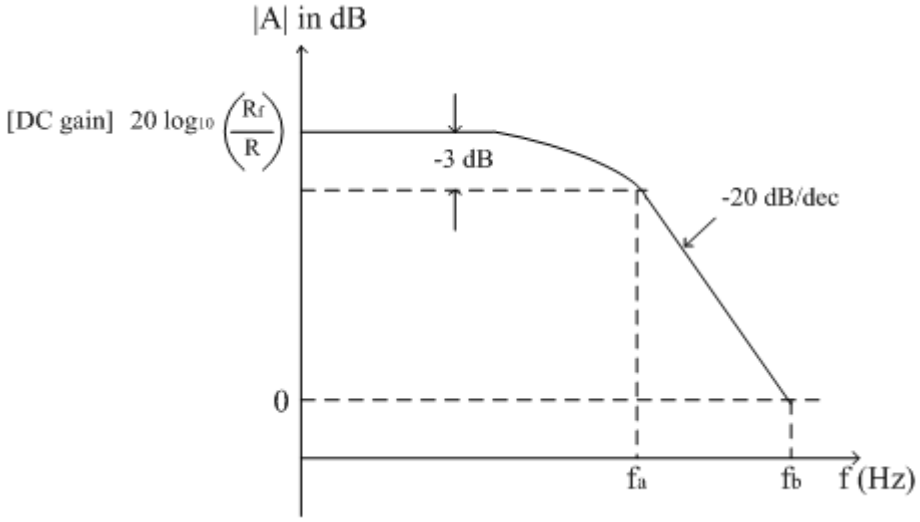
Where f=Operating frequency
The magnitude of gain A is,

$$|A|=\left|\frac{R_f}{R}\left[\frac{1}{1+\ j\left(\frac{f}{f_a}\right)}\right]\right|$$

$$|A|=\left|\frac{R_f}{R}\left[\frac{1}{\sqrt{1+\ \left(\frac{f}{f_a}\right)^2}}\right]\right|$$

Consider the following cases:
1. When f=0 ,the gain $|A|=|R_f/R|$=dc gain
2. When $0<f<f_a$,the gain $|A|\cong|R_f/R|$
3. When $f>f_a$,the gain $|A|\ll|R_f/R|$
4. When $f= f_a$, the gain $|A|=|R_f/R\ (1/\sqrt{2})\ |$ Hence, |
the gain in dB is given as
$20\log|A|=20\log|0.707\ (R_f/R)\ |$
|A| in dB=$20\log(0.707)+20\log(R_f/R)$
|A| in dB=$20\log(R_f/R)$ – 3dB
|A| in dB=DC gain (i.e.maximum gain) – 3dB
Thus the frequency f_a is the frequency at which gain is reduced by 3 dB from its maximum value. Hence frequency f_a is also called as 3dB frequency.
From ideal integrator response, we have defined frequency f_b which is 0dB frequency (or unity gain frequency).

The detailed frequency response of practical integrator is shown in figure below



Between the frequency ranges f_a to f_b the response is highly linear and dropping at the rate of –20dB/decade. Thus the frequency range f_a to f_b referred as true integration range where actual integration of the input signal is possible.

Thus the true integration is possible over the range $f_a<f<f_b$

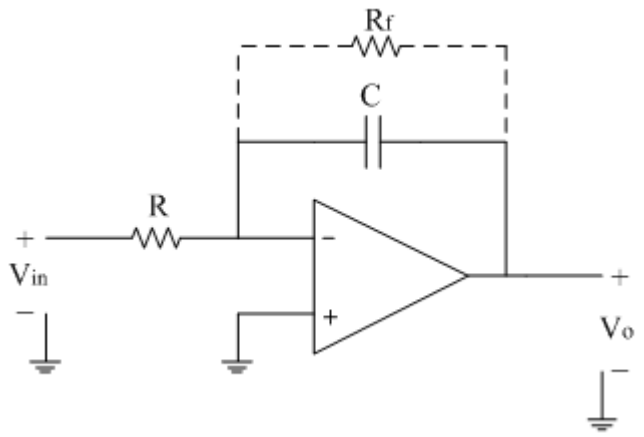
The practical integrator is also called as lossy integrator as it integrates only frequencies greater than f_a (i.e. higher frequencies) effectively.

Thus we can have following observations from frequency response of practical integrator:

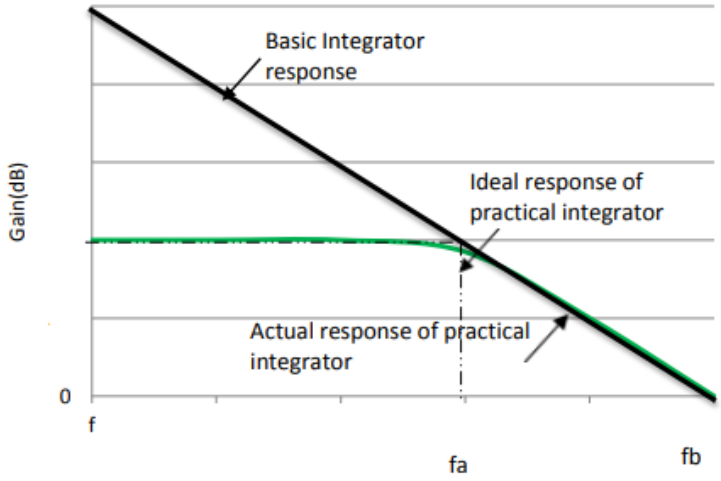
1. Bandwidth of practical integrator is f_a which is higher than BW of an ideal integrator.
2. DC gain (at f=0) is $|R_f/R|$ which is typically ≥10.
3. For better integration $f_b \geq 10 f_a$.
4. For proper integration Time period T of input signal $\geq R_f C$

DESIGN:

Design a practical integrator which works between 1600 Hz and 16000Hz



Frequency Response of basic and practical integrator:



Let C_f= 10 nf =10x 10^{-9} f

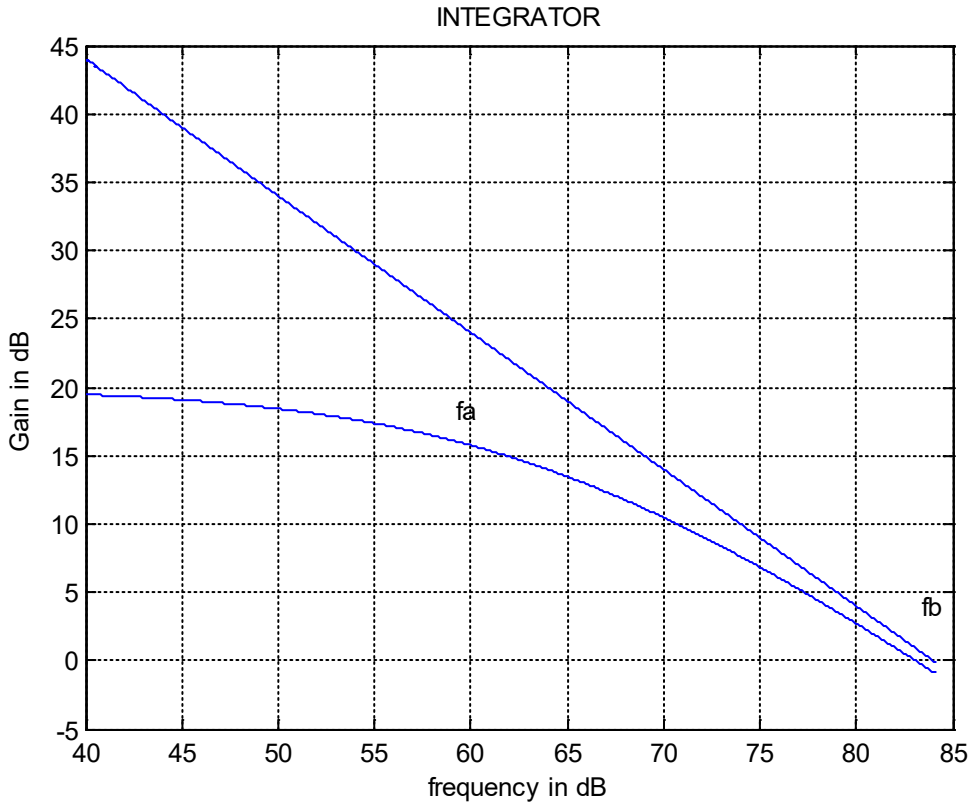
$f_a = 1600 = \frac{1}{2\pi R_f C} = \frac{1}{2\pi R_f \, 10 \times 10^{-9}}$

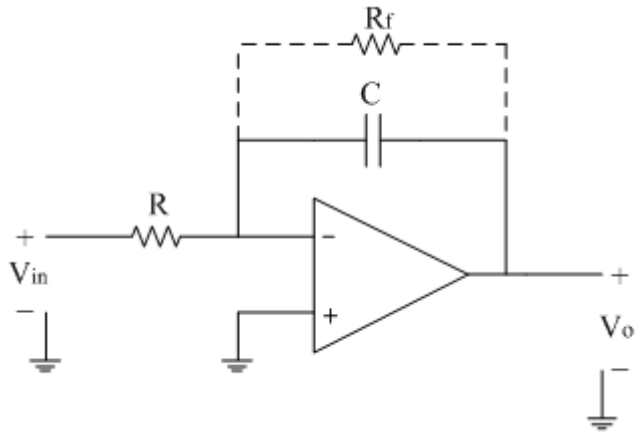
R_f = 9952 = 10 000 =10 Kohm

$f_b = 16000 = \frac{1}{2\pi R C} = \frac{1}{2\pi \times R \times 10 \times 10^{-9}}$

R = 995 = 1000 =1 Kohm

MATLAB SIMULATION WITH ABOVE VALUES





DESIGN INTEGRATOR:

R = 10 Kohm R_f= 100Kohm C =10 nf

$$f_a = \frac{1}{2\,\pi\,R_f\,C}$$

the frequency at which the gain is -3 dB.

$f_a = \frac{1}{2 \times \pi \times 100 \times 10^3 \times 10 \times 10^{-9}} = 159.2$ Hz

f_b: Gain limiting frequency,

$f_b = \frac{1}{2 \times \pi \times 10 \times 10^3 \times 10 \times 10^{-9}} = 1590$ Hz

i) SINE WAVE:

Input is 1V peak to peak at 5000 Hz

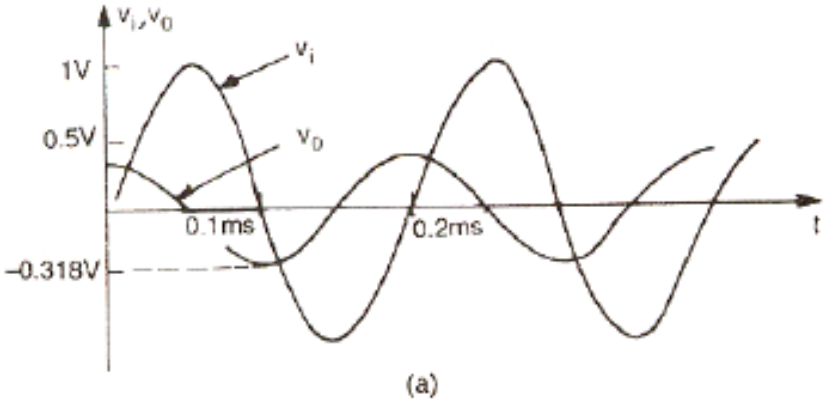
$V_o = -\frac{1}{R\,C}\int v_i\,dt =$

$$-\frac{1}{10 \times 10^3 \times 10 \times 10^{-9}}\int \sin(2 \times 3.14 \times 5000)\,t\,dt$$

$$= -\frac{10^4}{2 \times 3.14 \times 5000}\int -\cos(2 \times 3.14 \times 5000)\,dt$$

= 0.318 cos (2 π 5000t)

Integrator



(a)

ii) STEP INPUT:

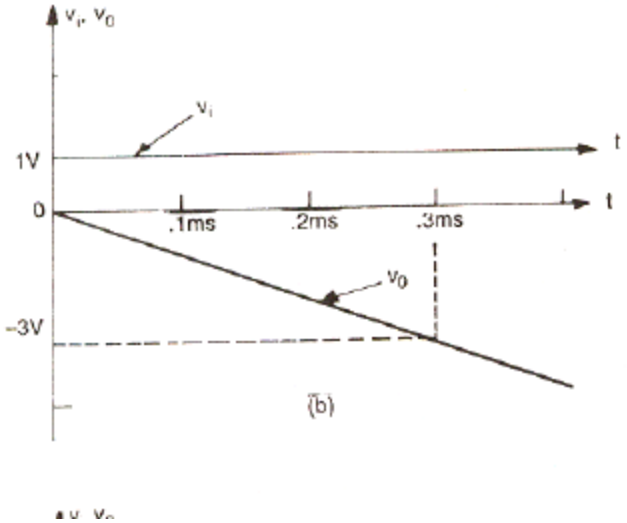
Input is a step voltage v_i= 1 v for 0≤ t ≥0.3 ms

$$Vo = -\frac{1}{R\,C}\int v_i\,dt$$

$$-\frac{1}{10\times 10^{3}\times 10\times 10^{-9}}\int_0^{0.3ms} 1\;dt$$

-10^4x t $|_{t=0}^{t=0.3ms}$= -10^4 x 0.3 x 10^{-3}= −3 v

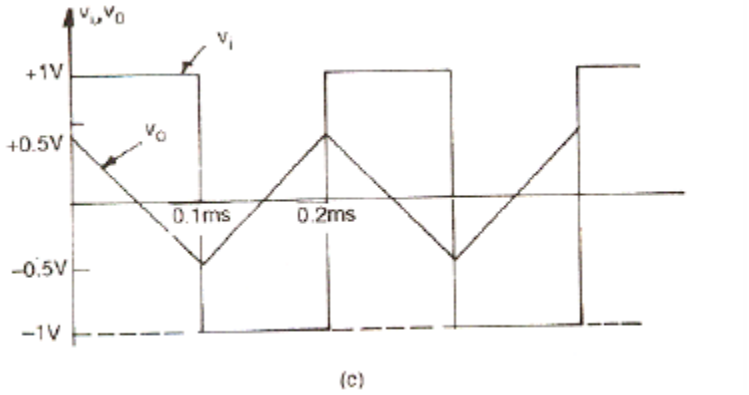
Output voltage is a ramp function



III) SQUARE WAVE INPUT

Input of constant amplitude of 1v from 0 to 0.1 ms and – 1v
from 0.1 ms to 0.2 ms and frequency is 5 KHz.
The outputs are two ramps in opposite directions. The resultant output is triangle wave

$$-\frac{1}{R\,C}\int_0^{0.1ms} 1\,dt = -10^4 \text{ x } 0.1 \text{ x } 10^{-3} = -1\text{v}$$



(c)

QUESTIONS FOR VIVA-VOCE IN LESSON 4 (Answers are given in a separate file)

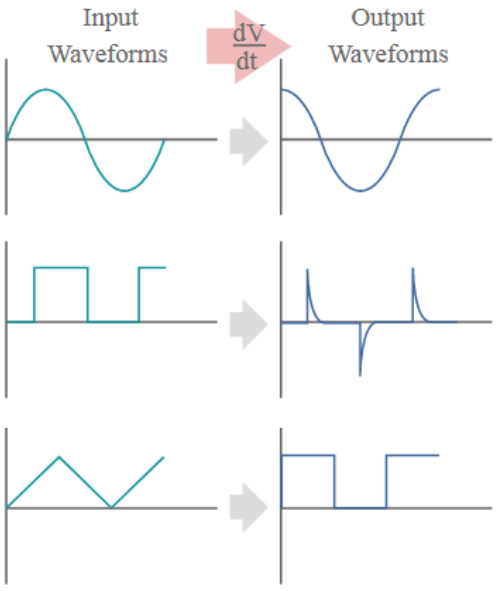
1. For an op-amp. integrator circuit, sine wave input of 4 Sin 1000t is given. In the circuit, R = 200 MΩ and C = 0.1 µF. Determine the value of output voltage.
2. What type of output waveform is obtained when a triangular wave is applied to integrator circuit
3. What is an integrator?
4. Write down the expression for Vo of an integrator.
5. Draw the output waveform of the integrator for different waveforms.
6. What is the purpose behind the connection of Rf in the feedback path of integrator?
7. What are the applications of integrator

EXPERIMENT NO.5
DIFFERENTIATOR CIRCUIT USING OP-AMP

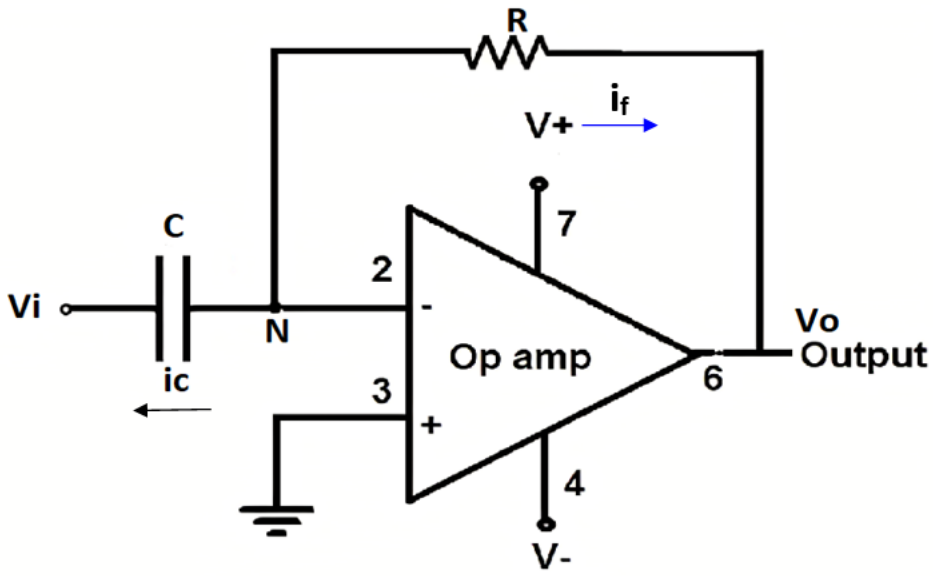
By Exchanging the positions of 'R' and 'C' in integrator the differentiator circuit is obtained. The circuit which produces the differentiation of the input voltage at its output is called differentiator

PRACTICAL EXAMPLES :

Parameter	**Differentiation**
Distance	Speed
Velocity	Acceleration

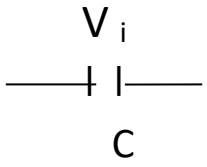


Waveforms and their differentiated derivatives


R
i_f
V+
C
7
2
Vi
N
-
Op amp
Vo
Output
ic
3
6
+
4
V-

Node N is at virtual ground potential

From fundamentals



From fundamentals

$i_c = C\frac{d\,v_i}{dt}$

from Kirchhoff law

$$i_f = \frac{0 - v_o}{R} = \frac{-v_o}{R}$$

$i_c = i_f$

$$i_c = C\ \frac{d\,v_i}{dt} = i_f = \frac{-\,v_0}{R}$$

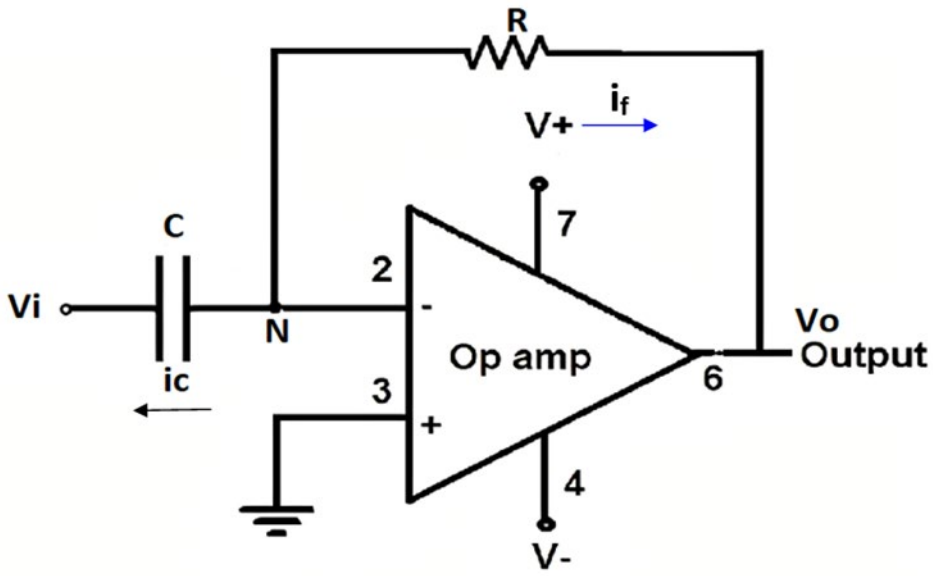
$$v_0 = -R\,C\frac{d\,v_i}{dt}$$

output v_o = derivative of v_i input voltage multiplied by

– (RC)

— ve sign indicates 180 ^{0} phase shift

FINDING GAIN :



ω = 2 π f

Z_f = R and $Z_i = \frac{1}{J\,\omega\,C}$

G $= \frac{v_o}{v_i} =$

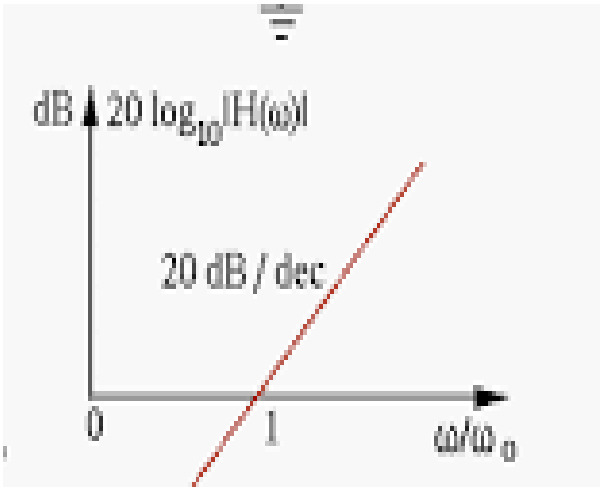
$$G = \frac{v_o}{v_i} = -\frac{R}{\frac{1}{J\omega C}} = -RCJ\omega = -J\omega RC$$

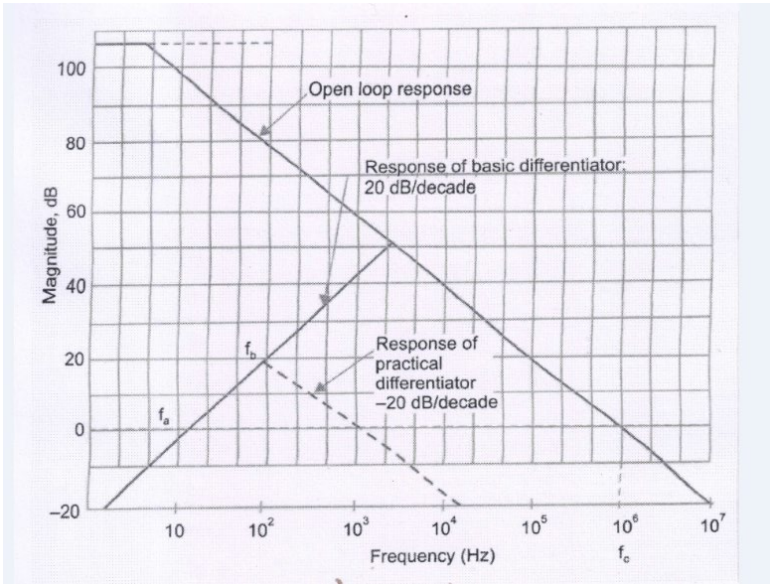
NOTES : G =(a + Jb)or G =(a –Jb)

Magnitude = |G| = $sqrt\,(a^2 + b^2)$

$$|G| = |-J\omega RC| = \sqrt{(\omega RC)^2} = RC\,\omega = RC\,2\,\pi\,f$$

Gain increases with frequency at a rate of + 20dB /decade. At higher frequencies it becomes very large . This leads to instability and noise problems.





Find out frequency at which gain |G| becomes = 1
ie 20 log 1 = 20 x0 =0 dB

|G| = 1 (0 db) when f = f_a

1 = $RC\ 2\ \pi\ f_a$

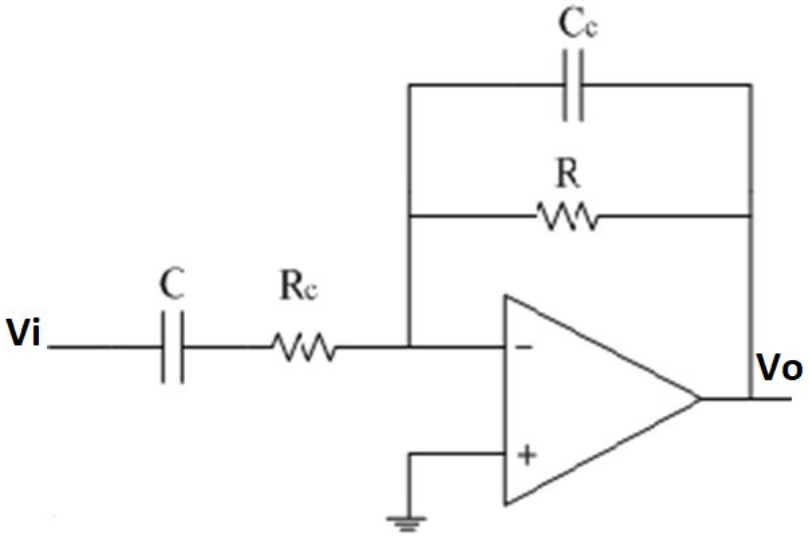
$$f_a = \frac{1}{2\ \pi\ RC}$$

$$\boxed{f_a = \frac{1}{2\ \pi\ RC}}$$

PRACTICAL DIFFERENTIATOR :

$|G| = RC\,\omega = RC\,2\,\pi\,f$

Gain increases with frequency at a rate of + 20dB /decade. At higher frequencies it becomes very large . This leads to instability and noise problems.



$$Z_f = \frac{R \times \frac{1}{J \times \omega C_C}}{R + \frac{1}{J \times \omega C_C}} = R \frac{\frac{1}{J \times \omega C_c}}{\frac{RJ \times \omega C_c + 1}{J \times \omega C_C}}$$

$$Z_f = R \frac{1}{1 + J\,\omega\,C_C R}$$

$$Z_i = R_c + \frac{1}{J\,\omega\,C} = \frac{J\,\omega\,R_C C + 1}{J\,\omega\,C}$$

$$\text{Gain } G = \frac{V_0}{V_i} = -\frac{Z_f}{Z_i}$$

$$G = -R\frac{1}{1 + \mathrm{J}\,\omega\,\mathrm{RC}_C} \times \frac{\mathrm{J}\,\omega\,\mathrm{C}}{\mathrm{J}\,\omega\,\mathrm{R_c C} + 1}$$

Let $\mathrm{R} \times \mathrm{C_c} = \mathrm{R_c} \times \mathrm{C}$

$$G = -\frac{\mathrm{J}\,\omega\,\mathrm{RC}}{(1 + \mathrm{J}\,\omega\,\mathrm{R_c\,C})^2} = -\frac{\mathrm{J}\,\omega\,\mathrm{RC}}{(1 + \mathrm{J}\,\omega\,\mathrm{R_1\,C_1})^2}$$

$$Let\ f_b = \frac{1}{2\,\pi\ R_c\ C} = \frac{1}{2\,\pi\,R\ C_c}$$

$$2\,\pi\ R_c\,C = \frac{1}{f_b}$$

$$G = -\frac{\mathrm{J}\,\omega\,\mathrm{RC}}{(1 + \mathrm{J}\,\omega\,\mathrm{R_c\,C})^2} = -\frac{\mathrm{J}\,2\,\pi\,\mathrm{f\,RC}}{(1 + \mathrm{J}\,2\,\pi\,\mathrm{f\,R_c\,C})^2}$$

$$G = -\frac{\mathrm{J}\,2\,\pi\,R\,\mathrm{C}}{(1 + \mathrm{J}\,(\frac{f}{f_b}))^2}$$

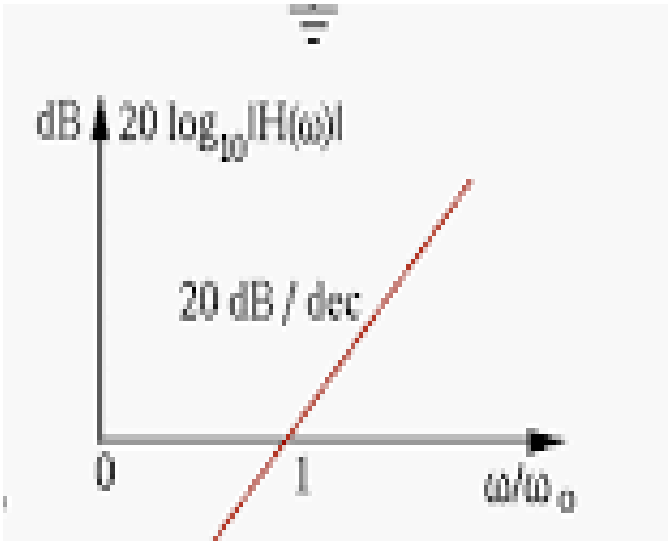
CASE (I) FOR f <f_b

denominator $(1 + J\ \frac{f}{f_b})^2 \approx 1$

$\mathrm{G} = -\mathrm{J}\,2\,\pi\,\mathrm{f\,RC}$

$$|\mathrm{G}| = \sqrt{0^2 + (2\,\pi\,\mathrm{f\,RC})^2} = 2\,\pi\,\mathrm{f\,RC}$$

Gain G directly increases with frequency. For increase of 10 times in frequency the output increases by 10 (2 π R C is constant)20 log 10 = 20 dB



CASE (II) WHEN F > FB

$$\text{denominator } (1 + \text{J}\ \frac{f}{\text{f}_\text{b}}\ )^2 \approx (J\frac{f}{f_b})^2$$

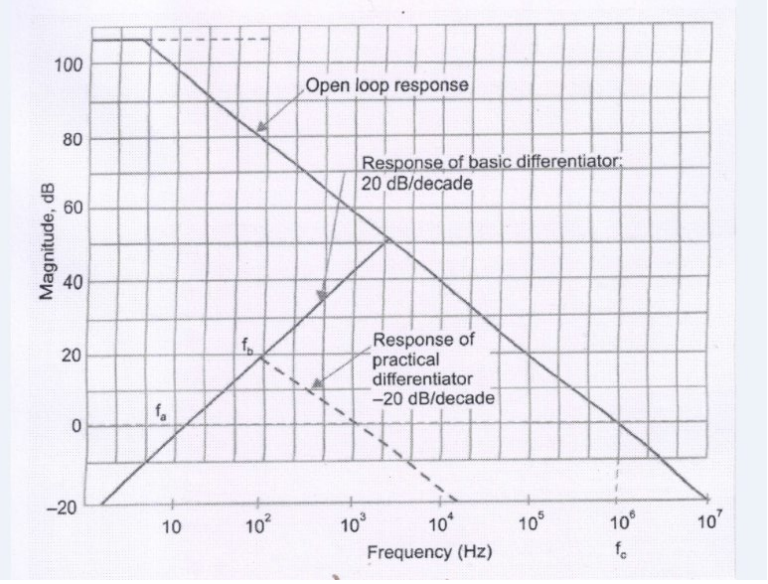
$$G = -\ \frac{J2\,\pi\,R\,\text{C}}{(\text{J}\ \frac{f}{f_b})^2} = -\ \frac{J\frac{f}{f_a}}{(\text{J}\ \frac{f}{f_b})^2}$$

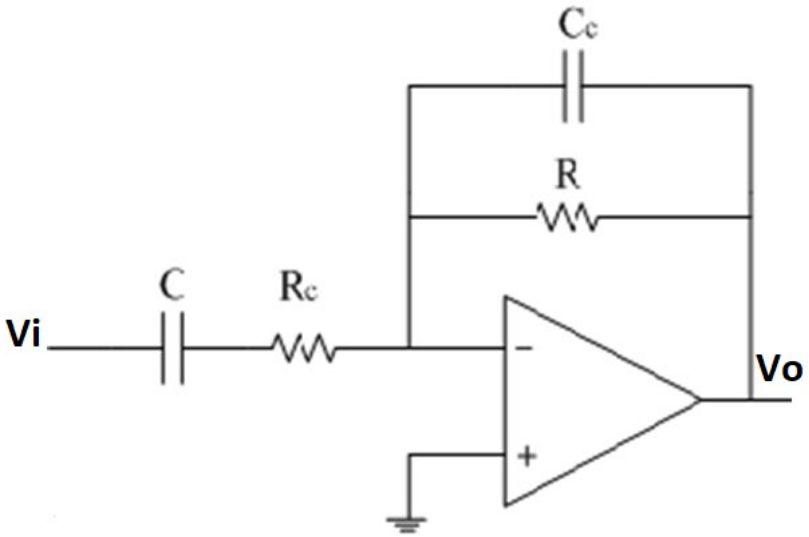
$$|G| = \frac{\sqrt{(\frac{f}{f_a})^2}}{\sqrt{(\frac{f}{f_b})^{2\times 2}}} = \frac{(\frac{f}{f_a})}{(\frac{f}{f_b})^2} = \frac{(f_b)^2}{f_a} \times \frac{1}{f}$$

$$(\ since\ \frac{(f_b)^2}{f_a} = \left(\frac{1}{2\,\pi\,R\text{C}}\right)^2\ \times\ 2\,\pi\,R\text{C}\ is\ \ a\ constant)$$

So |G| is proportional to $\frac{1}{\text{f}}$

so |G| Decreases at —20 dB/decade





EXPERIMENT:

Differentiate an input signal with f = 100 Hz.

Let f = f_{max} = f_a = 100 Hz =

$$f_a = \frac{1}{2\,\pi\,R\,\mathrm{C}}$$

C = 0.1 μf = 0.1 x 10^{-6} f

$$100 = \frac{1}{2\,\pi\,R\ \times\ 0.1\ \text{x}\ 10^{-6}}$$

$$R = \frac{1}{2\,\pi\ \ \times 100 \times\ 0.1\ \text{x}\ 10^{-6}} = 15900 = \ 15.9\ K'\Omega$$

Choose fb = 10 fa = 1000 Hz

$$But\ \ f_b\ \ =\ \ \frac{1}{2\,\pi\ \ R_c\ \ C}$$

$$1000 = \ \frac{1}{2\,\pi\,R_c \times 0.1\ \text{x}\ 10^{-6}}$$

$$R_c = \frac{1}{2\,\pi\ \ \times 1000 \times\ \ 0.1\ \text{x}\ 10^{-6}} = 1.59\ K'\Omega$$

Since $\mathrm{R}\ \times \mathrm{C_c} =\ \ \mathrm{R_c}\ \times \mathrm{C}$

$$Cc = \frac{1.59\ \times\ \ 10^3\ \ \times 0.1\ \ \times 10^{-6}}{15.9\ \times\ 10^3} = 0.01\ \ \times 10^{-6}\ =\ .01\ \mu f$$

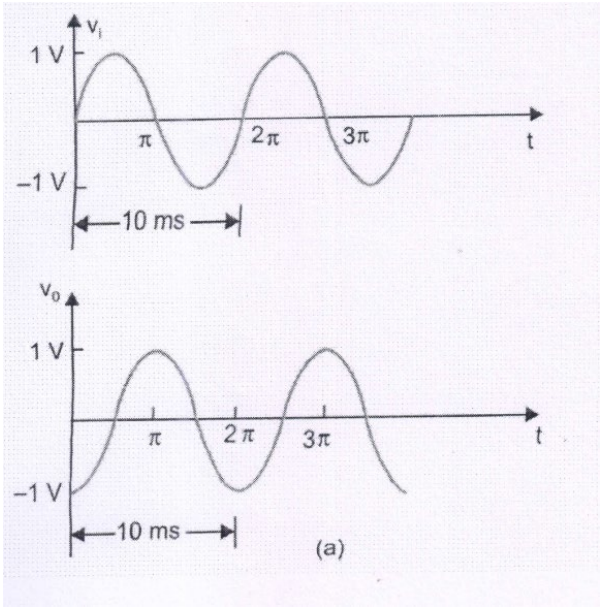
a) Vi = 1 sin 2π (100) t

Vo = –R_f $C_1\frac{dv_i}{dt}$ = –15.9 x 10^{3} x 0.1 x 10^{-6} $\frac{d\ (1 \sin 2\pi\ (100)\ \text{t}}{dt}$

Vo = –15.9 x 10^{3} x 0.1 x 10^{-6} x 2π x 100 cos (2π x 100) t

Vo = – 0.999 Cos (2π x 100) t

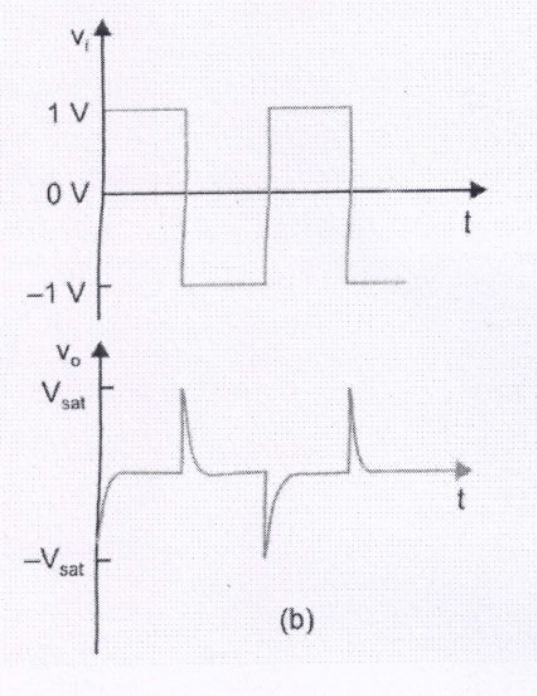
Vo = Cos (2π x 100) t



Increase the frequency to 200 Hz. and 300 Hz.now the peak amplitude of Cos wave will be —2 V and —3V respectively

b) For a square wave input 1volt peak and 1000 Hz. The output wave form will consists of positive and negative spikes of magnitude Vsat (13 V for +/ –15 V supply))

During the time periods for which input is constant at +/–1 V the differentiator output will be zero. However when input translates between +/–1 V levels the slope of the input is infinite for an ideal square. The output gets clipped to about
+/ 13 v



QUESTIONS FOR VIVA-VOCE IN LESSON 5 (ANSWERS ARE GIVEN IN A SEPARATE file)

1.Sketch the output wave forms, if a square wave input is applied to op-amp differentiator circuit. Given R = 0.1 kΩ, C = 0.01 µF. frequency of the square wave input is 100 Hzs

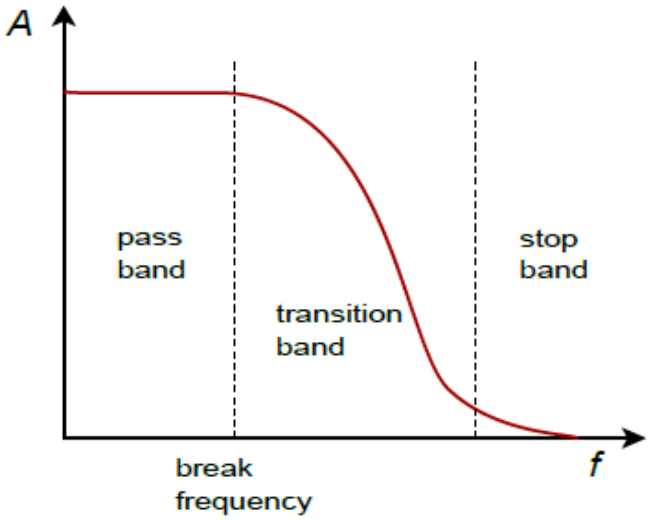
2. Sketch the Input and Output waveforms when we apply a 1Khz triangle wave with peak to peak value of 5V to the Differentiator circuit. 3. A low frequency differentiator is desired for a particular application to Perform the operation Vo (t) =-0.001 dvi(t)/dt . Determine the suitable design of differentiator circuit for the periodic signal with a frequency of 1 KHz.

4.Determine the component values of a differentiator circuit to perform true differentiation, when the input is a square wave of 1 kHz frequency.

EXPERIMENT NO.6A
ACTIVE FILTER APPLICATIONS LPF

WHAT IS A FILTER?

An electric filter is a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. Filters may be classified in a number of ways:

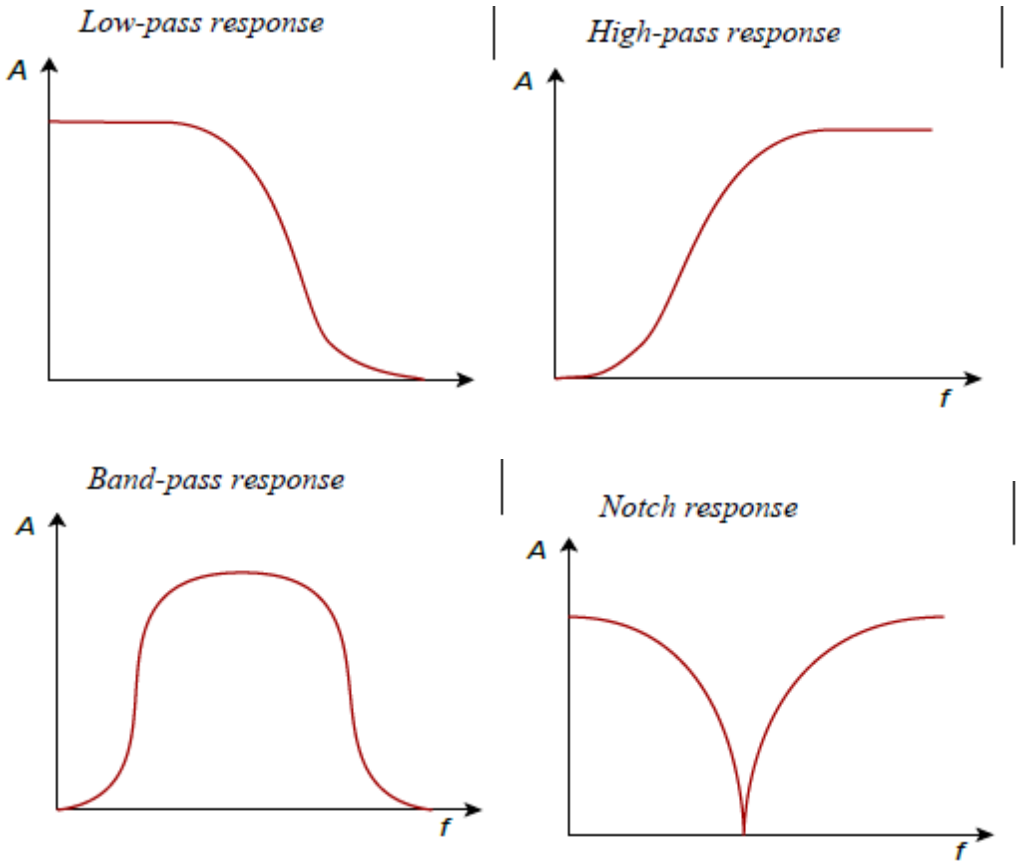


1) BASED ON COMPONENTS USED IN THE CIRCUIT :

i) Passive filters – Use only passive elements like resistors, capacitors, and inductors (coils) **ii) Active filters:** use in addition to resistors, capacitors and inductors also active components like transistors, op-amps

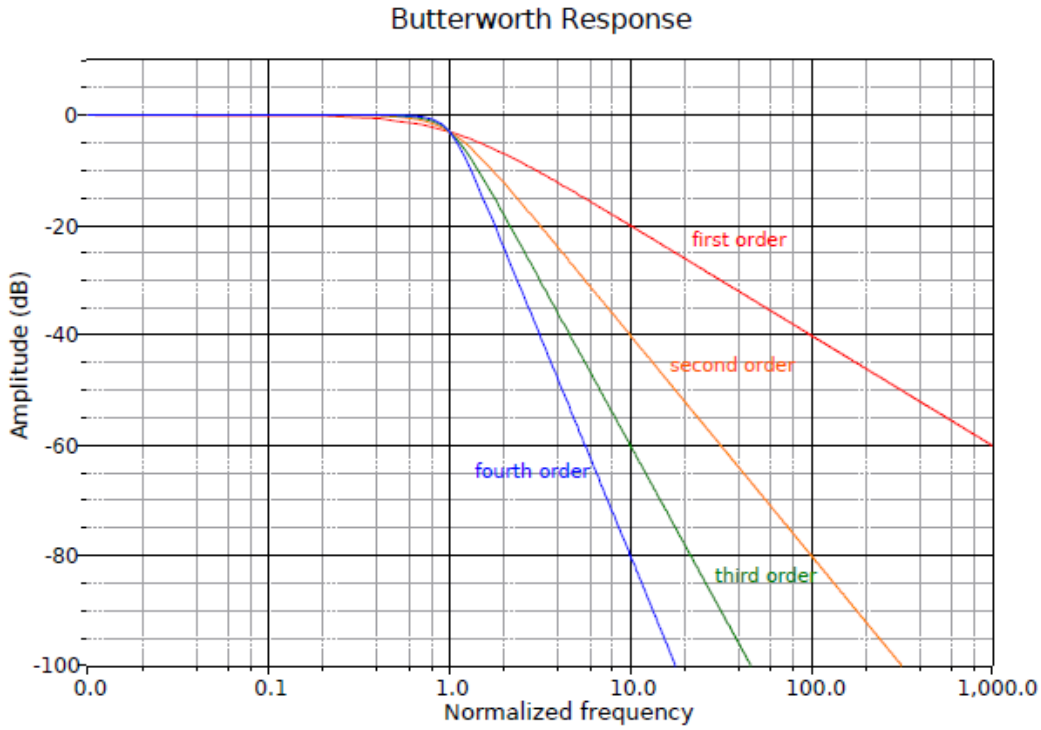
2) BASED ON FREQUENCY RANGE:

i) Low pass filter (LPF) - Allows low frequencies
ii) High pass filter(HPF) - Allows high frequencies
iii)Band pass filter (BPF) - Allows band of frequencies
iv) Band reject filter (BRF)- Rejects band of frequencies
v)All pass filter- Allows all frequencies but with a phase shift



3) BASED ON ORDER OF FILTER

i) First order ii) Second order iii) etc.,



4) BASED ON TYPE OF FREQUENCY RESPONSE

i) Butter worth ii) Bessel

iii) Chebysshev iv) Eliptic

ADVANTAGES OF ACTIVE FILTERS:

1. Active filters do not exhibit insertion loss like passive filters. Active filters can be made with flexible pass band gain.
2. No loading problems because of high input impedance of op-amp
3. Active filters avoid the use of Inductors which are difficult to make and costly
4. Active filters are less costly compared to passive filters.

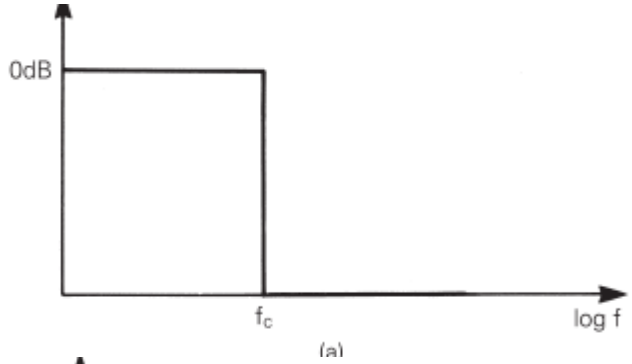
DISADVANTAGES OF ACTIVE FILTERS:

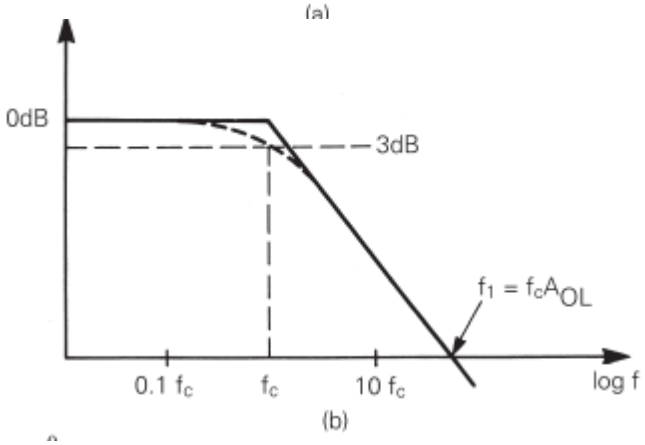
1.Active filters require a DC power supply whereas passive do not.
2. Active filters are limited in their frequency range. An op amp has a finite gain-bandwidth product, and the active filter produced can certainly not be expected to perform beyond it. For example, it would be impossible

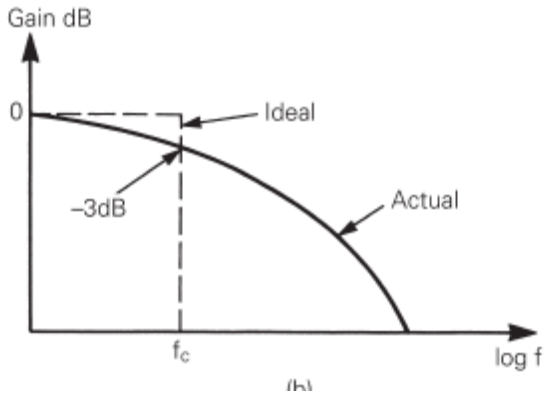
to design a filter that only passes frequencies above 10 MHz when using a standard µA741. Passive filters do not have this limitation and can work well into the hundreds of MHz.

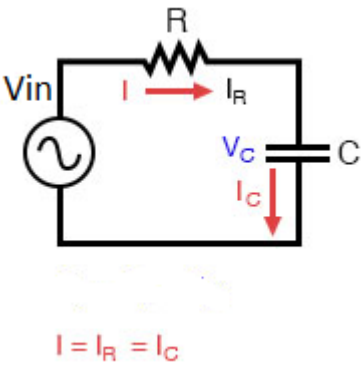
3. Finally, active filters are not designed to handle large amounts of power. They are low signal-level circuits. With appropriate component ratings, passive filters may handle hundreds of watts of input power.

THEORY OF FIRST ORDER BUTTERWORTH LOW PASS FILTER









$I = I_R = I_C$

Impedance of capacitor = $\frac{1}{J\ \omega\ C}$

Current flowing in the series circuit $= i_c = \frac{V_i}{R+\frac{1}{J\ \omega\ C}} = \frac{V_i}{\frac{J\ \omega\ R\ C+1}{J\ \omega\ C}}$

Voltage across capacitor = current x impedance of capacitor

$$V_C = V_i \left[\frac{\cancel{J\omega c}}{1 + J\omega R c} \times \frac{1}{\cancel{J\omega C}}\right] = \frac{V_i}{1 + J\omega R c}$$

$$G = \frac{V_C}{V_i} = \frac{1}{1 + J\omega R c}$$

Based on the formula magnitude of $\frac{1}{a+J\ b} = \frac{1}{\sqrt{a^2+b^2}}$

$$|G| = \frac{1}{\sqrt{1^2 + (\omega\ R\ C)^2}}$$

If magnitude is 0.0707 ie 20 log (0.707) = – 3 dB

Frequency f_h at – 3 dB Gain is

$$0.707 = \frac{1}{\sqrt{1^2+(2\ \pi\ f_h\ R\ C)^2}} = \frac{1}{\sqrt{2}}$$

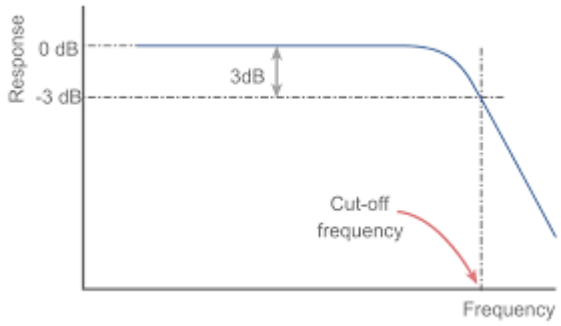
$$(2\ \pi\ f_h\ R\ C)^2 = (1)^2$$

$$2\ \pi\ f_h\ R\ C = 1$$

$$f_h = \frac{1}{2\ \pi\ R\ C}$$

f_h is called the corner frequency

FREQUENCY RESPONSE OF LPF



Thus the Low – Pass filter has a constant gain A_f from 0 Hz to the almost high cut-off frequency f_h it has the gain 0.707A_f at exactly f_h and after f_h gain decreases at a constant rate with an increase in frequency. The gain decreases 20 dB (= 20 log 10) each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_h is 20 dB/decade. The frequency f = f_h is called the cut-off frequency because the gain of the filter at this frequency is down by 3 dB (=20log 0.707) from 0 Hz. Other equivalent terms for cut-off frequency are –3dB frequency, break frequency, or corner frequency.

LAB EXPERIMENT FIRST ORDER LOW PASS FILTER (Butterworth)

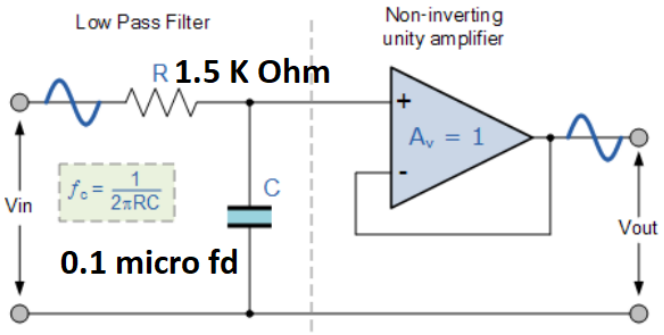
Aim: To design and setup a LPF Butterworth filter and plot the frequency response for different frequencies

EQUIPMENT/COMPONENTS

Sl.No.	Name and Specification	Quantity
1	Dual Power Supply +/−15 V	1
2	Function Generator (0 – 1 MHz)	1
3	Oscilloscope 10 MHz	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors and capacitors	4
7	Probes and Connecting wires	As required
8	Multimeter	1

A first Order Low Pass Butter worth filter uses RC network for filtering. Note that here the op- amp is used in the non-inverting configuration. hence it does not load down the RC network.

PROBLEM 1: Design a LPF filter with corner frequency of $f_h = 1000$ Hz and gain 1



$$f_h = \frac{1}{2\,\pi\ R\ C}$$

f_h = 1000 Hz and let C = 0.1 µ f

$$f_h = \frac{1}{2\,\pi\ R\ C}$$

$$1000 = \frac{1}{2\,\pi\ R\ \times\ 0.1\ \times\ 10^{-6}}$$

$$R = \frac{1}{2\,\pi\ \times 0.1 \times 10^{-6} \times 1000} = 1592\ \Omega \text{ say } 1.5\ K\Omega$$

$$\text{Magnitude of Gain } |G| = \frac{1}{\sqrt{1^2 + (\omega\ R\ C)^2}}$$

$$|G| = \frac{1}{\sqrt{1^2 + (2 \times \pi \times\ f\ \times 1.5 \times 10^3\ \times 0.1 \times 10^{-6})^2}}$$

Using the calculator find out |G| for different values of ' f ' fill the table below

Sl.NO	FREQUENCY	GAIN RATIO	GAIN dB	Theoretical Peak to peak Output voltage	Experimental peak to peak
1	200 Hz	0.98	– 0.18	9.8 v	
2	400	0.94	– 0.54	9.4	
3	600	0.87	– 1.21	8.7	
4	800	0.80	– 1.94	8.0	
5	1000	0.73	– 2.94	7.3	
6	1062	0.71	– 2.98	7.1	
7	1500	0.58	– 4.73	5.8	
8	2000	0.47	– 6.56	4.7	
9	4000	0.26	– 11.7	2.6	
10	5000	0.21	– 13.6	2.1	
11	10000	0.10	– 19.6	1.0	
12	50000	0.02	– 33.6	0.2	

PROCEDURE FOR EXPERIMENT 1

1. Connect the components/equipment as shown in the circuit diagram.

2. Switch ON the power supply.

3. Connect channel 1 of CRO to input terminals (Vi) and channel 2 to output terminals (Vo).

4. From a function generator give different frequencies with peak to peak voltage of 10 V (+ 5V to –5V) The frequency may be from 200 Hz..

5. By varying the input frequency in regular intervals, note down the output voltage.

6. Calculate the gain (peak Vo/peak Vi) and Gain in dB = 20 log (Vo/Vi) at every frequency.

7. Plot the frequency response curve (taking frequency on X-axis & Gain in dB on Y-axis) using Semi log Graph.

8. Find out the high cut-off frequency, f_h (at Gain ratio=0.707)

– 3 dB) from the frequency response plotted.

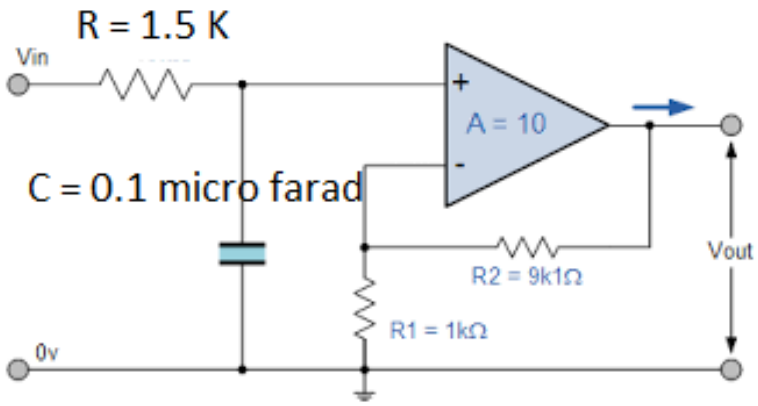
9. Verify the practical (f_h from graph) and the calculated theoretical cut-off frequency (f_h= 1/2πRC).

DESIGN PROBLEM 2

PROBLEM 2: Design a LPF filter with corner frequency of f_h = 1000 Hz and gain 10

1. cut-off frequency, f_h =1 KHz and value for gain $A_f = 10$
2. Assume a value of C = 0.1 μF
3. Calculate the value of R using the equation
4. Finally, select values of R1 and R2 dependent on the desired pass band gain using A_f = 1+ R2/R1 .
5. Assume a value for R1 =1KΩ and calculate R2. R2 will be 9.1K

CIRCUIT DIAGRAM:



PROCEDURE FOR EXPERIMENT 2

Repeat the steps as given in "PROCEDURE FOR EXPERIMENT 1" Except that at Step 4 apply peak to peak voltage of 1V (+05V to –0.5V)

1. Connect the components/equipment as shown in the circuit diagram.

2. Switch ON the power supply.

3. Connect channel 1 of CRO to input terminals (Vi) and channel 2 to output terminals (Vo).

4. Set Vi = 1V & fin = 10Hz using function generator.

5. By varying the input frequency in regular intervals, note down the output voltage.

6. Calculate the gain (Vo/Vi) and Gain in dB = 20 log (Vo/Vi) at every frequency.

7. Plot the frequency response curve (taking frequency on X-axis & Gain in dB on Y-axis) using Semi log Graph.

8. Find out the high cut-off frequency, f_h (at Gain ratio= 0.707)

– 3 dB from the frequency response plotted.

9. Verify the practical (f_h from graph) and the calculated theoretical cut-off frequency (f_h= 1/2πRC).

Sl.NO	FREQUENCY	GAIN RATIO	GAIN dB	Theoretical Peak to peak Output voltage	Experimental peak to peak voltage
1	200 Hz	0.98	– 0.18	9.8 v	
2	400	0.94	– 0.54	9.4	
3	600	0.87	– 1.21	8.7	
4	800	0.80	– 1.94	8.0	
5	1000	0.73	– 2.94	7.3	
6	1062	0.71	– 2.98	7.1	
7	1500	0.58	– 4.73	5.8	
8	2000	0.47	– 6.56	4.7	
9	4000	0.26	– 11.7	2.6	
10	5000	0.21	– 13.6	2.1	
11	10000	0.10	– 19.6	1.0	
12	50000	0.02	– 33.6	0.2	

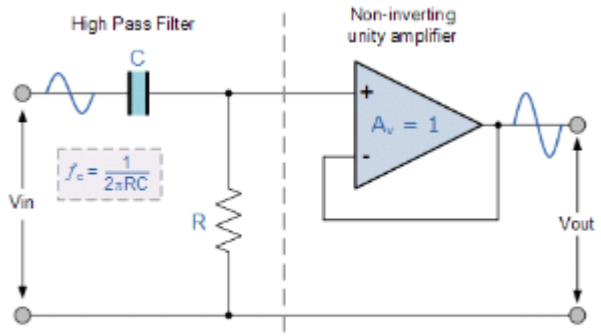
EXPERIMENT NO. 6B
ACTIVE FILTER APPLICATION HPF (FIRST ORDER)

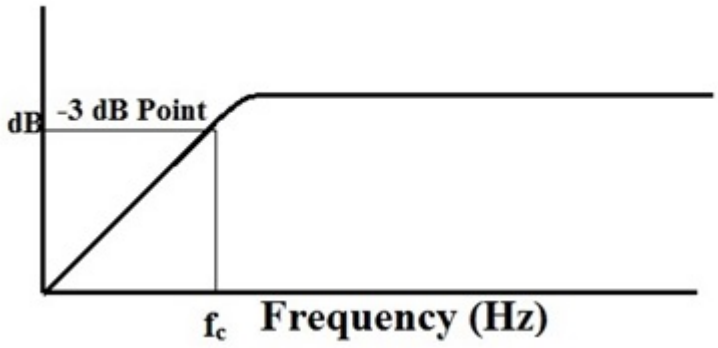
THEORY:

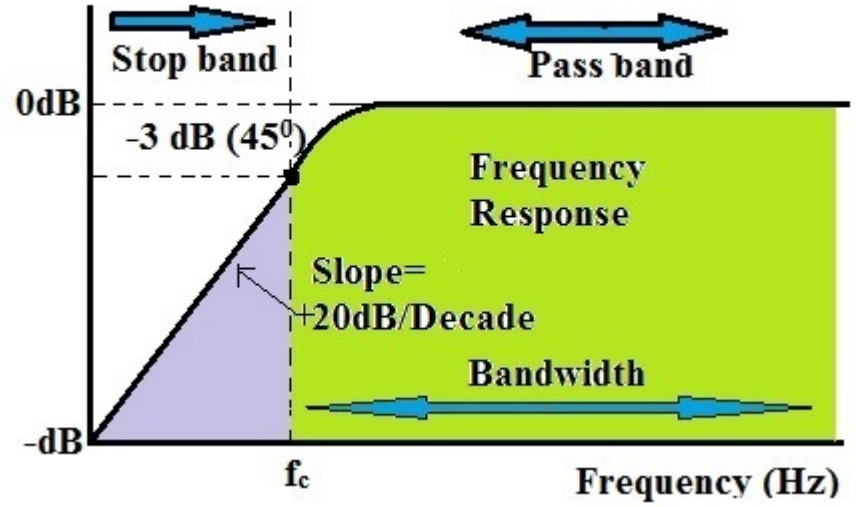
An active High pass filter is created by combining a passive RC filter network with an op-amp

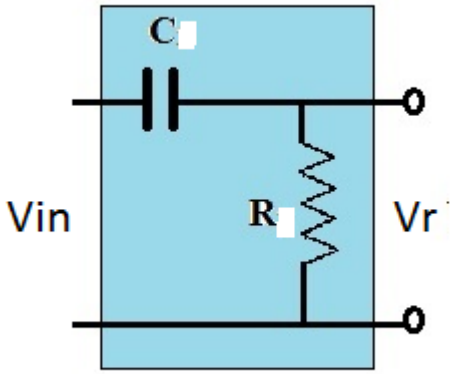
Using an op-amp we can design the filter to have a gain also. The standard inverting or noninverting op-amp configurations can be used to get inverting or non-inverting outputs. This is not possible with passive filter which does not use op-amp

FIRST ORDER HIGH PASS FILTER GAIN 1:









Current flowing in Resistor R = Ir

$$\frac{Vin}{R + \frac{1}{J\omega C}}$$

Ir = $\frac{Vin\, J\omega C}{1 + J\omega CR}$

Voltage across Resistance Vr = $\frac{Vin\, J\omega C}{1 + J\omega CR} \times R$

$$Vr = Vin\ \frac{J\omega RC}{1\ +\ J\omega RC} =\ Vin\frac{J\ 2\ \pi\ f\ RC}{1\ +\ J\ 2\ \pi\ f\ RC}$$

$$Let\ f_C = \frac{1}{2\ \pi\ R\ C}$$

So $\quad 2\ \pi\ R\ C = \frac{1}{f_c}$

Substituting in Vr

$$Vr = Vin\ \frac{J\ \frac{f}{f_C}}{1\ +\ J\ \frac{f}{f_C}}$$

$\frac{\text{Vr}}{\text{Vin}}$ = G = $\frac{J\frac{f}{f_C}}{1 + J\frac{f}{f_C}}$

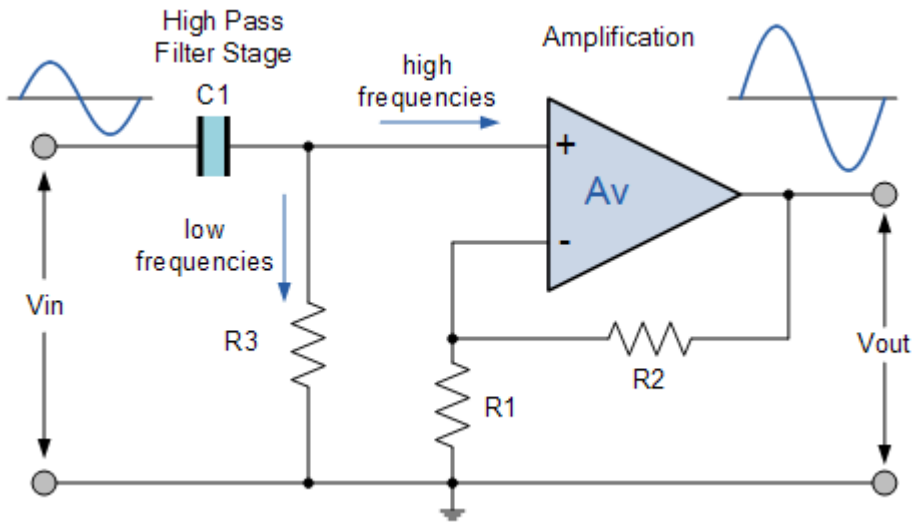
If a + jb is a vector Magnitude = $\sqrt{a^2 + b^2}$

$|G| = \frac{\sqrt{(\frac{f}{f_C})^2}}{\sqrt{1+(\frac{f}{f_C})^2}} = \frac{\frac{f}{f_C}}{\sqrt{1+(\frac{f}{f_C})^2}}$

When f = f_c

$|G| = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = \frac{1}{1.404} = 0.707$

20 log (0.707) = —3 dB



Let 1+ $\frac{R2}{R1}$ = A when R2= R1 , A = 2

$$|G| = \frac{A\frac{f}{f_C}}{\sqrt{1+(\frac{f}{f_C})^2}}$$

1. At very low frequencies f < f_c Gain magnitude < A

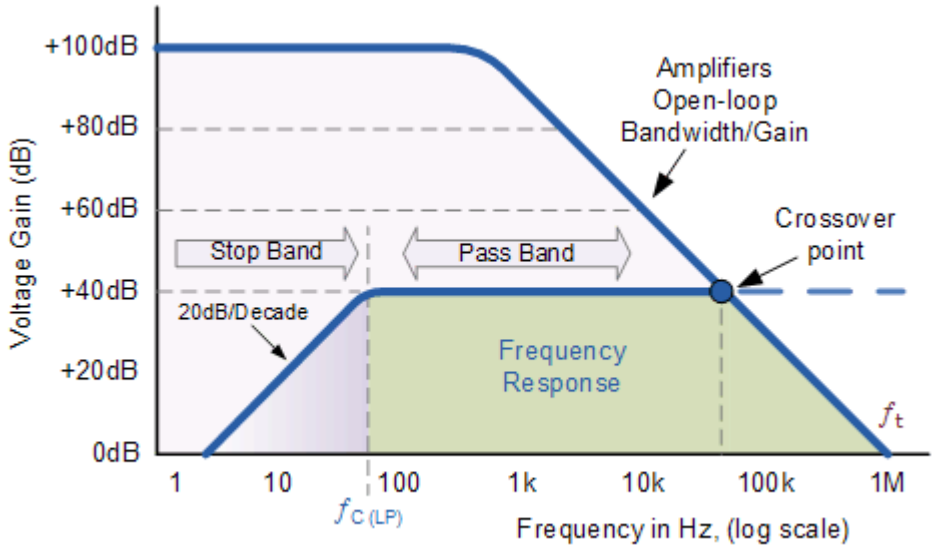
$\frac{f}{f_C}$ is far less than 1. So denominator $\sqrt{1+(\frac{f}{f_C})^2} = \sqrt{1} = 1$

$|G| = \frac{A\frac{f}{f_C}}{1}$ So |G| = A is small value initially as f increases it |G| also increases until it becomes A when f = fc. Since |G| is directly proportional to f the rate of increase will be

20 dB /decade

2. At cut off frequency f = f_c Gain magnitude = $\frac{A}{\sqrt{2}} = 0.707\ A$
3. At high frequency f > f_c Gain magnitude = A

4. The upper frequency limit of pass band is determined by the open loop band width of op-a



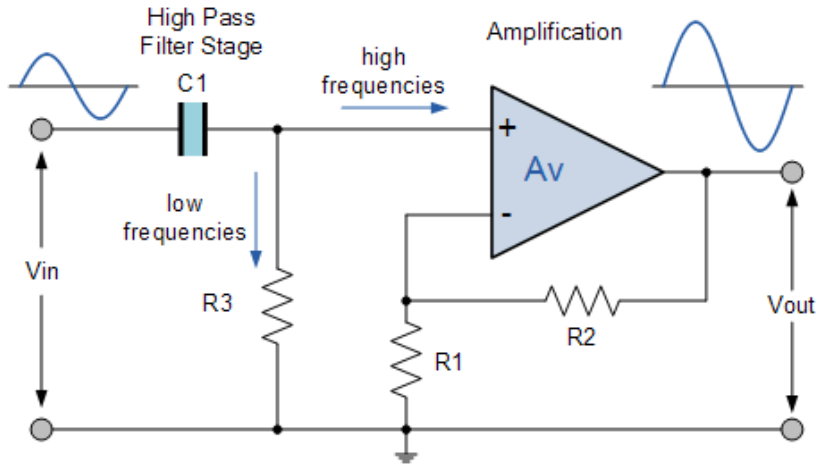
LAB EXPERIMENT FIRST ORDER BAND PASS FILTER

AIM: To design and setup a HF filter and plot the frequency response to different frequencies

EQUIPMENT/COMPONENTS

Sl.No.	Name and Specification	Quantity
1	Dual Power Supply +/−15 V	1
2	Function Generator (0 – 1 MHz)	1
3	Oscilloscope 10 MHz	1
4	Bread Board	1
5	IC 741 C	1
6	Resistors and capacitors	4
7	Probes and Connecting wires	As required
8	Multimeter	1

PROBLEM: Design a HF with Cutoff frequency of 1000 Hz and with a gain of 2



A = 2 which means $1+\frac{R2}{R1}$

R1 = 10 K Ω so R2 = 10 KΩ

Cut off frequency = f_c = 1000 Hz

Let C = 10 nf =10 x 10^{-9} farad

$1000 = \frac{1}{2\pi R C} = \frac{1}{2\times 3.14\times R\times 10\times 10^{-9}}$

R = 15.92 K Ω nearly 16 K Ω

PROCEDURE FOR EXPERIMENT

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect channel 1 of CRO to input terminals (Vi) and channel 2 to output terminals (Vo).
4. From a function generator give different frequencies with peak to peak voltage of 5 V (+2. 5V to –2.5V) The frequency may be from 100 Hz..
5. By varying the input frequency in regular intervals, note down the output voltage. Find out the Gain and Put the values in the table
6. Calculate the gain (peak Vo/peak Vi) and Gain (Vo/Vi) at every frequency using the formula =

G = $A_f \frac{2\pi f R C}{\sqrt{1+(2\pi R C)}}$ where $A_f = 2$ .Put the values in the table

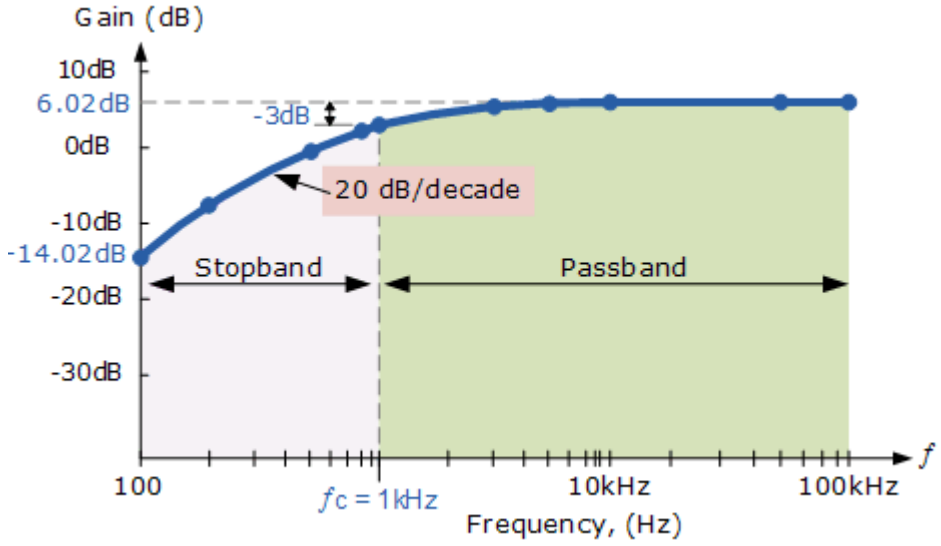
7. Plot the frequency response curve (taking frequency on X-axis & Gain in dB on Y-axis) using Semi log Graph.

8. Find out the cut-off frequency, f_c (– 3 dB) from the frequency response plotted.

9. Verify the practical (f_c from graph) and the calculated theoretical f_c

Sl.no.	**Frequency Hzs**	**Gain ratio**	**Gain ratio after** $\mathbf{1+\frac{R2}{R1}}$	**Observed Gain ratio**	**Observed Gain ratio in dB 20 log Gain ratio**
1	100	0.1	0.2		
2	200	0.195	0.39		
3	500	0.445	0.89		
4	800	0.625	1.25		
5	1000	0.705	1.41		
6	3000	0.95	1.90		
7	5000	0.98	1.96		
8	10000	0.995	1.99		
9	50000	1.00	2.00		
10	100000	1.00	2.00		

Plot the graph between Frequency and Observed Gain ratio in dB on a Semi Log graph sheet



QUESTIONS FOR VIVA-VOCE IN LESSONS 6A, 6B (Answers are given in a separate file)

1. List the advantages of active filters over passive filter.
2. Derive fH of second order LPF.
3. Draw the frequency response for ideal and practical of all types of filters.
4. Design a first order low pass filter for 2 kHz frequency.
5. Draw the ideal and practical frequency response characteristics of high pass filter.
6. What are the applications of LPF and HPF

EXPERIMENT NO. 7
IC 741 WAVEFORM GENERATORS-SINE, SQUARE WAVE & TRIANGULAR WAVES

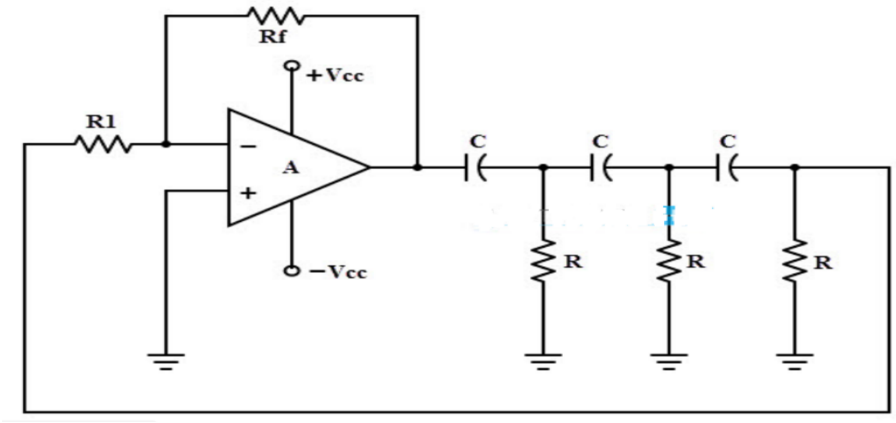
- **AIM**: To generate SINE, SQUARE, TRIANGULAR Waveforms, Determine its Frequency and Plot the waveforms

- **EQUIPMENT & COMPONENTS**

Sl.No.	Name and Specification	Quantity
1	Dual Power Supply +/−15 V	1
2	Function Generator (0 – 1 MHz)	1
3	Oscilloscope 20 MHz	1
4	Bread Board	1
5	OP-AMP IC 741 C	1
6	Resistors and capacitors	Assorted
7	Probes and Connecting wires	As required

- **1. GENERATION OF SINE WAVE: (THEORY)**
- There are number of varieties of oscillators which generate Sinewave. Ex: 1. RC phase shift 2. Wien Bridge 3. Quadrature oscillator etc.
- For continuous sustained oscillations two of the following BARKHAUSENS criterion must be satisfied
- **THE BARKHAUSENS CRITERION STATES THAT:**
- 1. The total phase shift around a closed loop as the signal proceed from input through amplifier output, feedback network back to input completing a closed loop is 360^0 or 0^0 or n 2π where n= integer
- 2. The magnitude of the product of the open loop gain of the amplifier (A) and feedback factor βis unity i.e. Aβ= 1

- **1. RC PHASE SHIFT OSCILLATOR**

- 

- From theory it is known for 3 numbers of RC networks each giving 60^0 phase shift
- Frequency of oscillation $f_O = \frac{1}{2\pi R C \sqrt{6}} = \frac{0.065}{RC}$
- Each network acts as a load for its previous network . From the theory to maintain the overall loop gain (for oscillations) =1 it can be deduced that the minimum gain of the inverted configuration must be 29 or more
- $\frac{R_f}{R_1} \geq 29$ ie $R_f \geq 29\ R_1$
- **1. EXPERIMENT FOR GENERATION OF SINEWAVE:**

  Design a phase shift Oscillator for a frequency = 600Hz

  (Formula) $f = \frac{0.065}{R C}$

  $600 = \frac{0.065}{R C}$

  Let C = 0.1 x 10^{-6} farad (0.1 µF)

  Substituting C in the above formula we get R = 1083(say 1K)

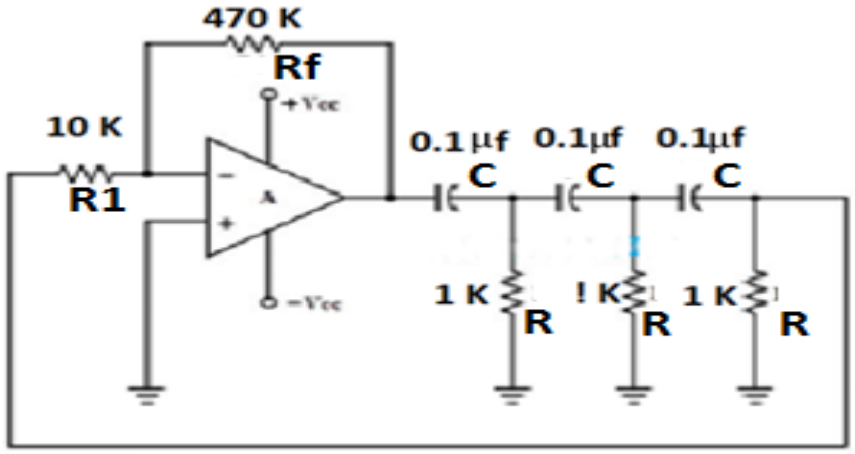
  R1 should be more than 10 x R to avoid loading of R

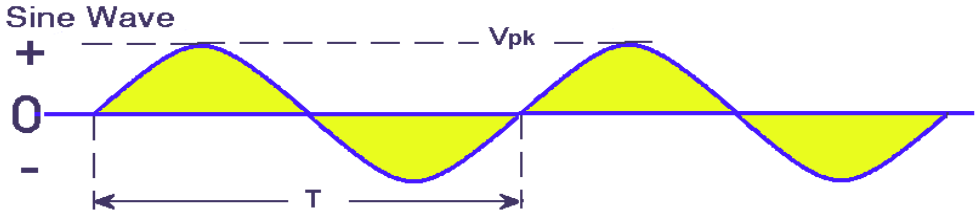
  So R1 = 10 x 1 K = 10K

  Since $\frac{R_f}{R_1} \geq 29$ from the theory

If R_f =470 K then $\frac{R_f}{R_1} = \frac{470\ K}{10\ K} = 47$.

So it satisfies the theory



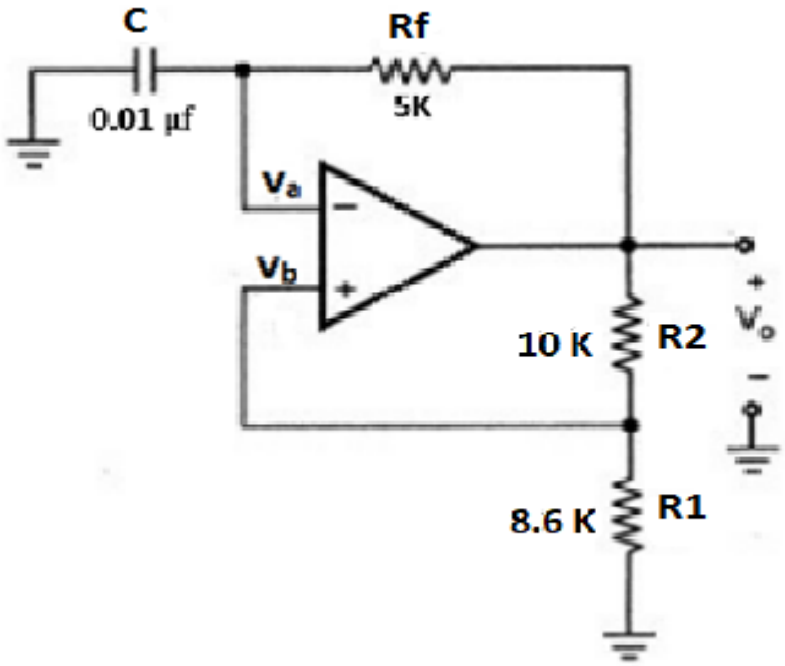


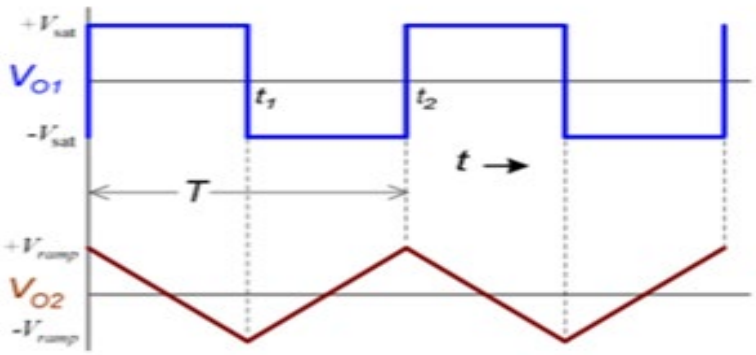
- **PROCEDURE**
- A) Connect the Circuit as per the Circuit diagram above
- B) switch on the Power supply
- C) observe the output waveform on the Oscilloscope. Measure the time period of the Sine wave.
- Frequency of the Sine wave is equal to the reciprocal of the measured time period
- Compare it with the theoretical value. Find out the % error which is $\frac{Theoretical-Practical}{Theoretical} \times 100$

2. EXPERIMENT FOR GENERATION OF SQUARE WAVE:

- Design a square wave generator (using Astable multivibrator) using op-amp with frequency of 10 KHz and using 0.1 µF

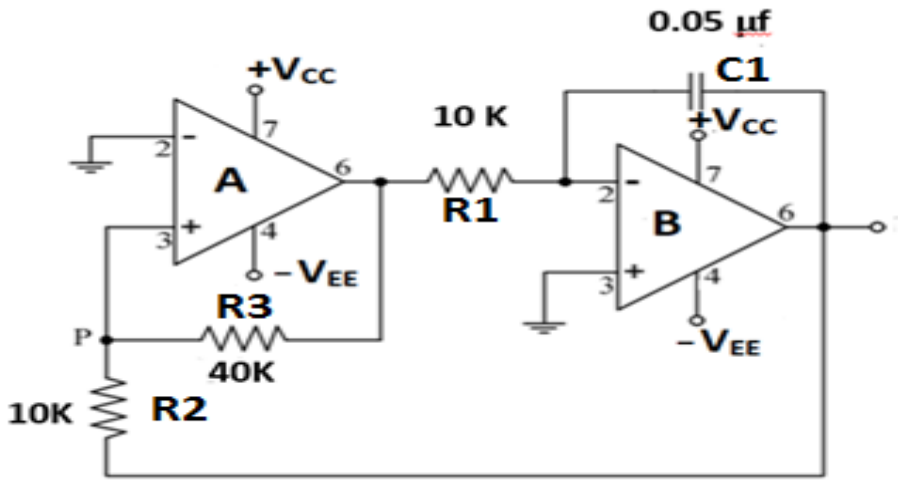
- Formula from theory $f = \frac{1}{2 R_f C \ \ln\left[\frac{2 R_1 + R_2}{R_2}\right]}$
- From Theory we know that
- If R1 =0.86R2 ; then $f = \frac{1}{2 R C}$
- If R_2 = 10 KΩ then R_1 = 8.6 KΩ
- Let C = 0.01 µf
- f = (10) (10^3) = $\frac{1}{2 R_f C} = \frac{1}{2 R_f (0.01)(10^{-6})}$ ∴ $R_f = 5000\ \Omega$

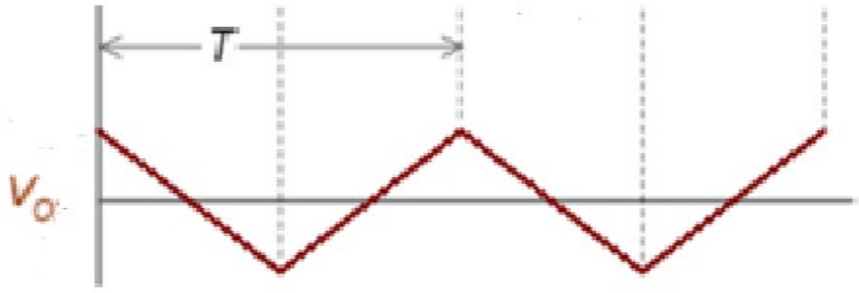




- **PROCEDURE**
- A) Connect the Circuit as per the Circuit diagram above
- B) switch on the Power supply
- C) observe the output waveform on the Oscilloscope. Measure the time period of the Square wave.
- Frequency of the Square wave is equal to the reciprocal of the measured time period
- Compare it with the theoretical value. Find out the % error which is $\frac{Theoretical-Practical}{Theoretical} \times 100$

- **3. EXPERIMENT FOR GENERATION OF TRIANGULAR WAVE:**





- Design a triangular wave generator so that f_0 = 2 KHz and v_o (pp) = 7VSupply voltages = ± 15 V
- Let V_{sat} =14 V
- v_0(pp) = $2\frac{R_2}{R_3}(V_{sat})$ (From theory)
- $\frac{R_2}{R_3} = \frac{v_0(pp)}{2\ V_{sat}} = \frac{7}{(2)(14)}$ $\therefore 4\ R_2 = R_3$
- Let R_2 = 10 KΩ then R_3 =40 KΩ
- $f_0 = \frac{R_3}{4\ R_1\ C_1\ R_2}$ (From Theory)
- $2000 = \frac{(40)(10^3)}{(4)(R_1\ C_1)(10)(10^3)}$
- $\therefore$ $R_1\ C_1 = (0.5)\ (10^{-3})$sec
- Let C_1 = 0.05 µF$\therefore$ $R_1 = \frac{(0.5)(10^{-3})}{(0.05)\ (10^{-6})}$ = 10 KΩ
- **PROCEDURE**
- A) Connect the Circuit as per the Circuit diagram above
- B) switch on the Power supply
- C) observe the output waveform on the Oscilloscope. Measure the time period of the Triangular wave.
- Frequency of the Triangular wave is equal to the reciprocal of the measured time period
- Compare it with the theoretical value. Find out the % error which is $\frac{Theoretical-Practical}{Theoretical} \times 100$

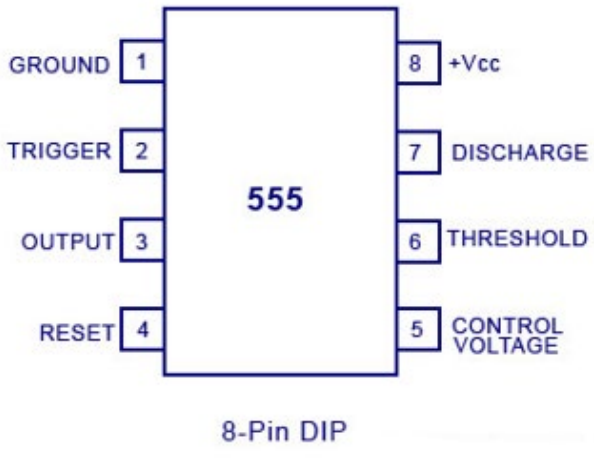
EXPERIMENT NO.8
MONOSTABLE MULTIVIBRATOR USING IC 555

- **AIM**: To Design a Monostable Multivibrator using IC 555 Timer to get 100 msecs pulse output

- **EQUIPMENT & COMPONENTS**

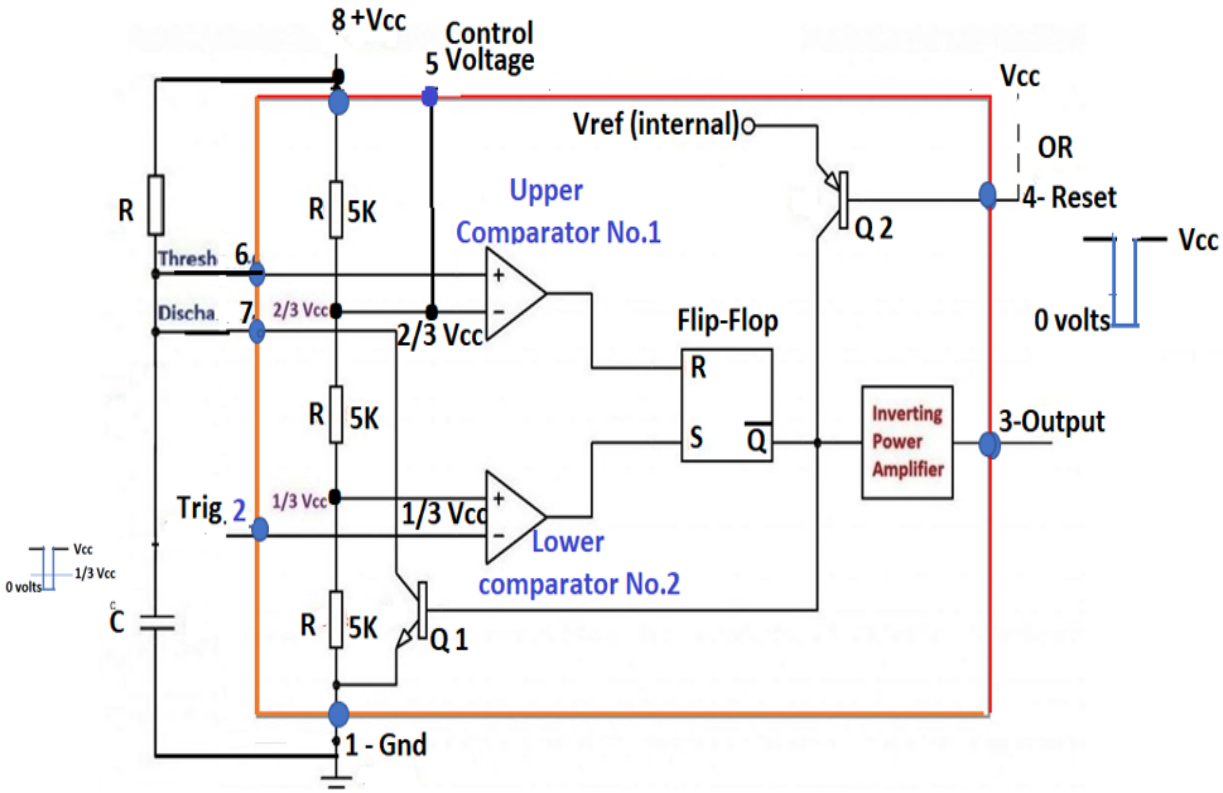
Sl.No.	Name and Specification	Quantity
1	Regulated Power Supply	1
2	Pulse Generator (0 – 10 MHz)	1
3	Oscilloscope 20 MHz	1
4	Bread Board	1
5	Timer IC 555	1
6	Diode	1
6	Resistors and capacitors	Assorted
7	Probes and Connecting wires	As required

- **THEORY:**
- IC 555 is basically a monolithic timing circuit that produces accurate and highly stable time delays or oscillations**.**
- Applications include dc-dc converters, digital logic probes, waveform generators, analog frequency meters , tachometers, temperature measurement and control devices, voltage regulators etc.
-



8-Pin DIP

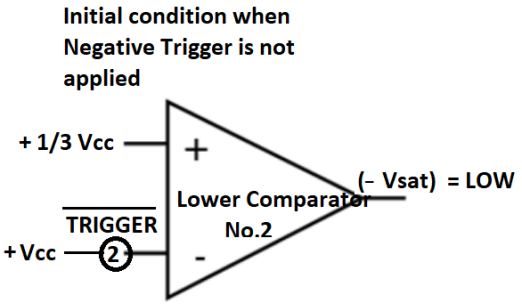
- The timer IC 555 works in three modes – i) one-shot or monostable multivibrator or ii) as a free-running or astable multivibrator or iii) can be used as Schmitt trigger

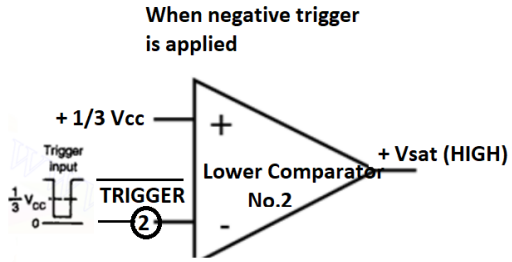


- **DESCRIPTION OF MONOSTABLE OPERATION:**
- **I) STANDBY STATE:**
- Flip-flop FF Q = low and $\bar{Q} = 1$. So transistor Q1 is ON. This clamps the external capacitor and connects it to ground. Capacitor is now in discharged mode.
- Since $\bar{Q} = 1$ is connected to Power amp which is an Inverter, output at pin no. 3 is LOW.

- **II) TRIGGER MODE OR "SET STATE" OF FF**
- Now negative trigger is applied to pin no.2 $(\overline{TRIGGER})$. As the trigger voltage passes through $\frac{Vcc}{3}$ and become less than $\frac{Vcc}{3}$ the

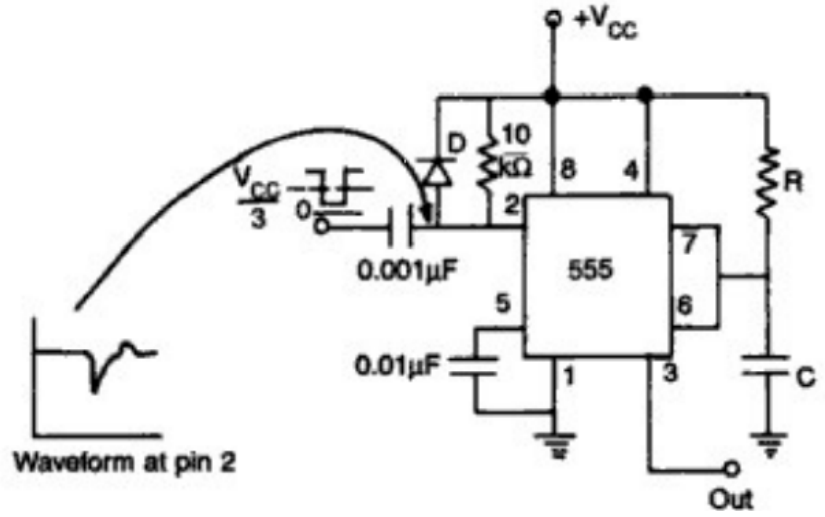
Lower comparator (No.2) changes state and goes to HIGH state from Low.

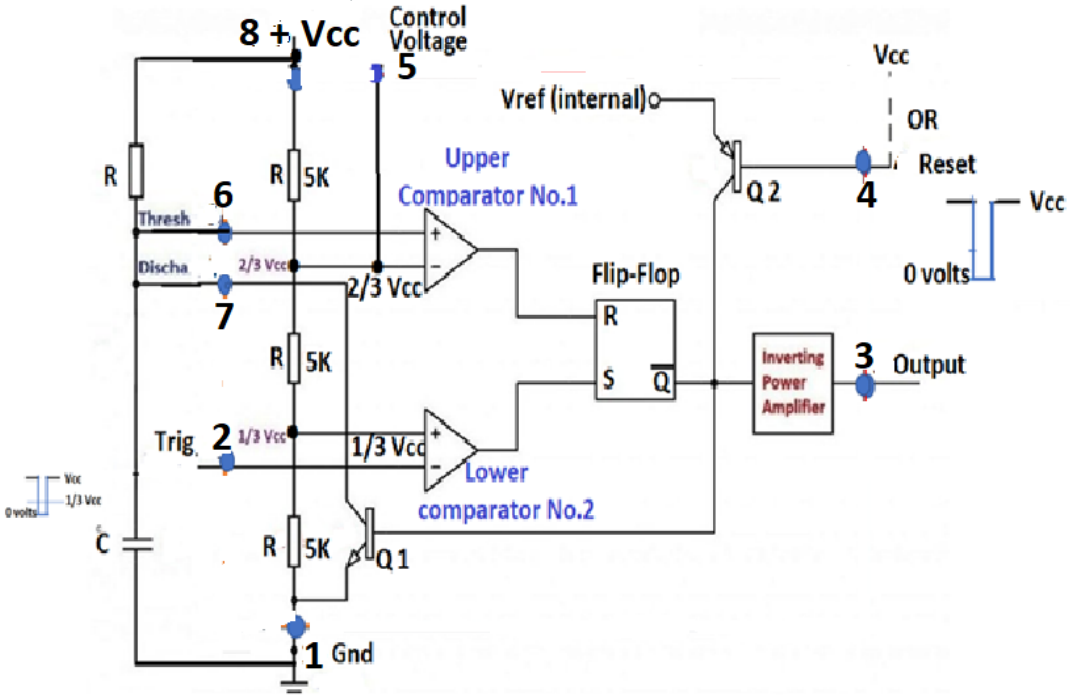
- 

- 

- **III). RESET STATE OF FF:**
- The rise in capacitor voltage is exponential with a time constant of RC.
  Upper comparator No.1, Inverting input is connected to a fixed voltage +2/3 Vcc. So the Comparator 1 is at (–Vsat) ie LOW. After a time period T the voltage across Capacitor reaches
- 2/3 Vcc and starts rising above 2/3 Vcc. This rising voltage is connected to Non inverting input of the comparator. The instant this becomes more than 2/3 Vcc, the comparator 1 output becomes(+ Vsat) HIGH. This is applied to the RESET terminal of FLIP-FLOP.
- FF now will be reset and Q= LOW and $\bar{Q}$ = HIGH . Since $\bar{Q}$ is connected to Output pin No.3 through an inverter, the output pin becomes LOW.
- $\bar{Q}$ (HIGH) is also connected to base of Transistor Q1 and the Q1 becomes ON.(transistor switch closes). This shorts the capacitor to ground. The cycle repeats with a new trigger pulse.
- **Pulse Width Of Monostable :**
- From theory Pulse width of monostable T = 1.1 R C secs

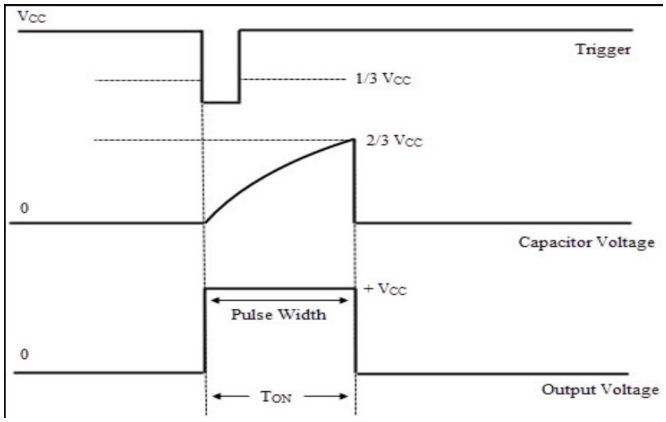
EXPERIMENT FOR MONOSTABLE





Let C= 1 µF and R= 100 KΩ

Then T = 1.1 x 100 x 10^3 x 1 x 10^{-6} = 0.11sec= 110 milli secs



PROCEDURE:

1.Connect the 555 timer as shown in the figure above

2, Connect the oscilloscope at the output terminal

3. Apply the input pulse from the pulse generator

4. Note down the input trigger (pin no.2) and output pulse (pin no.3) using the two channels of the Oscilloscope

5. Note down the output at pin no. 7 & 8 (charging of capacitor) and the output pulse (pin no. 3) using the two channels of the Oscilloscope

6. Measure the pulse width of the output pulse. This is the Monostable output

7. calculate the percentage error in pulse width

$= \frac{Theoritical - Practical}{Theorical} \times 100$

8. Change the value of Capacitor from 1 µF to 0.1 µF and repeat the above steps

RECORDINGS OF THE EXPERIMENT:

Sl.No	R	C	Theoretical Pulse width	Measured Pulse width	Error Percentage
1	100 K	1µF	110 millisecs		
2	100 K	0.1µF	11 millisecs		

QUESTIONS FOR VIVA – VOCE IN LESSON NO.8

1. List the important features of the 555 Timer.
2. What is the function of control input (pin5) of 555 timers?
3. List the applications of 555 timers in Monostable mode.

4. Why do we use negative trigger for Monostable operation?
5. Explain the trigger circuit used for Monostable multivibrator?
6. What are the applications of Monostable multivibrator
7. Consider 555 monostable multivibrator circuit. If RA = 10 kΩ, determine the value of C for output pulse duration of 1 msec.
8. For the above circuit, if RA = 10 kΩ and C = 0.1 μF, determine the value of fH.
9. In the case of 555 monostable circuit, if RA = 10 kΩ and C = 0.2 μF, calculate the time interval.
10. Design a Monostable multivibrator to produce an output pulse 2 msec wide

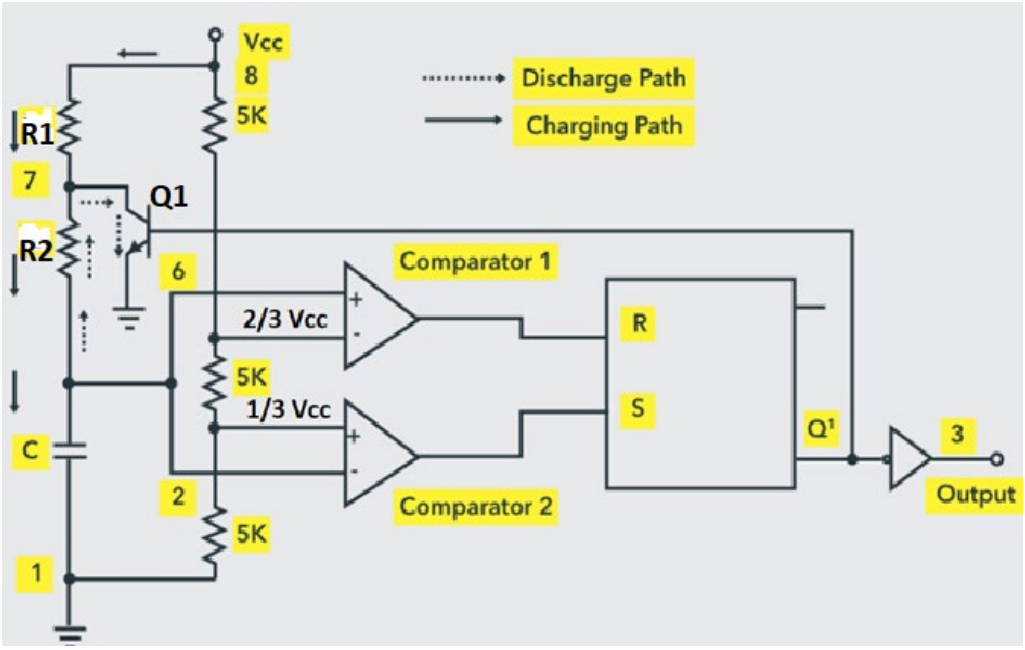
EXPERIMENT NO.9
ASTABLE MULTIVIBRATOR USING IC 555

AIM: To Design Astable Multivibrator using IC 555 Timer to get a frequency of 6900 Hzs and duty ratio of 52.38%

EQUIPMENT & COMPONENTS

Sl.No.	Name and Specification	Quantity
1	Regulated Power Supply	1
2	Pulse Generator (0 – 10 MHz)	1
3	Oscilloscope 20 MHz	1
4	Bread Board	1
5	IC 741 Op-Amp	1
6	Resistors and capacitors	Assorted
7	Probes and Connecting wires	As required

THEORY:



Astable Multivibrator often called a free-running Multivibrator. External Trigger input is not required to operate the 555 as an Astable Configuration. However, the time during which the output is either high or

low is determined by two external components **Resistor & Capacitor**. Figure shows the 555 as Astable Multivibrator. Initially, when the output is high, capacitor C starts charging towards Vcc through resistor R1 and R2. As soon as voltage across the capacitor equals to 2/3 Vcc, comparator 1 triggers the flip-flop, and the output becomes low. Now capacitor discharges through R2 and transistor Q1. When the voltage across capacitor C equals to 1/3Vcc, comparator2's output triggers the flip-flop, and the output goes high. Then the cycle repeats.

The output voltage waveforms are as shown in figure. In this way capacitor periodically charges and discharges between 2/3Vcc and 1/3Vcc respectively.

The time during which the capacitor charges from 1/3Vcc to 2/3 Vcc is equal to the ON time of the timer (i.e. the output is HIGH) and is given by t_c =0.69(R1+R2)C ---- (1)

The time during which the capacitor discharges from 2/3 Vcc to 1/3Vcc is equal to the OFF time of the timer, during which the output is LOW and is given by t_d =0.69 R2 C --- (2)

The total time period of the output is the sum of charging time

(t_c) and discharging time (t_d) and is given by

T = t_c + t_d = 0.69(R1 + 2R2) C --- (3)

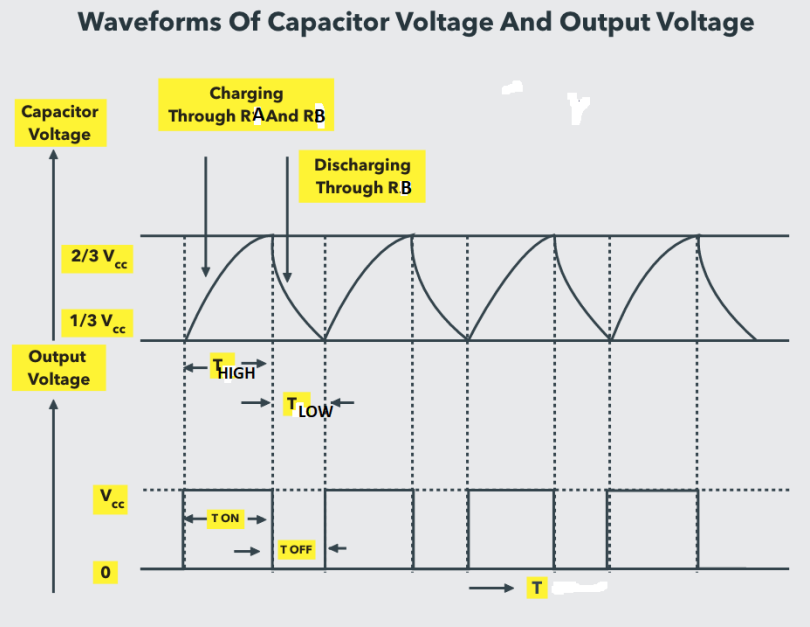
Therefore the frequency of oscillations of Astable multivibrator is given by

$$f = \frac{1}{T} = \frac{1}{0.69\ (R1 + 2R2)C} = \frac{1.45}{(R1 + 2R2)C}$$

DUTY CYCLE: This term is used in conjunction with Astable Multivibrator. The duty cycle is the ratio of the ON time, tc during which the output is high to the total time period T. It is generally expressed as a percentage.

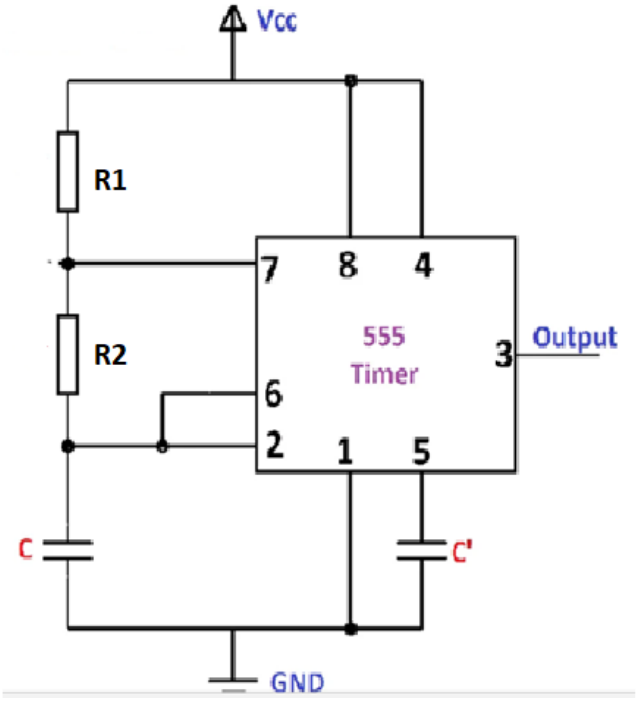
Duty cycle D (percent) =

$$\frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100 = \frac{t_C}{T} \times 100 = \frac{R1 + R2}{R1 + 2\,R2} \times 100$$



EXPERIMENT FOR ASTABLE MULTIVIBRATOR:

Design an Astable Multivibrator using IC 555 timer to generate a square wave of 6.9 KHz with 52.38 % Duty Cycle



DESIGN CALCULATIONS:

Let C= 0.01 μ f

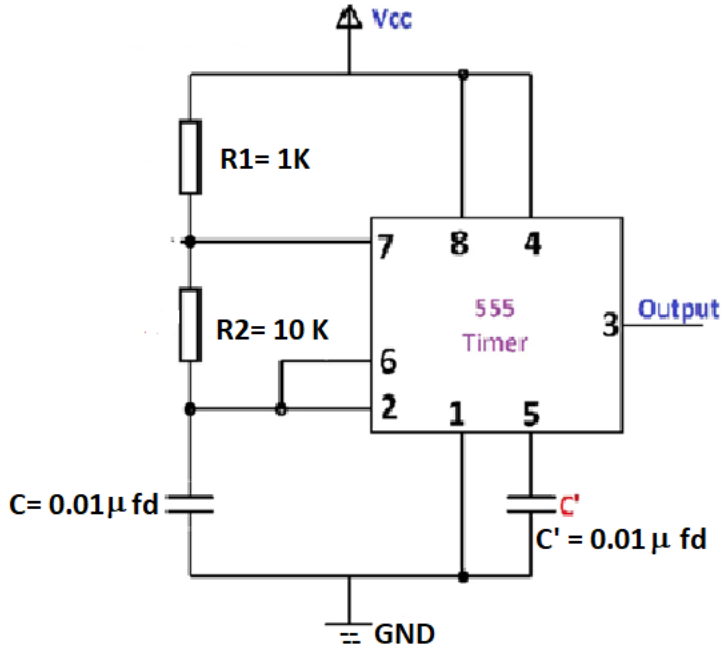
Frequency = 6900 = $\frac{1.45}{(R1+2\,R2)\,C} = \frac{1.45}{(R1+2\,R2) \times 0.01 \times 10^{-6}}$

(R1 + 2 R2) = 21014

Duty cycle = 0.5238 = $\frac{(R1+R2)}{(R1+2\,R2)} = \frac{(R1+R2)}{21014}$

R1 + R2 = 11007

Let R1 = 1000 = 1 KΩ Then R2 becomes 10007 = 10 KΩ



PROCEDURE:

1. Connect the IC 555 timer in Astable mode as shown in the figure. Connect the Oscilloscope at the output terminal (pin 3) and observe the output.
3. Record the waveforms at pin3, across the capacitor & compare them with the sample output waveforms as shown in figure
4. Measure the charging time (tc), discharging time (td) and total time period/ frequency from the output waveform.
5. Calculate tc, td, time period (T), frequency (f) of the square wave output and percentage duty cycle theoretically.
6. Change the capacitor value as per the table given below and repeat above steps

TABLE FOR ASTABLE MULTI VIBRATOR

C = 0.01 µfd R1=Rb = 1 K R2 =Ra =10 K							
Theoritical Values				Measured practical values			
tc	td	T	F Freque-ncy	tc	td	T	F Freque-ncy
75.9 µSEC	69 µSEC	144 µSEC	6.994 KHzs				
C = 0.047 µfd R1 = Rb = 1K R2 = Ra = 10 K							
Theoritical Values				Measured Practical values			
tc	td	T	F Freque-ncy	tc	td	T	F Freque-ncy
356 µSEC	324.4 µSEC	680.4 µSEC	1.47 KHZs				

EXPERIMENT NO.10
SCHMITT TRIGGER CIRCUITS USING IC 741

AIM: To Design and construct Schmitt trigger circuits using IC 741

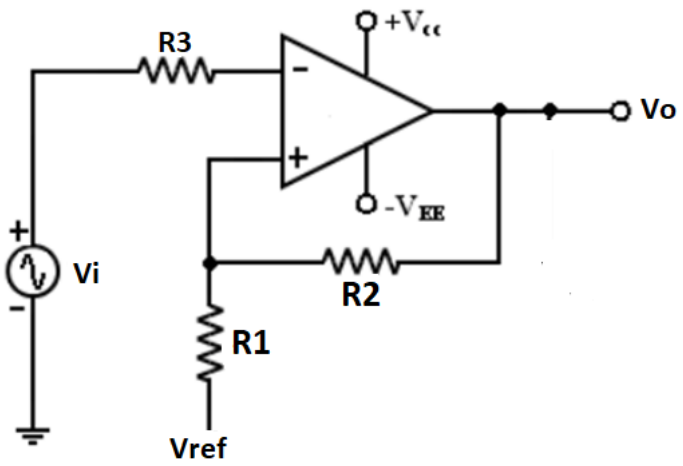
EQUIPMENT & COMPONENTS

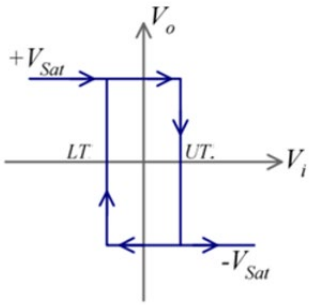
Sl.No.	Name and Specification	Quantity
1	Regulated Power Supply	1
2	Pulse Generator (0 – 10 MHz)	1
3	Oscilloscope 20 MHz	1
4	multimeter	1
5	Bread Board	1
6	Timer IC 555	1
7	Resistors and capacitors	Assorted
8	Probes and Connecting wires	As required

THEORY:

Circuit diagram of Schmitt trigger is shown in Figure. It's also called regenerative comparator. The input Voltage is applied to the inverting terminal & feed back voltage to the non-inverting terminal. $\mathbf{V_i}$ triggers the output $\mathbf{V_o}$ whenever $\mathbf{V_i}$ exceeds certain voltage levels. These voltages are Upper threshold voltage V_{UT} and Lower threshold voltage $V_{LT.}$ The hysteresis width is difference between these two values

SCHMITT TRIGGER CIRCUIT





As long as V_i is less than V_{UT} , V_o remains at + V_{sat}

Using Superposition theorem

$V_{UT} = \frac{Vref\ R2}{R1+R2} + \frac{R1\ Vsat}{R1+R2}$

When V_i is just greater than V_{UT} , V_o regeneratively switches to $-V_{sat}$ and remains at this level as long as $\mathbf{V_i > V_{LT}}$ (not V_{UT})

$V_{LT} = \frac{Vref\ R2}{R1+R2} - \frac{R1\ Vsat}{R1+R2}$

only when V_i is less than $\mathbf{V_{LT}}$, $\mathbf{V_o}$ switches to $+V_{sat}$ from $-V_{sat}$

$V_H = V_{UT} - V_{LT} = \frac{2\ R1\ V_{sat}}{R1+R2}$

EXPERIMENT FOR SCHMITT TRIGGER:

DESIGN CALCULATIONS:

Design the Schmitt trigger circuit with value of VUT = + 1 V and VLT = – 1 V .

2. For OP-AMP 741C let ± Vsat ≡ ±13V . Assume Vref = 0, so the another end of R1 is grounded.

$VUT = +1 = \frac{R1\ Vsat}{R1+R2} = \frac{R1 \times 13}{R1+R2}$

13 R1 =R1 + R2 So 12 R1 = R2

Let R1= 10 K

R2 = 120 K = say 100 K

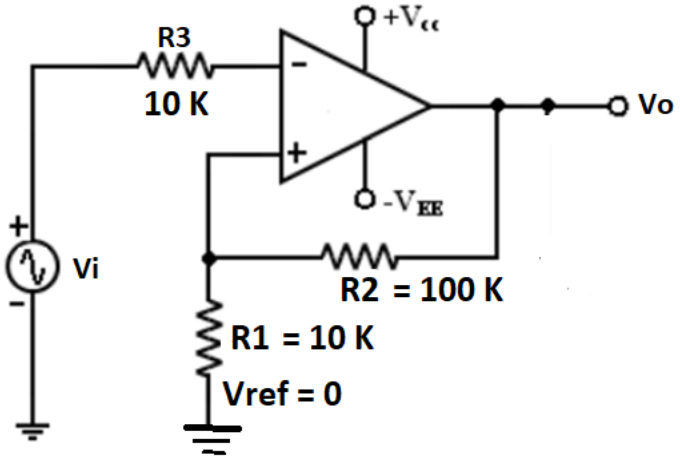
New value of VUT = $\frac{R1 \times 13}{R1+R2} = \frac{10 \times 10^3 \times 13}{10 \times 10^3 + 100 \times 10^3} = 1.182$

New value of VLT = –1.182

Hysteresis = 1.182 –(–1.182) = 2.364 V

$$R3 = R1 \,||\, R2 = \frac{R1 \times R2}{R1+R2} = 10K$$

SCHMITT TRIGGER CIRCUIT



PROCEDURE: 1.

1.Connect the circuit as shown Figure.

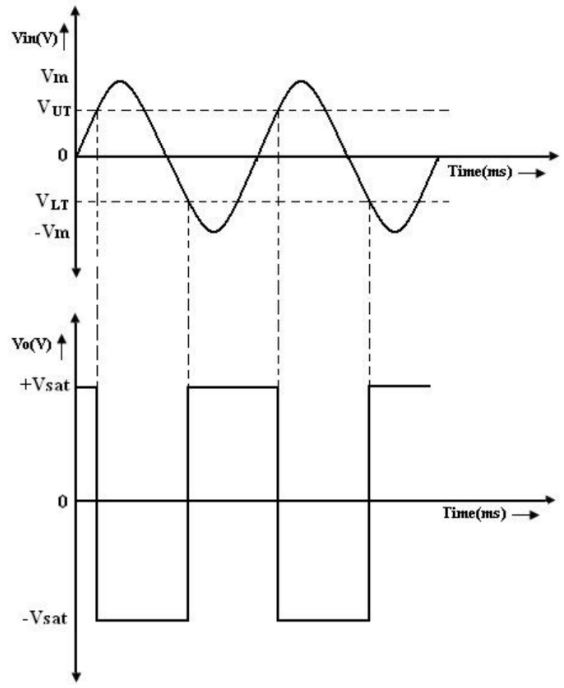
2. Apply Function Generator sinewave signal at input terminals Vi at 10V(p-p) & frequency 1KHz.

3. Connect oscilloscope - CH2 at output terminals Vo, Oscilloscope -CH1 at input terminals Vi.

4. Observe square wave output on for the given input sine wave & compare them with the sample waveform as shown in figure.

5. Note down the practical VUT , VLT and VH values in tabular column.

7. Compare the theoretical and practical values of VUT, VLT and VH



		Theoretical values			Practical values		
Sl.no	**Sine wave (Peak to peak)**	**Upper Thres-hold VUT Volts**	**Lower Thres-Hold VLT Volts**	**Hyster-esis Volts**	**Upper Thres-hold VUT**	**Lower Thres-Hold VLT**	**Hyster-esis**
1	20 V	+1.18	–1.18	2.36			
2	15 V	+1.18V	–1.18	2.36			
3	10 V	+1.18V	–1.18	2.36			

EXPERIMENT NO. 11
IC 565- PHASE LOCK LOOP

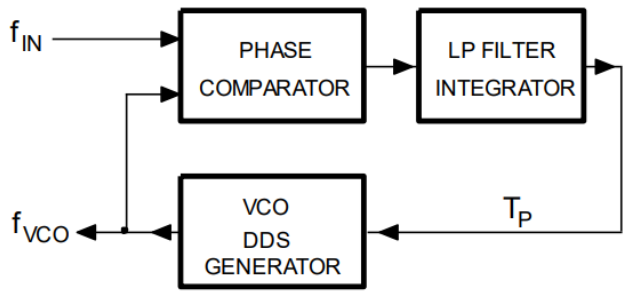
AIM: To measure the free running frequency, capture range and lock range of Phase Lock Loop (PLL)

EQUIPMENT & COMPONENTS

Sl.No.	Name and Specification	Quantity
1	Regulated Power Supply	1
2	Function Generator (0 – 10 MHz)	1
3	Oscilloscope 20 MHz	1
4	Bread Board	1
5	PLL IC 565	1
6	Resistors and capacitors	Assorted
7	Probes and Connecting wires	As required

THEORY:

The figure shows the phase-locked loop (PLL) in its basic form. The PLL consists of i) a phase detector ii) a low pass filter and iii) a voltage controlled oscillator as shown.



The phase detector, or comparator compares the input frequency f_{IN} with the feedback frequency f_{OUT}. The output of the phase detector is proportional to the phase difference between f_{IN} and f_{out}. The output voltage of a phase detector is a dc voltage and therefore is often referred to as the error voltage. The output of the phase detector is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level. This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in establishing the dynamic

characteristics of the PLL circuit. The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: free running, capture, and phase lock

Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phaselocked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phase-locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action

CAPTURE RANGE:

It is the frequency range ± Δ ω_C centered about ω_O , over which the PLL can acquire lock with an input signal. The capture range is affected by filter characteristics

LOCK RANGE:

When PLL is in lock, the frequency range ± ω_L , centered about ω_o , over which the loop can track the input is called Lock range. It is affected by the operating range of the phase detector and the VCO

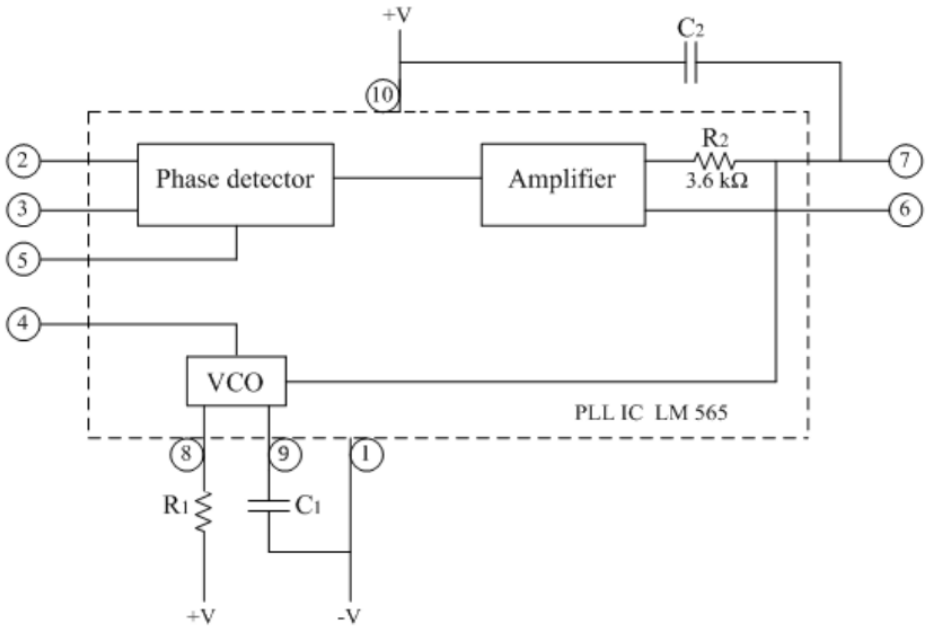
CAPTURE TIME OR PULL IN TIME :

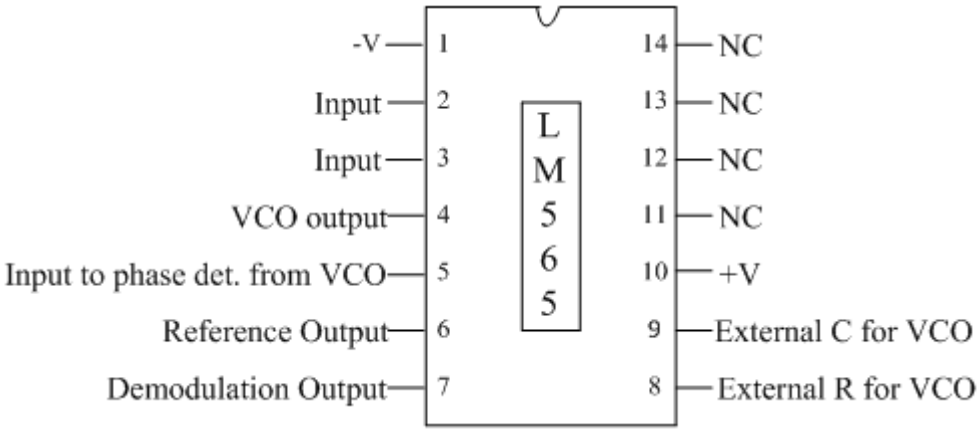
The Capture of an input signal does not take place as soon as the signal is applied, but it takes finite time. The total time taken by the PLL to establish a lock is called pull in time

FREE RUNNING FREQUENCY :

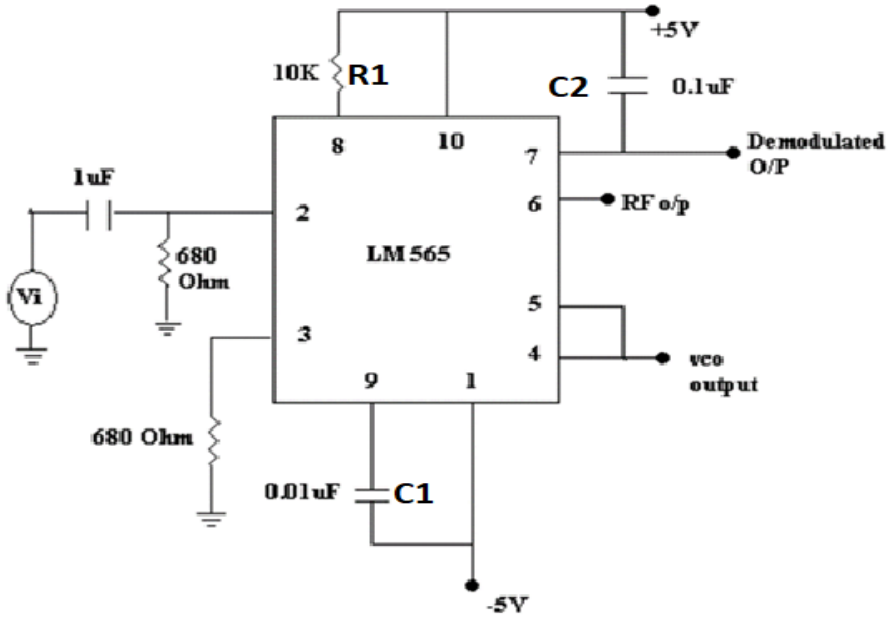
VCO is in free running mode when the control voltage is zero. The output frequency of free running VCO is called center frequency or free running frequency

Theoretically using the formula $f_0 = \frac{1.2}{4\,R_1\,C_1}$





EXPERIMENT FOR PLL:



DESIGN CALCULATIONS:

FREE RUNNING FREQUENCY :

Theoretically using the formula $f_0 = \frac{1.2}{4\ R_1\ C_1}$ =

$$\frac{1.2}{4\ (10 \times 10^3)\ \ (0.01 \times 10^{-6})} = 3030\ Hz$$

LOCK RANGE:

f_L= (+/–) $\frac{8\ f_0}{V}$ where V= + V –(–V), where is f_0 free running frequency

f_L= (+/–) $\frac{8\ (3030)}{10}$ = 2424 Hz

CAPTURE RANGE:.

$$f_C = \left[\frac{f_L}{2\,\pi\,R_F C_2}\right]^{1/2} = \left[\frac{f_L}{2\,\pi\,(3.6\times10^3)C_2}\right]^{1/2}$$

$$\left[\frac{2424}{2\,(3.14)\,(3.6\times10^3)(0.1\times10^{-6})}\right]^{1/2} = 1035\text{Hz}$$

Where 3.6 K is the fixed internal resistance in the IC NE 565

PROCEDURE:

1. Apply +5v to pin 10 and –5v to pin 1 of LM565
2. Connect R1= 10KΩ resistor from pin 8 to10 and C1 =0.01μF capacitor from pin 9 to 1.
3. Connect 680Ω resistor from pin 2 & pin 3 to ground.
4. Connect pin 4 (VCO o/p) to CRO and measure its frequency. This frequency is called the free running frequency, fo.
5. Calculate f_0 theoretically using the formula $f_0 = \frac{1.2}{4\,R_1\,C_1}$ and compare it with practical value.
6. Connect the circuit as shown in figure.
7. Apply square wave at the input with an amplitude of 2Vpp and also connect it to channel 1 of oscilloscope.
8. Connect pin 4 (VCO o/p) to channel 2 of Oscilloscope.
9. Vary the input signal frequency in steps and measure its corresponding o/p frequency.
10. Find the lock range and capture range from the obtained data. 11. Calculate lock range, f_L and capture range, f_C theoretically using formula

$f_L = (+/-)\ \frac{8\,f_0}{V}$ where V = +V- (-V) and

$$f_C = \left[\frac{f_L}{2\,\pi\,(3.6\times10^3)C_2}\right]^{1/2}$$

12. Compare theoretical and practical values.

S.No	Input frequency Hz	Output Frequency Hz	f_C in Hz	f_L in Hz

LESSON NO.12

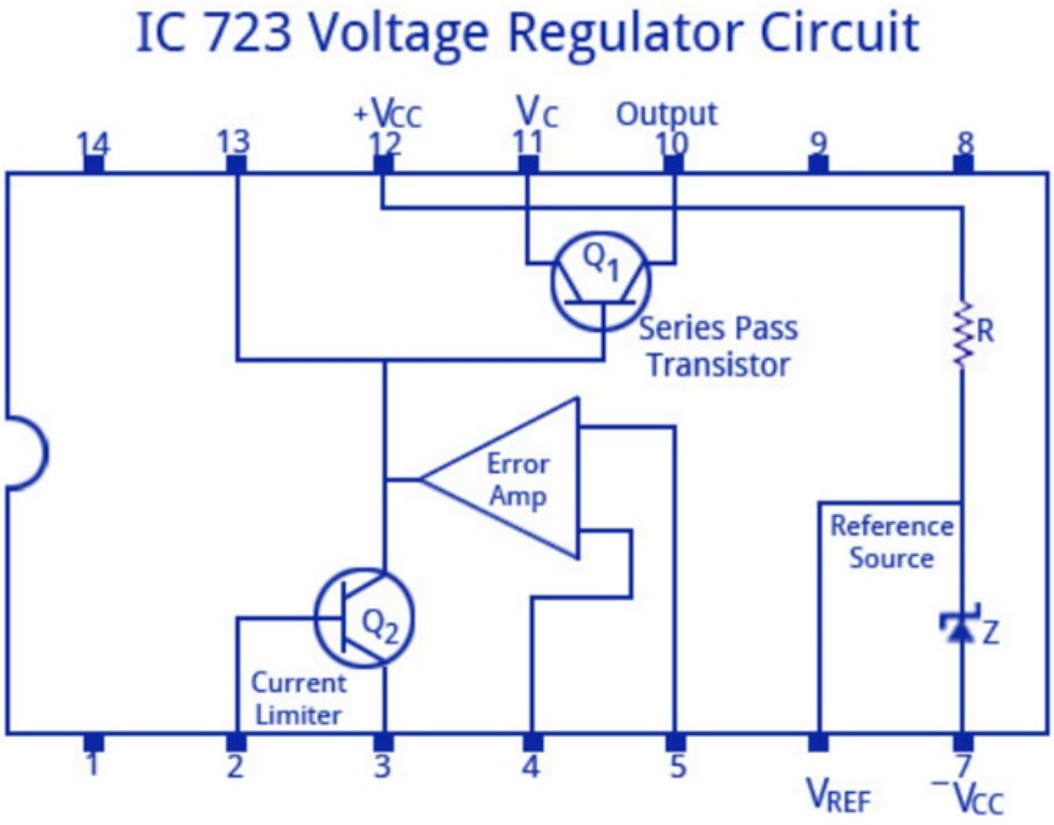
IC 723 – VOLTAGE REGULATOR

- **AIM**: AIM: Study the operation of Voltage regulator using IC 723 and plot the Line regulation and Load regulation characteristics

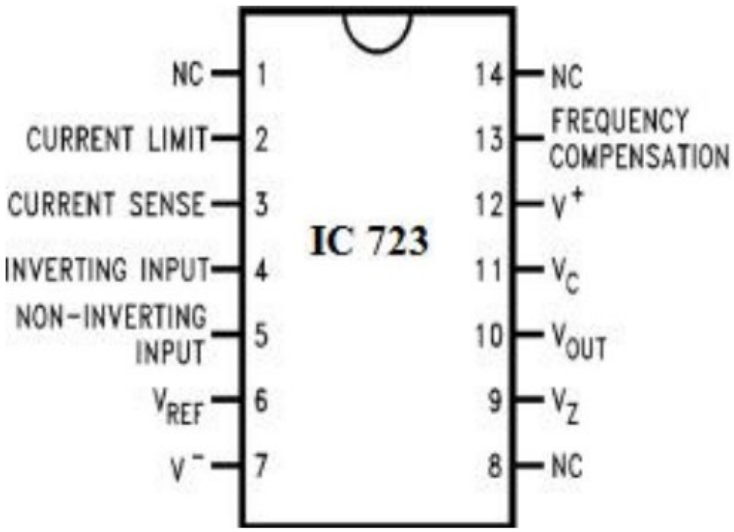
- **EQUIPMENT & COMPONENTS**

Sl.No.	Name and Specification	Quantity
1	IC 723	1
2	Dual power supply	1
3	Voltmeter	1
4	Ammeter	1
5	Resistors 3.3 K Ω , 4.7 KΩ , 100 Ω	1 each
6	Potentiometer 1 K Ω , 6 KΩ	1 each
7	Bread Board	1
8	Connecting wires and probes	As required

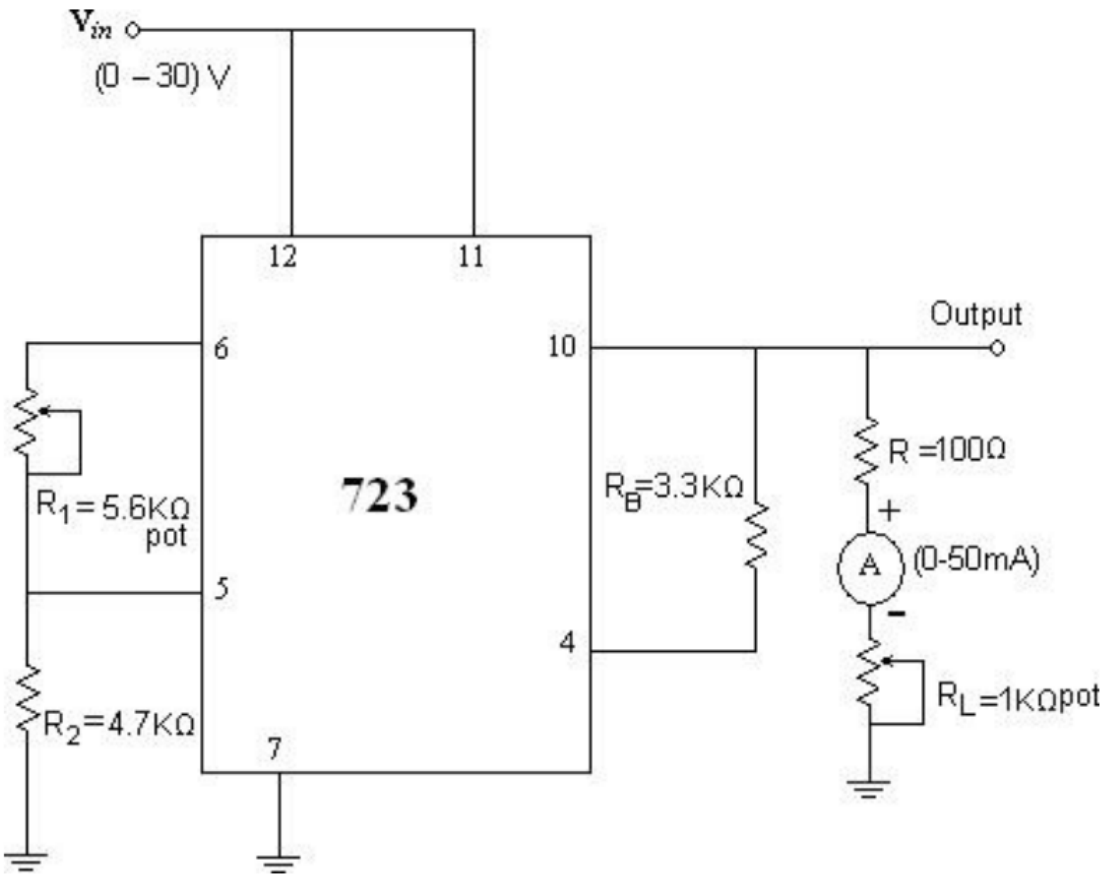
THEORY:



PIN DIAGRAM:


NC
1
CURRENT LIMIT
2
CURRENT SENSE
3
INVERTING INPUT
4
NON-INVERTING INPUT
5
V_{REF}
6
V^-
7
IC 723
14
NC
13
FREQUENCY COMPENSATION
12
V^+
11
V_C
10
V_{OUT}
9
V_Z
8
NC

CIRCUIT DIAGRAM:



A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage variations. Using IC 723, we can design both low voltage and high voltage regulators with adjustable voltages**.**

For a low voltage regulator, the output VO can be varied in the range of voltages Vo < Vref, where as for high voltage regulator, it is VO > Vref. The voltage Vref is generally about 7.5V. Although voltage regulators can be designed using OP-AMPs, it is quicker and easier to use IC voltage regulators

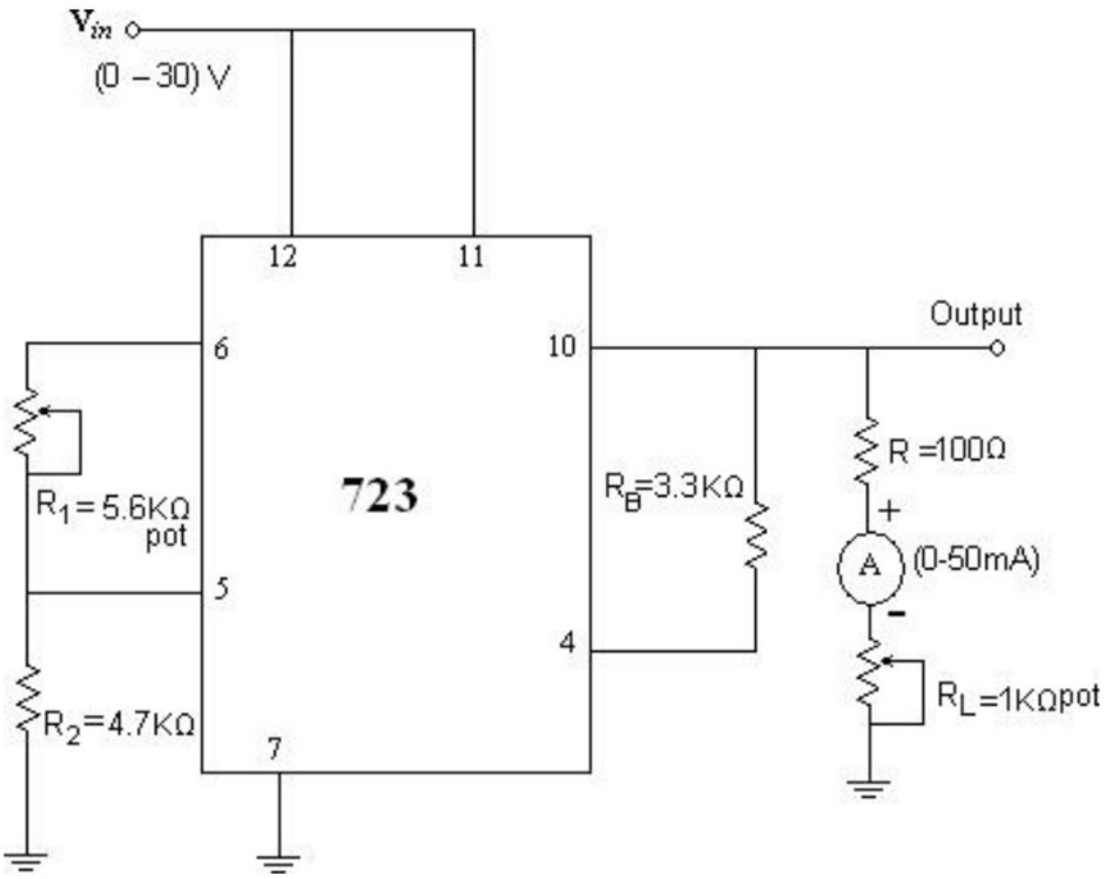
IC 723 is a general purpose regulator and is a 14-pin IC with internal short circuit current limiting, thermal shutdown, current/voltage boosting etc. Furthermore it is an adjustable voltage regulator which can be varied over both positive and negative voltage ranges. By simply varying the connections made externally, we can operate the IC in the required mode

of operation. Typical performance parameters are line and load regulations which determine the precise characteristics of a regulator

MAIN FEATURES

1. The minimum voltage that can be achieved from IC 723 Regulator Circuit is 2 V, and the maximum is around 37 V.
2. The peak voltage that can handled by the IC is 50 V in pulsed form, and 40 V is the maximum continuous voltage limit.
3. The maximum output current from this IC is 150 mA which can be upgraded to as high as10 amps through an external series pass transistor integration.
4. The maximum tolerable dissipation of this IC 500 mW, therefore it should be mounted on a suitable heatsink in order to allow optimal performance from the device.
5. Being a linear regulator, the IC 723 needs an input supply that should be at least 3 V higher than the desired output voltage, and the maximum difference between the input and the output voltage should never be allowed to exceed 37 V.

CIRCUIT DIAGRAM:



DESIGN CALCULATIONS:

Assume IO=1mA,

VR=7.5V, RB = 3.3 kΩ

For given Vo = 5 Volts

R2 = $\frac{V0}{IO}$ = $\frac{5}{1 \times 10^{-3}}$ = 5 KΩ we can use 4.7 KΩ

R1 = $\frac{VR - V0}{IO}$ = $\frac{7.5 - 5}{1 \times 10^{-3}}$ = 2.5 KΩ we can use a 10 K potentiometer to adjust the output voltage to 5 V

R3 = $\frac{R1 \times R2}{R1 + R2}$ = $\frac{10K \times 4.7K}{10K + 4.7K}$ = 3.2 K we can use 3.3 KΩ

Similarly for given Vo = 3 Volts

R2 = $\frac{V0}{IO}$ = $\frac{3}{1 \times 10^{-3}}$ = 3 KΩ we can use 3 KΩ

R1 = $\frac{VR - V0}{IO}$ = $\frac{7.5 - 3}{1 \times 10^{-3}}$ = 4.5 KΩ we can use a

10 K potentiometer to adjust the output voltage to 5 V
R3 can be same as above ie 3.3 K

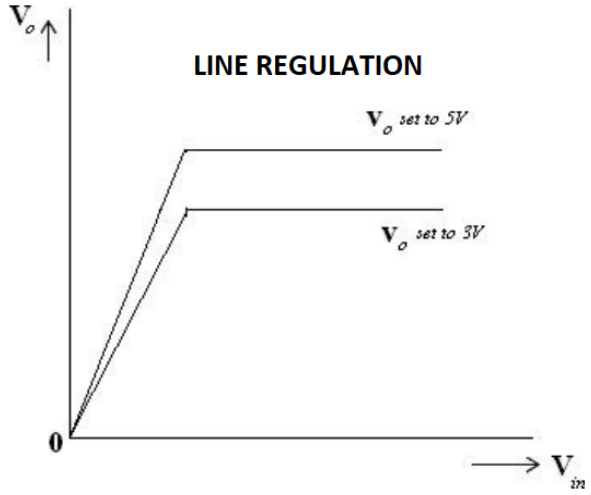
PROCEDURE FOR EXPERIMENT:

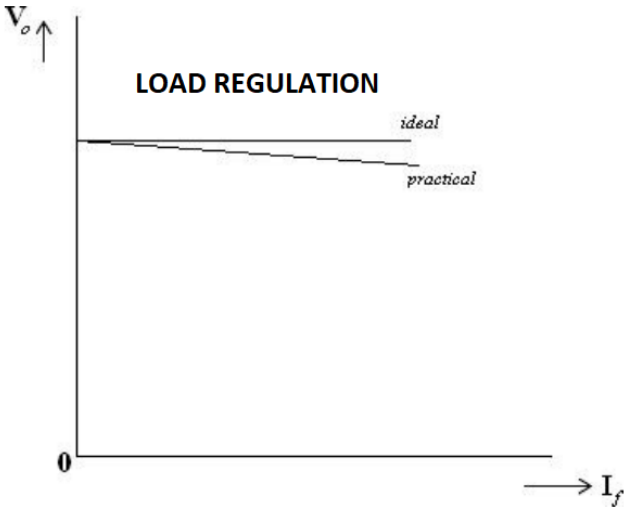
A) LINE REGULATION:

1. Connect the circuit as shown in figure.
2. Obtain R1 and R2 forVo = 5V
3. By varying Vin from 2 to 10V, measure the output voltage Vo. 4. Draw the graph between Vin and Vo as shown in model graph 5. Repeat the above steps for Vo = 3V.

B) LOAD REGULATION:

1. Set Vi such that VO = 5 V
2. By varying RL (1K pot) measure IL (in steps of 1 ma) and note down Vo
3. Plot the graph between IL and Vo as shown in model graph
4. Repeat the above steps for Vo = 3V





LINE REGULATION

Vi (V)	Output set to 5V	Output set to 3V
	Vo (V)	Vo (V)
O		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

LOAD REGULATION

Load current IL (ma)	output set to 5 V	Output set to 3 V
	Vo (V)	Vo (V)

LINE REGULATION:

Vi	Output set to 5 V
	Vo
8 V	(X1)
10 V	(X2)

Line regulation $= \frac{\Delta VO}{\Delta Vi} \times 100 = \frac{(X2 - X1)}{(10-8)} \times 100$

LOAD REGULATION:

IL (ma)	OUTPUT set to 5 V
	Vo
(A)	(M1)
(B)	(M2)

Load Regulation= $\frac{\Delta VO}{\Delta IL} \times 100 = \frac{(M2-M1)}{(B-A)} \times 100$

LESSON NO.13
THREE TERMINAL VOLTAGE REGULATORS 7805, 7809, 7912

AIM: TO study the 3-terminal fixed voltage regulator using IC 78XX and 79XX series and to find line regulation and load regulation characteristics

EQUIPMENT & COMPONENTS

Sl.No.	Name and Specification	Quantity
1	IC 7805	1
2	IC 7809	1
3	IC 7912	1
4	DIGITAL MULTIMETER	1
5	RESISTORS	As Required
6	Bread Board	1
7	Connecting wires and probes	As required

THEORY:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage. IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/ voltage boosting, internal short circuit current limiting, thermal shunt down and floating operation for high voltage application

POSITIVE VOLTAGE REGULATORS: 78xx is the series of three terminal positive voltage regulators in which xx indicate the output voltage rating of the IC

7805: This is a three terminal regulator which gives a regulated output of +5V fixed. The maximum unregulated input voltage which can be applied to 7805 is 35V.

7809: This is also three terminal fixed regulator which gives regulated voltage of +9V

NEGATIVE VOLTAGE REGULATORS: 79xx is the series of negative voltage regulators which gives a fixed negative voltage as output according to the value of xx.

7912: This is a negative three terminal voltage regulator which gives a output of −12V

LINE REGULATION: It is defined as the change in the output voltage for a given change in the input voltage. It is expressed as a percentage of output voltage or in millivolts

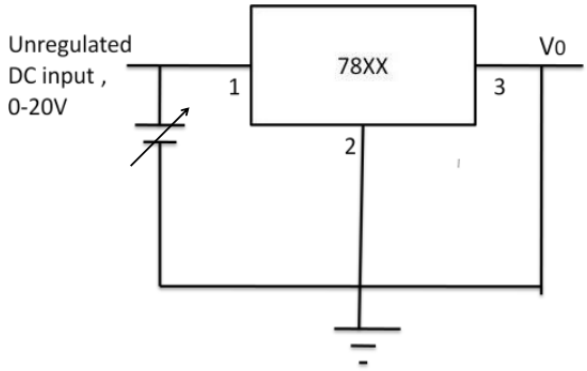
%RL = $\frac{\Delta V_0}{\Delta V_{in}}$ x 100

LOAD REGULATION: It is the change in output voltage over a given range of load currents that is from full load to no load. It is usually expressed in millivolts or as a percentage of output voltage

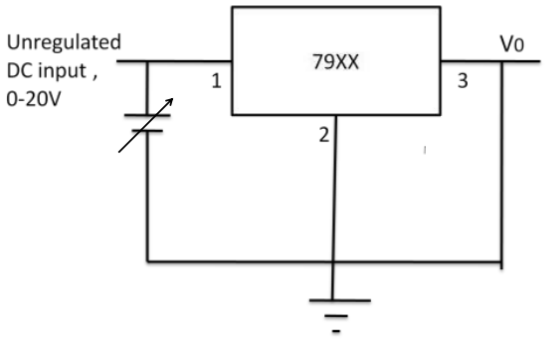
%R Load = $\frac{(Vnl-Vfl)}{Vnl}$ X 100

EXPERIMENT:

(a) Fixed Positive Voltage Regulator



(b) Fixed Negative Voltage Regulator



PROCEDURE:

(A) LINE REGULATION: 1. Connect the circuit diagram as shown in figure.

2. Apply the unregulated voltage to the input of IC 78XX/ 79XX and note down the regulator output voltage.

3. Vary input voltage from 1V to 15V for 78XX and -1V to -15V for 79XX and record the output voltages.

4. Calculate the line regulation of the regulator using the formula

Line Regulation = ΔVo / ΔVin × 100

LINE REGULATION

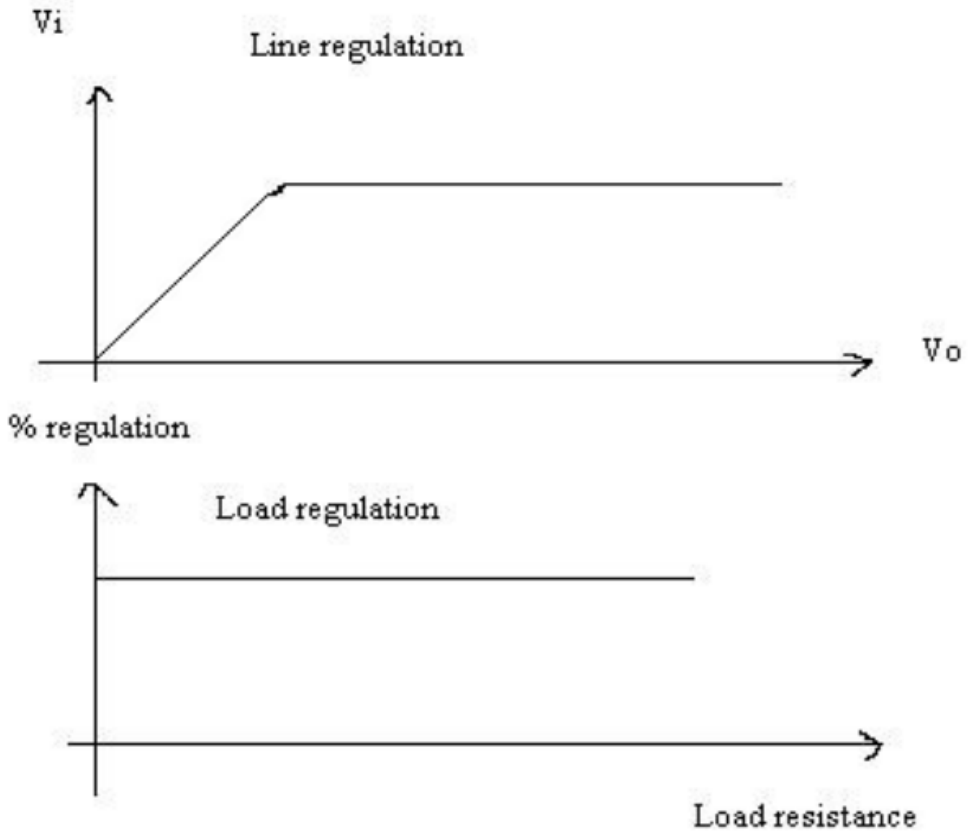
IC 7805		IC 7809		IC 7912	
LINE VOLTAGE Vin (V)	**OUTPUT VOLTAGE Vo (V)**	**LINE VOLTAGE Vin (V**	**OUTPUT VOLTAGE Vo (V**	**LINE VOLTAGE Vin (V)**	**OUTPUT VOLTAGE Vo (V)**

(B) LOAD REGULATION

1. Connect the circuit diagram as shown in figure.
2. Replace the fixed resistance by a decade resistance box.
3. Vary the load resistance in regular steps of 1 kΩ.
4. Note down the corresponding output across the load using voltmeter.
5. Calculate the load regulation of the regulator using the formula

Load Regulation = %R Load = $\frac{(Vnl-Vfl)}{Vnl}$ x 100

Regulated Output VFL (V)	Load Current IL (mA) Load	Resistance RL (kΩ)	% Load Regulation


Vi
Line regulation
Vo
% regulation
Load regulation
Load resistance