ANALOG AND DIGITAL ELECTRONICS

Subject Code: CS301ES Regulations : R18 - JNTUH

Class: II Year B.Tech CSE I Semester



Department of Computer Science and Engineering Bharat Institute of Engineering and Technology Ibrahimpatnam-501510,Hyderabad



ANALOG AND DIGITAL ELECTRONICS (CS301ES) COURSE PLANNER

I. COURSE OVERVIEW:

The course has been designed to introduce fundamental principles of analog and digital electronics. The students completing this course will understand basic analog and digital electronics, including semiconductor properties, operational amplifiers, combinational and sequential logic and analog-to-digital digital-to-analog conversion techniques. Finally, students will gain experience in with the design of analog amplifiers, power supplies and logic devices.

II. PREREQUISITS:

- 1. Basic Electronics
- 2. Number Systems

III. COURSE OBJECTIVES:

1.	To introduce components such as diodes, BJTs and FETs.
2.	To know the applications of components.
3.	To give Understand of various types of amplifier circuits.
4.	To learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
5.	To understand the concepts of combinational logic circuits and sequential circuits.

IV. COURSE OUTCOMES:

S.No.	Outcomes	Bloom's Taxonomy Level
1.	Know the characteristics of various components.	Knowledge, Understand (Level1, Level2)
2.	Understand the utilization of components.	Apply, Create (Level 3, Level 6)
3.	Design and analyze small signal amplifier circuits.	Analyze (Level 4)
4.	Learn Postulates of Boolean algebra and to minimize combinational functions.	Knowledge, Understand (Level1, Level2)
5.	Design and analyze combinational and sequential circuits.	Analyze (Level 4)
6.	Know about the logic families and realization of logic gates.	Knowledge, Understand (Level1, Level2)

V. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (PO)	Level	Proficiency assessed by
PO1	Engineering Knowledge : Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Assignments



		Z	November 1997
	Program Autcomes (PA)	Level	Proficiency
		Lever	assessed by
	Problem Analysis: Identify, formulate, review research		
PO2	literature, and analyze complex engineering problems	2	Examples
101	reaching substantiated conclusions using first principles of	_	Linumpies
	mathematics, natural sciences, and engineering sciences.		
	Design/ Development of Solutions: Design solutions for		
	complex engineering problems and design system		Assignments.
PO3	components or processes that meet the specified needs with	3	Exercises
	appropriate consideration for the public health and safety,		Literenses
	and the cultural, societal, and environmental considerations.		
	Conduct Investigations of Complex Problems: Use		
	research-based knowledge and research methods including		
PO4	design of experiments, analysis and interpretation of data,	-	-
	and synthesis of the information to provide valid		
	conclusions.		
	Modern Tool Usage: Create, select, and apply appropriate		
PO5	techniques, resources, and modern engineering and IT tools	_	_
105	including prediction and modeling to complex engineering		
	activities with an Understand of the limitations.		
	The Engineer and Society: Apply reasoning informed by		
PO6	the contextual knowledge to assess societal, health, safety,	_	_
100	legal and cultural issues and the consequent responsibilities		
	relevant to the professional engineering practice.		
	Environment and Sustainability: Understand the impact of		
PO7	the professional engineering solutions in societal and	_	_
107	environmental contexts, and demonstrate the knowledge of,		
	and need for sustainable development.		
	Ethics : Apply ethical principles and commit to professional		
PO8	ethics and responsibilities and norms of the engineering	-	-
	practice.		
	Individual and Team Work: Function effectively as an		Orral
PO9	individual, and as a member or leader in diverse teams, and	1	Discussions
	in multidisciplinary settings.		Discussions
	Communication: Communicate effectively on complex		
	engineering activities with the engineering community and		
PO1	with society at large, such as, being able to comprehend and	2	Document
0	write effective reports and design documentation, make	2	Preparation,
	effective presentations, and give and receive clear		Presentation
	instructions.		



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	Program Outcomes (PO)	Level	Proficiency assessed by
PO1 1	Project management and finance : Demonstrate knowledge and Understand of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	3	Assignments
PO1 2	Life-Long Learning : Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.	2	Assignments

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: None

VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

	Program Specific Outcomes	Leve l	Proficiency assessed by
PSO 1	Foundation of Mathematical Concepts: To use mathematical methodologies to crack problem using suitable mathematical analysis, data structure and suitable algorithm.	2	Lectures, Assignment s
PSO 2	Foundation of Computer System: The ability to interpret the fundamental concepts and methodology of computer systems. Students can understand the functionality of hardware and software aspects of computer systems.	1	Tutorials
PSO 3	Foundations of Software Development: The ability to grasp the software development life cycle and methodologies of software systems. Possess competent skills and knowledge of software design process. Familiarity and practical proficiency with a broad area of programming concepts and provide new ideas and innovations towards research.	-	-

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: None

VII.SYLLABUS:

UNIT – I: Diodes and Applications: Junction diode characteristics: Open circuited p-n junction, p-n junction as a rectifier, V-I characteristics, effect of temperature, diode resistance, diffusion capacitance, diode switching times, breakdown diodes, Tunnel diodes, photo diode, LED.

Diode Applications - clipping circuits, comparators, Half wave rectifier, Full wave rectifier, rectifier with capacitor filter.

UNIT – II: BJTs: Transistor characteristics: The junction transistor, transistor as an amplifier, CB, CE, CC configurations, comparison of transistor configurations, the operating point, self-bias or Emitter bias, bias compensation, thermal runaway and stability, transistor at low frequencies, CE amplifier response, gain bandwidth product, Emitter follower, RC coupled amplifier, two cascaded CE and multistage CE amplifiers.



UNIT-III: FETs and Digital Circuits: FETs: JFET, V-I characteristics, MOSFET, low frequency CS and CD amplifiers.

Digital Circuits: Digital (binary) operations of a system, OR gate, AND gate, NOT, EXCLUSIVE OR gate, De Morgan Laws, NAND and NOR DTL gates, modified DTL gates, HTL and TTL gates, output stages, RTL and DCTL, CMOS, Comparison of logic families.

UNIT – IV: Combinational Logic Circuits: Basic Theorems and Properties of Boolean Algebra, Canonical and Standard Forms, Digital Logic Gates, The Map Method, Product-of-Sums Simplification, Don't-Care Conditions, NAND and NOR Implementation, Exclusive-OR Function, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.

UNIT – V: Sequential Logic Circuits: Sequential Circuits, Storage Elements: Latches and flip flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Shift Registers, Ripple Counters, Synchronous Counters, Random-Access Memory, Read-Only Memory.

TEXT BOOKS:

1. Integrated Electronics: Analog and Digital Circuits and Systems, 2/e, Jaccob Millman,

Christos Halkias and Chethan D. Parikh, Tata McGraw-Hill Education, India, 2010.

2. Digital Design, 5/e, Morris Mano and Michael D. Cilette, Pearson, 2011.

REFERENCE BOOKS:

1. Electronic Devices and Circuits, Jimmy J Cathey, Schaum's outline series, 1988.

2. Digital Principles, 3/e, Roger L. Tokheim, Schaum's outline series, 1994.

NPTEL Web Course: <u>https://nptel.ac.in/courses/108102095</u>

https://nptel.ac.in/courses/117106086

NPTEL Video Course: <u>https://nptel.ac.in/courses/108102095</u>

https://nptel.ac.in/courses/117106086

GATESYLLABUS:DigitalLogic:

Boolean algebra. Combinational and sequential circuits. Minimization. Number representations and computer arithmetic (fixed and floating point).

Session	Week	Unit	Topics	Course Learning Outcomes	Teaching Methodolog y	Reference				
1			Unit-I: Introduction	Know the physics of P-N junction.	Chalk and Talk	T1, T2				
2	1	1	1	1	1 1	1 1	Open circuited P-N junction	Understand the open circuited P-N junction.	Chalk and Talk	T1, T2
3			P-N junction as a rectifier	Understand how the diode acts as rectifier and study the characteristics of rectifiers.	Chalk and Talk	T1, T2				

VIII.COURSE PLAN (WEEK-WISE):

					Any ALLAND RATE AND DOTOR							
4			V-I Characteristics	Understand the V characteristics of P-N junction.	Chalk and Talk	T1, T2						
5			Effect of temperature,	Understand the temperature	Chalk and	Т1 Т2						
5			diode resistance	effects and diode resistance	Talk	11, 12						
6			Diffusion Capacitance,	Know about drift and	Chalk and	Т1 Т2						
0			**. Drift Capacitance	diffusion capacitances.	Talk	11, 14						
7	2		Diode switching times	Understand diode switching times.	Discussion	T1, T2						
8			Breakdown diodes	Understand the concept of breakdown in diodes and study the operation and characteristics of Zener diode.	Chalk and Talk	T1, T2						
9			Tunnel diode	Understand the operation, characteristics and applications of tunnel diode	Chalk and Talk	T1, T2						
10	3		Photo diode, LED	Understand the operation, characteristics and applications of photo diode and LED.	Chalk and Talk	T1, T2						
11			Clipping circuits,	Explain clipping circuits,	Chalk and	T1 T2						
11			Comparators	comparators.	Talk, PPTs	11, 12						
12									Half wave rectifier	Understand how the diode acts as rectifier and study the characteristics of rectifiers.	Chalk and Talk, PPTs	T1, T2
13			Full wave rectifier	Understand how the diode acts as rectifier and study the characteristics of rectifiers.	Chalk and Talk, PPTs	T1, T2						
14	4		Rectifier with capacitor filter	Understand the general conditions for filters and study the rectifier with capacitor filter.	Chalk and Talk, PPTs	T1, T2						
15			Revision									
16			Mock Test-I									
17	5	2	<u>Unit-II</u> : Transistor characteristics: The junction transistor	Understand the basics of transistors.	Chalk and Talk, PPTs	T1, T2						
18			Transistor as an amplifier	Study the operation of transistor as an amplifier.	Chalk and Talk, PPTs	T1, T2						

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19			CB, CE, CC	Study the characteristics of	Chalk and	т1 т2				
17			Configurations	CB,CE,CC configurations.	Talk, PPTs	11, 12				
20			CB, CE, CC	Study the characteristics of	Chalk and	т1 т2				
20			Configurations	CB,CE,CC configurations.	Talk, PPTs	11, 12				
21			Bridge Class							
22							Comparison of transistor configurations	Compare various configurations of transistors.	Chalk and Talk	T1, T2
23	6		Operating point, Self- bias or Emitter bias	Understand the concept of operating point and purpose of biasing.	PPTs, discussions	T1, T2				
24			Bias Compensation, Thermal Runaway and Stability	Studyaboutbiascompensation,thermalrunawayandstability.stability.stability.stability.	Chalk and Talk	T1, T2				
25			Transistor at low	Explain the operation of	Chalk and	T1,				
23			frequencies	transistor at low frequencies.	Talk	T2, R1				
26	7		CE Amplifier Response, Gain Bandwidth Product	Explain the operation of CE amplifier, study its frequency response and gain bandwidth product.	Chalk and Talk, PPTs	T1, T2, R1				
27			Bridge Class							
28			Emitter Follower	Understand the operation of emitter follower.	Chalk and Talk	T1, T2				
29			RC Coupled Amplifier, Two Cascaded CE and Multistage CE Amplifiers	Explain the operation of RC coupled two cascaded CE and multistage CE amplifiers.	Chalk and Talk	T1, T2				
30	8		<u>Unit-III</u> : JFET, V-I Characteristics	Understand the operation, V-I characteristics of JFET.	Chalk and Talk, PPTs	T1, T2				
31			MOSFET	Understandthe operation,V-IcharacteristicsofMOSFFET.	Chalk and Talk, PPTs	T1, T2				
32		3	Bridge Class							
33	9	5	Low frequency CS and CD Amplifiers	Understand the operation of low frequency CS and CD amplifiers.	Chalk and Talk, PPTs	T1, T2				
34			Digital (binary) operations of a system,	Understand the arithmetic operations carried by digital	Chalk and Talk, PPTs	T1, T2				



					Approximation of the largest program of the l	
			**. Boolean Laws,	systems.		
			De Morgan Laws			
35			OR, AND, NOT, EX- OR, NAND and NOR DTL Gates, Modified	Understand the OR, AND, NOT, EX-OR, NAND and NOR DTL gates and	Chalk and Talk, PPTs	T1, T2
			DTL Gates	modified DTL gates.	, ~	
36			I Mid Examinations (W	(eek 9)		
			OR, AND, NOT, EX-	Understand the OR. AND.		
37			OR, NAND and NOR DTL Gates, Modified DTL Gates	NOT, EX-OR, NAND and NOR DTL gates and modified DTL gates	Chalk and Talk, PPTs	T1, T2
38	10	3	HTL and TTL Gates, Output Stages	Understand the HTL and TTL gates and their out put stages.	Chalk and Talk, PPTs	T1, T2
39			RTL, DCTL and CMOS	Understand the RTL, DCTL and CMOS gates.	Chalk and Talk, PPTs	T1, T2
40			Comparison of Logic Families	Comparevariouslogicfamilies.	Chalk and Talk, PPTs	T1, T2
41			Bridge Class			
42			<u>Unit-IV</u> : Introduction to Combinational Logic Circuits	Understand the design and analysis of combinational logic circuits.	Chalk and Talk, PPTs	T1, T2
43	11		Basic Theorems and Properties of Boolean Algebra	Learn Boolean algebra and logical operations in Boolean algebra.	Chalk and Talk, PPTs	T1, T2
44			Canonical and Standard Forms		Chalk and Talk, PPTs	T1, T2
45			Bridge Class			
46		4	Digital Logic Gates	Identify basic building blocks of digital systems.	Chalk and Talk, PPTs	T1, T2
47	12		The Map Method	AnalyzetoavoidtheredundanttermsinBoolean	Chalk and Talk, PPTs	T1, T2
48			Product-of-Sums Simplification, Don't- Care Conditions	functions	Chalk and Talk, PPTs	T1, T2
49	12		NAND and NOR Implementation	Design functions using universal gates.	Chalk and Talk, PPTs	T1, T2
50	13		Exclusive-OR Function	Understand the EX-OR function.	Chalk and Talk, PPTs	T1, T2



51			**. Binary Adders	Understand the design and analysis of combinational logic circuits.	Chalk and Talk, PPTs	T1, T2
52			Bridge Class			
53			Binary Adder- Subtractor, Decimal Adder	Understand the design and analysis of combinational logic circuits.	Chalk and Talk, PPTs	T1, T2
54	14		Binary Multiplier, Magnitude Comparator		Chalk and Talk, PPTs	T1, T2
55 56		DecodersAnalyzethedesignofEncodersdecoders,encodersand		Chalk and Talk, PPTs	T1, T2	
57			Multiplexers Bridge Class	multiplexers.	,	
59	16		<u>Unit-V</u> :Sequential Circuits	Understand the design and analysis of sequential logic circuits.	Chalk and Talk, PPTs	T1, T2
60			Storage Elements: Latches and flip flops	Understand construction of latches and flip flops.	Chalk and Talk, PPTs	T1, T2
61		5	Analysis of Clocked Sequential Circuits, State Reduction and Assignment	Analysetheclockedsequentialcircuitsandperformstatereductionandassignments.	Chalk and Talk, PPTs	T1, T2
62	17			Shift Registers Understand the design and analysis of shift registers.	Chalk and Talk, PPTs	T1, T2
63			Bridge Class			
64			Ripple Counters, Synchronous Counters	Understand the design and analysis of various counters.	Chalk and Talk, PPTs	T1, T2
65	18		Random-Access Memory, Read-Only Memory	Understand the concept of memory.	Chalk and Talk, PPTs	T1, T2
65			Revision	Revise above topics.	PPTs	T1, T2
			II Mid Examinations (V	Veek 18)		

IX.MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES



													25	IN THE INVERSE REPORTED IN	2
Course	Course Program Outcomes									Pr	ogram	Specific			
Outcomes														Outco	mes
	РО	PO	PO	PO	DO5	РО	D 07	PO	DOG	PO	PO	PO	PS	PS	DCO1
	1	2	3	4	P05	6	P07	8	P09	10	11	12	01	02	PS03
CO1	3	2	3	-	-	-	-	-	1	-	-	2	2	1	-
CO2	3	2	2	-	-	-	-	-	-	-	-	2	2	-	-
CO3	3	2	3	-	-	-	-	-	-	2	3	-	-	-	-
CO4	3	2	2	-	-	-	-	-	-	2	1	-	2	-	-
CO5	3	2	3	-	-	-	-	-	1	-	3	-	-	1	-
CO6	3	2	2	-	-	-	-	-	-	-	3	2	-	-	-
Average	3	2	2.5	-	-	-	-	-	1	2	2.5	2	2	1	-
Average (Rounded)	3	2	3	-	-	-	-	-	1	2	3	2	2	1	-

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None X IUSTIFICATIONS FOR CO-PO MAPPING:

Mapping	Low (1), Medium (2),	Justification	
	High(3)		
CO1-PO1	3	Students will be able to Students will be able to understand open circuited P-N junction.	
CO1-PO2	2	Students will be able to understand how the diode acts as	
01-102	2	rectifier and study the characteristics of rectifiers.	
CO1 PO3	3	Students will be able to understand the V-I characteristics of	
01-105	5	P-N junction.	
	1	Students will be able to understand the temperature effects and	
diode resistance		diode resistance	
CO1-PO12	2	Know about drift and diffusion capacitances.	
CO1-PSO1	2	Students will be able to understand diode switching times.	
		Students will be able to understand the concept of breakdown	
CO1-PSO2	2 2	in diodes and study the operation and characteristics of Zener	
		diode.	
CO2 PO1	3	Students will be able to understand the operation,	
C02-F01	5	characteristics and applications of tunnel diode	
	2	Students will be able to understand the operation,	
CO2-FO2	2	characteristics and applications of photo diode and LED.	
CO2-PO3	2	To explain clipping circuits and comparators.	
CO2 PO12	2	Students will be able to understand how the diode acts as	
C02-P012	2	rectifier and study the characteristics of rectifiers.	
CO2 DSO1	2	Students will be able to understand the general conditions for	
C02-F501	2	filters and study the rectifier with capacitor filter.	



CO3-PO1	3	To study the operation of transistor as an amplifier.
CO3-PO2	2	To study the characteristics of CB,CE,CC configurations.
CO3-PO3	3	Compare various configurations of transistors.
CO2 DO10	a a	Understand the concept of operating point and purpose of
C03-P010	2	biasing.
CO3-PO11	3	Study about bias compensation, thermal runaway and stability.
CO4-PO1	3	Explain the operation of transistor at low frequencies.
CO4 DO2	2	Explain the operation of CE amplifier, study its frequency
CO4-PO2	2	response and gain bandwidth product.
CO4-PO3	2	Understand the operation of emitter follower.
CO4 DO10	2	Explain the operation of RC coupled two cascaded CE and
C04-P010	2	multistage CE amplifiers.
CO4 DO11	1	Students will be able to understand the operation, V-I
C04-P011	1	characteristics of JFET.
	2	Students will be able to understand the operation, V-I
C04-PS01	2	characteristics of MOSFFET.
CO5 DO1	2	Students will be able to understand the operation of low
C05-P01	3	frequency CS and CD amplifiers.
CO5 DO2	2	Students will be able to understand the arithmetic operations
C03-P02	2	carried by digital systems.
CO5 DO2	2	Students will be able to understand the OR, AND, NOT, EX-
C03-P03	5	OR, NAND and NOR DTL gates and modified DTL gates.
CO5 DO0	1	Students will be able to understand the design and analysis of
05-109	9 1	combinational logic circuits.
CO5 PO11	3	Students will be able to analyze the design of decoders,
005-F011	5	encoders and multiplexers.
CO5-PSO2	1	Students will be able to understand the EX-OR function.
CO6-PO1	3	To design functions using universal gates.
COG PO2	2	Students will be able to understand the design and analysis of
000-102	2	sequential logic circuits.
CO6-PO3	2	Students will be able to understand construction of latches and
		flip flops.
CO6-PO11	3	Analyse the clocked sequential circuits and perform state
	5	reduction and assignments.
CO6-PO12	2	Students will be able to understand the concept of memory.

XI.QUESTION BANK (JNTUH) : UNIT - I



S.No.	Question	Blooms	Course
		Taxonomy	Outcom
		Level	е
1.	Explain the formation of PN junction diode.	Remember	1
2.	Discuss the operation of PN junction diode as rectifier.	Understand	1
3	Define biasing. Briefly describe the operation of PN	Understand	1
5.	diode under forward and reverse bias conditions.	Understand	1
	Sketch the V-I characteristics of p-n junction diode for		
1	forward bias voltages. Distinguish between the	Evaluation	1
4.	incremental resistance and the apparent resistance of the	Evaluation	1
	diode?		
5	Explain the temperature dependence of VI characteristics	Comprehensi	1
5.	of PN diode?	on	1
6	Derive an expression for total diode current starting from	Knowledge	1
0.	Boltzmann relationship in terms of the applied voltage?		I
	Explain the V-I characteristics of Zener diode and	Understand	
7.	distinguish		1
	between Avalanche and Zener Break downs?		
8	Explain the concept of diode capacitance. Derive	Understand	1
0.	expression for transition capacitance?		-
	Define depletion region at p-n junction? What is the		
9.	effect of	Remember	1
	forward and reverse biasing of p-n junction on the		-
	depletion region? Explain with necessary diagrams?		
	Explain the tunneling phenomenon. Explain the	Understand	
10.	characteristics of tunnel diode with the help of necessary		1
	energy band diagrams?		
	What is the photo diode? Explain its principle of	Remember	
11.	operation and		1
	applications in detail?		
12.	Explain the construction and working of LED?	Understand	1
13.	Discuss the applications of diode as clipper circuits.	Remember	1
14.	Briefly explain the operation of a comparator.	Remember	1
15	Draw the block diagram of a regulated power supply and	Understand	1
15.	explain its operation?		1
16	Draw the circuit of a half-wave-rectifier and find out the	Analyze	1
10.	ripplefactor, % regulation? Efficiency and PIV?		1



		2000	3
17	Draw the circuit of bridge rectifier and explain its	Analyze	1
17.	operation with the help of input and output waveforms?		1
	With suitable diagrams, explain the working of centre-	Understand	
18.	tapped full wave rectifier. Derive expressions for V _{DC} ,		1
	I_{DC} , V_{rms} and I_{rms} for it?		
10	Explain the relative merits and demerits of all the	Understand	1
19.	rectifiers?		1
20	Mention the need for filter circuits in rectifiers. Explain	Understand	1
20.	the working of capacitor filter.	Understand	1

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define Electronics?	Remember	1
2.	Explain about forward bias of diode?	Understand	1
3.	Explain about reverse bias of diode?	Understand	1
4.	Write the applications of diode?	Comprehensio n	1
5.	Draw the V-I characteristics of diode?	Comprehensio n	1
6.	List the differences between ideal diode and practical diode?	Remember	1
7.	Define diffusion capacitance?	Knowledge	1
8.	Define transition capacitance?	Remember	1
9.	Define static resistance?	Remember	1
10.	Define dynamic resistance	Remember	1
11.	Write the equation of diode current	Remember	1
12.	Define cut-in voltage?	Remember	1
13.	Write the differences between avalanche and zener breakdown mechanisms?	Knowledge	1
14.	Define zener breakdown mechanism?	Remember	1
15.	Define depletion region?	Remember	1
16.	Explain the temperature dependence of VI characteristics of PN diode?	Understand	1



		2000	25
17.	Define doping?	Remember	1
18.	Explain about extrinsic semiconductor	Understand	1
19.	Explain about unbiased PN junction?	Understand	1
20.	Write down the expression for diode current?	Knowledge	1
21.	Define drift current?	Remember	1
22.	List the applications of Zener diode?	Analyze	1
23.	Define forbidden energy gap?	Remember	1
24.	With appropriate circuit diagram explain the DC load line analysis of semiconductor diode?	Analyze	1
25.	Define Peak Inverse voltage of a diode?	Remember	1
26.	What is the principle of operation of photodiode?	Knowledge	1
27.	Give the principle of operation of Light Emitting Diode?	Analyze	1
28.	Define diffusion current?	Remember	1
29.	List the applications of LED.	Analyze	1
30.	Define photodiode?	Remember	1

UNIT – II

S.No.	Question	Blooms	Course
		Taxonomy	Outcome
		Level	
1.	With a neat diagram explain the various current components in an NPN bipolar junction transistor & hence derive general equation for collector current, I_C ?	Understand	2
2.	Define Early-effect; explain why it is called as base- width modulation? Discuss its consequences in transistors in detail?	Remember	2
3.	How transistor acts as an amplifier?	Remember	2
4.	Draw the input and output characteristics of a transistor in common emitter configurations?	Comprehensio n	2
5.	Draw the input and output characteristics of a transistor in common base configurations?	Evaluate	2
6.	Draw the input and output characteristic of a transistor in common	Comprehensio n	2



		7999	25
	collector configurations?		
7.	Explain the constructional details of Bipolar Junction Transistor?	Understand	2
8.	Derive the relation among α , β and γ ?	Evaluation	2
9.	What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors?	Remember	2
10.	Analyze general transistor amplifier circuit using h parameter model. Derive the expressions for A_I , A_V , R_i , R_o , A_{Is} , A_{Vs} .	Analyze	2
11.	Draw the circuit of an emitter follower, and derive the expressions for A_I , A_V , R_i , R_o in terms of CE parameters.	Remember	2
12.	Write the analysis of a CE amplifier circuit using h parameters. Derive the expressions for A_I , A_V , R_i , R_o , A_{Is} , A_{Vs} .	Analyze	2
13.	Define h-parameter of a transistor in a small signal amplifier. What are the benefits of h-parameters?	Remember	2
14.	Compare the different types of coupling methods used in multistage amplifiers.	Remember	2
15.	Sketch two RC-coupled CE transistor stages. Show the middle and low frequency model for one stage. Write the expressions for current gains.	Remember	2
16.	Explain about different methods of Inter stage coupling in amplifiers. When two stages of identical amplifiers are cascaded, obtain the expressions for overall voltage gain, current gain and power gain.	Understand	2

Short Answer Questions:

S.No.	Question	Blooms Taxonomy	Course
		Level	Outcome
1.	What is meant by operating point Q?	Comprehension	2
2.	Draw the symbols of NPN and PNP transistor?	Comprehension	2
3.	Explain the operation of BJT and its types?	Understand	2
4.	Explain the breakdown in transistor?	Understand	2
5.	Explain the transistor switching times?	Understand	2
6.	Define Transistor current?	Remember	2
7.	Define early effect or base width modulation?	Remember	2
8.	Explain about transistor amplifier?	Understand	2



		25	24
9.	Define current amplification factor?	Remember	2
10.	When does a transistor act as a switch?	Comprehension	2
11.	Explain about the various regions in a transistor?	Understand	2
12.	Draw the small signal model of a CE configuration?	Knowledge	2
13.	Draw the output characteristics of NPN transistor in CEconfiguration?	Comprehension	2
14.	Define hie and hfe in CE configuration?	Remember	2
15.	Define hoe and hre in CB configuration?	Remember	2
16.	Define saturation region?	Remember	2
17.	Write the relation between IC, β , IB and ICBO in a BJT?	Knowledge	2
18.	Define cutoff region?	Remember	2
19.	Define active region?	Remember	2
20.	Describes the various current components in a BJT?	Knowledge	2
21.	Define amplifier?	Remember	2
22.	Draw the hybrid model of a CB configuration?	Knowledge	2
23.	List the classification of amplifiers.	Remember	2
24.	List the classification of amplifiers based on frequency of operation	Remember	2
25.	Define various hybrid parameters.	Remember	2
26.	Draw the hybrid equivalent model of CE Amplifier	Understand	2
27.	In a multistage amplifier, what is the coupling method required to amplify dc signals?	Remember	2
28.	Write the expression for lower $3 - dB$ frequency of an n – stage amplifier with non – interacting stages.	Remember	2
29.	Two stages of amplifier are connected in cascade. If the first stage has a decibel gain of 40 and second stage has an absolute gain of 20 then what is the overall gain in decibels.	Evaluate	2
30.	Why the overall gain of multistage amplifier is less than the product of gains of individual stages.	Understand	2
31.	What are the main characteristics of a Darlington amplifier?	Understand	2
32.	Why direct coupling is not suitable for amplification of high frequency	Understand	2



UNIT - III

S.No.	Question	Blooms Taxonomy	Course
		Level	Outcome
1.	Explain the operation of FET with its characteristics and explain the different regions in transfer characteristics?	Comprehension	3
2.	Define pinch-off voltage and trans conductance in field effect transistors?	Comprehension	3
3.	With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on thecharacteristics?	Application	3
4.	Explain how a FET can be made to act as a switch?	Knowledge	3
5.	Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers?	Knowledge	3
6.	Create a relation between the three JFET parameters, μ , r d and gm?	Creating	3
7.	How a FET can be used as a voltage variable Resistance (VVR)?	Remember	3
8.	Explain the construction & operation of a P- channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?	Understand	3
9.	Sketch the drain characteristics of MOSFET for different values of VGS& mark different regions of operation.	Comprehension	3
10.	Explain the principle of CS amplifier with the help of circuit diagram. Derive the expressions for AV, input impedance and output Impedance?	Understand	3
11.	Write the expressions for mid-frequency gain of a FET Common Source?	Knowledge	3
12.	Discuss the high frequency response of CD Configuration?	Knowledge	3
13.	What is the effect of external source resistance on the voltage gain of a common source amplifier? Explain with necessary derivations?	Remember	3
14.	Draw the small-signal model of common drain FET amplifier. Derive expressions for voltage gain and output resistance?	Analyze	3
15.	 a) Solve the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: i.100 – 110000 ii. 11010 - 1101. b) Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code .Write short notes 	Apply	4

	on binary number systems.	E Contractor	
16.	 a) Solve arithmetic operation indicated below. Follow signed bit notation: i. 001110 + 110010 ii. 101011 - 100110. b) Explain the importance of gray code? 	Apply	4
17.	Solve (3250 - 72532)10using 10's complement?	Apply	4
18.	As part of an aircraft's functional monitoring system, a circuit is when the \gear down" switch has been activated in preparation for landing. Red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Design a circuit to meet this requirement? required to indicate the status of the landing gears prior to landing. Green LED display turns on if all three gears are properly extended	Understand	4
19.	Solve (a) Divide 01100100 by 00011001 (b) Given that (292)10 =(1204)b determine `b'	Apply	4
20.	Solve (a) What is the gray code equivalent of the Hex Number 3A7 (b) Find the biquinary number code for the decimal numbers from 0 to 9 (c) Find 9's complement (25.639)10	Apply	4
21.	Solve (a) Find (72532 - 03250) using 9's complement. (b) Show the weights of three different 4 bit self complementing codes whose only negative weight is - 4 and write down number system from 0 to 9.	Apply	4

Short Answer Questions:

S.No.	Question	Blooms Taxonomy	Course
		Level	Outcome
1.	Write the expressions for mid-frequency gain of a FET Common Source?	Knowledge	3
2.	Discuss the high frequency response of CD Configuration?	Knowledge	3
3.	What is the effect of external source resistance on the voltage gain of a common source amplifier? Explain with necessary derivations?	Remember	3
4.	Draw the small-signal model of common drain	Analyze	3

		and the second sec	
	FET amplifier. Derive expressions for voltage gain and output resistance?		
5.	Draw the small-signal model of common source FET amplifier.	Analyze	3
6.	Why FET is called a voltage operated device?	Evaluation	3
7.	List the important features of FET?	Knowledge	3
8.	Write short notes on millers theorem?	Knowledge	3
9.	Give the classifications of FETs and their application areas?	Knowledge	3
10.	Define pinch off voltage?	Comprehension	3
1.	Draw the structure of an n-channel JFET?	Knowledge	3
12.	Define rd and Gm?	Remember	3
13.	Draw the static characteristics curves of an n- channel JFET?	Comprehension	3
14.	Draw the drain characteristics of depletion type MOFET?	Knowledge	3
15.	Draw the small signal model of JFET?	Knowledge	3
16.	Draw the transfer characteristics for P-channel JFET?	Comprehension	3
17.	Draw the Drain V-I characteristics for p-channel JFET?	Knowledge	3
18.	Explain about ohmic and saturation regions?	Understand	3
9.	Draw the drain characteristics of an n-channel enhancement type MOSFET?	Knowledge	3
20.	Write short notes on binary number systems?	Understand	4
21.	Discuss 1's and 2's complement methods of subtraction?	Understand	4
22	Discuss octal number system?	Understand	4
23.	State and prove transposition theorem?	Knowledge	4
24.	Explain how do you convert AOI logic to NAND logic?	Understand	4
25.	Write a short note on five bit BCD codes?	Understand	4

UNIT - IV

S.No.	Question	Blooms Taxonomy	Course
		Level	Outcome
	A combinational circuit has 4 inputs(A,B,C,D)		
1.	and three outputs(X,Y,Z)XYZ represents a binary	Knowledge	6
	number whose value equals the number of 1's at		

	the input state the minterm expansion for the		
	X, Y, Z ii. state the maxterm expansion for the Y		
	and Z		
	A combinational circuit has four inputs		
	(A,B,C,D), which represent a binarycoded-		
	decimal digit. The circuit has two groups of four		
2.	outputs -S,T,U,V(MSB digit) and W,X,Y,Z.(LSB	Apply	6
	digit)Each group represents a BCD digit. The		-
	output digits represent a decimal number which is		
	five times the input number. Illustrate the		
	minimum expression for all the outputs?		
	Summarize the following Boolean expressions		
	using K-map and implement them using NOR		
3.	gates: (a) $F(A, B, C, D) = AB'C' + AC + A'CD'$	Understand	6
	(b) $F(W, X, Y, Z) = W'X'Y'Z' + WXY'Z' +$		
	W'X'YZ + WXYZ.		
1	Design BCD to Gray code converter and realize	Understand	6
4.	using logic gates?	Understand	0
5.	Design EX-OR using NAND gates?	Understand	6
6	compile the following expression using Karnaugh	Understand	6
0.	map (B'A + A'B + AB')	Understand	0
	Design a circuit with three inputs(A,B,C) and two		
7.	outputs(X,Y) where the outputs are the binary	Understand	6
	count of the number of "ON" (HIGH) inputs?		
0	Implement the INVERTER gate, OR gate and	TT 1 / 1	6
8.	AND gate using	Understand	6
9.	NAND gate, NOR gate?		6
	Design a circuit with four inputs and one output		
10.	where the output is 1 if the input is divisible by 3	Understand	6
	or 7?		
1.1	Implement the Boolean function $F = AB + CD + CD$	TT 1 . 1	(
11.	E	Understand	6
	Implement the Boolean function $F = AB + CD + CD$		
12.	E using NAND gates only?	Understand	6
12	Summarize the Boolean function $F(w, x, y, z) =$		
13.	$\Sigma(1, 3, 7, 11, 15) + d(w, x, y, z) = \Sigma(0, 2, 5)$	Understand	6
	Construct the logic diagram of a full subtractor		
14.	using only 2-input NAND gates?	Apply	5
15	Construct the logic diagram of a full subtractor	Apply	5
15.		Аррту	5



		2000	24
	using only 2-input NAND gates?		
16.	Use a multiplexer having three data select inputs to solve the logic for the function $F = \Sigma$ (0, 1, 2, 3, 4, 10, 11, 14, 15)	Apply	5
17.	Identify all the prime implicants and essential prime implicants of the following functions Using karnaugh map. $F(A,B,C,D) =$ $\Sigma(0,1,2,5,6,7,8,9,10,13,14,15).$	Knowledge	5
18.	Design a combinational circuit that generates the 9's complement of BCD digit?	Understand	5
19.	Design a combinational circuit to find the 2's complement of given binary number and realize using NAND gates?	Understand	5
20.	Design a logic circuit to convert gray code to binary code?	Understand	5
21.	Design circuit to detect invalid BCD number and implement using NAND gate only?	Understand	5
22.	Explain the design procedure for code converter with the help of example?	Understand	5
23.	Construct half subtractor using NAND gates?	Apply	5
24.	Design an 8-bit adder using two 74283?	Understand	5
25.	Explain the working of carry look-ahead generator?	Understand	5
26.	Explain carry propagation in parallel adder with neat diagram?	Understand	5
27.	Explain the circuit diagram of full subtractor and full adder?	Understand	5
28.	Construct and explain the working of decimal adder?	Apply	5

Short Answer Questions:

S.No.	Question	Blooms	Course
		Taxonomy	Outcome
		Level	
1.	Define K-map? Name its advantages and disadvantages?	Knowledge	6
2.	Write the block diagram of 2-4 and 3-8 decoders?	Understand	6
3.	Define magnitude comparator?	Knowledge	6
4.	Describe what do you mean by look-ahead carry?	Understand	6



		25	ES.
5.	Summarize the Boolean function $x'yz + x'yz' + xy'z' + xy'z + xy'z + xy'z' + xy'z + xy'z + xy'z' + xy$	Understand	6
6.	Explain how combinatorial circuits differ from sequential circuits?	Understand	6
7.	Explain what are the IC components used to design combinatorial circuits with MSI and LSI?	Understand	6
8.	Design the two graphic symbols for NAND gate?	Understand	6
9.	Design the two graphic symbols for NOR gate?	Understand	6
10.	Summarize the Boolean function x'yz + x'yz' + xy'z' + xy'z without using K- map?	Understand	6
11.	Explain the properties of EX-OR gate?	Understand	6
12.	Solve the function of fig with AND-OR INVRET implementations? $A^{\text{BC} \ 00} 01 11 10$ $0 1 0 0 0$ $1 0 0 1$	Apply	6
13.	Solve the following using NAND gates? a) (A+B)(C+D) b) A.B+CD(ABI+CD)	Apply	6
14.	Sketch the following equation using k-map and realize it using NAND gate? $Y=\sum m(4,5,8,9,11,12,13,15)$	Apply	6
15.	Solve Y=ABI+CD+(AIB+CIDI) using NAND gate?	Apply	6
16.	State that AND-OR network is equivalent to NAND- NAND network?	Knowledge	6
17.	Show both NAND and NOR gates are called Universal gates?	Apply	6
18.	Sketch the following logic function using k-map and implement it using logic gates? $Y(A,B,C,D) = \sum m(0,1,2,3,4,7,8,9,10,11,12,14)$	Apply	6
19.	Summarize the rules and limitations of K-map simplification?	Understand	6
20.	Analyze the steps for simplification of POS expression?	Apply	6

UNIT - V

S.No.	Question	Blooms	Course
		Taxonomy	Outcome
		Level	
1	Explain the design of Sequential circuit with an example.	Understand	5
1.	Show the state reduction, state assignment?	Understand	5

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2.	Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers?	Understand	5
3.	Design a 4-bit BCD Ripple Counter by using T-FF?	Understand	5
4.	Define BCD Down Counter and Draw its State table for BCD Counter?	Knowledge	5
5.	Explain the state reduction and state assignment in designing sequential circuit. Consider one example in the above process?	Understand	5
6.	Design a sequential circuit with two D flip-ops A and B. and one input x. when x=0,the state of the circuit remains the same. When x=1,the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00.and repeats?	Understand	5
7.	Design a Modulo-12 up Synchronous counter Using T- Flip Flops and draw the Circuit diagram?	Understand	5
8.	Explain the Ripple counter design. Also the decade counter design?	Understand	5
9.	Design a 3 bit ring counter? Discuss how ring counters differ from twisted ring counter?	Understand	5
10.	Design a left shift and right shift for the following data 10110101?	Understand	5
11.	Design Johnson counter and state its advantages and disadvantages?	Understand	5
12.	Explain with the help of a block diagram, the basic components of a Sequential Circuit?	Understand	5
13.	Explain about RS and JK flip-flops?	Understand	5
14.	Define T–Flip-flop with the help of a logic diagram and characteristic table?	Knowledge	5
15.	Define Latch. Explain about Different types of Latches in detail?	Knowledge	5
16.	Explain in detail about RAM and types of RAM?	Understand	5
17.	Illustrate the features of a ROM cell?	Apply	5
18.	Explain in detail about ROM and types of ROM?	Understand	5
19.	Explain coincident memory decoding?	Understand	5
20.	Describe what is meant by memory expansion? Mention its limits?	Understand	5

Short Answer Questions:



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S.No.	Question	Blooms	Course
		Taxonomy	Outcome
		Level	
1.	Differentiate combinational and sequential logic circuits?	Apply	5
2.	Explain basic difference between a shift register and counter?	Understand	5
3.	Illustrate applications of shift registers?	Apply	5
4.	Define bidirectional shift register?	Knowledge	5
5.	Describe dynamic shift register?	Knowledge	5
6.	Convert a JK Flip Flop to T	Understand	5
7.	Classify the basic types of counters?	Understand	5
8.	Differentiate the advantages and disadvantages of ripple counters?	Apply	5
9.	Convert a JK Flip Flop to SR	Understand	5
10.	Explain what is a variable modulus counter?	Understand	5
11.	Design and explain gated latch logic diagram?	Understand	5
12.	Define race around condition? How it can be avoided?	Knowledge	5
13.	Convert a JK Flip Flop to D	Understand	5
14.	Convert a SR Flip-Flop to JK	Understand	5
15.	List the types of RAM.	Knowledge	5
16.	State the features of a ROM cell?	Understand	5

OBJECTIVE QUESTIONS:

UNIT-I

1.	The conventional current in a P	N junction die	ode flows:	[]
	(a) From positive to negative		(b) From negative to positive		
	(c) In the direction opposite to t	he electron flo	ow. (d) Both (a) and (c) above		
2.	The cut in voltage (or knee vol	tage) of a silic	con diode is	[]
	(a) 0.2V (b) 0.6V	(c) 0.8 V	(d) 1.0V		
3.	When a diode is reverse biased,	it is equivale	nt to	[]
	(a) An OFF switch	(b) an ON sy	witch		
	(c) A high resistance	(d) none of t	he above		
4.	The resistance of a diode is equ	al to		[]
	(a) Ohmic resistance of the P- a	nd N- semico	nductors (b) Junction resistance		
	(c) Reverse resistance	(d) A	Algebraic sum of (a) and (b) above		
5.	For a silicon diode, the value of	the forward -	bias voltage typically	[]
	(a) Must be greater than 0.3	SV	(b) Must be greater that	an 0.7V	
	(c) Depends on the width of the	depletion reg	ion		
	(d) Depends on the concentration	on of majority	carriers		

	6	When forward biased a diada		1	1
	0.	(a) Blocks current	(b) conducts current	L]
		(a) Has a high registered	(d) drome e large veltage		
	7	(c) Has a high resistance	(d) drops a large voltage.	г	1
	7.	(a) The applied voltage	(b) the temperature	l]
		(c) The current	(d) the thermal voltage		
	8.	The forward region of a se	emiconductor diode characteristic curve	is where of	liode appears as
		(a) Constant current source	(b) a capacitor	L	-
		(c) An OFF switch	(d) an ON switch		
	9.	At room temperature of 25 °C, t (a) 0.5V (b) 0.3V	he barrier potential for silicon is 0.7 V. lts v (c) 0.9V (d) 0.7V	alue at 125°	C is[]
	10.	Junction breakdown of a PN ju	nction occurs	[]
		(a) With forward bias	(b) with reverse bias		
		(c) Because of manufacturing de	efect (d) None of these		
	11.	Reverse saturation current in a s	ilicon PN junction diode nearly doubles for	every	
		(a) 2° C rise in temperature	(b) 5° C rise in temperature	L	
		(c) 6° C rise in temperature	(d) 10° C rise in temperature		
	12.	The transition capacitance of	a diode is 1nF and it can withstand a 1	reverse pote	ntial of 400V. A
	12.	capacitance of 2nF which can w	ithstand a reverse potential of 1 kV is obtai	ned by conne	ecting
		(a) two 1nF diodes in series(b) six parallel branches with	s th each branches comprising there 1nF diod	les in series	
		(c) two 1nF diodes in series	S		
	12	(d) three parallel branches	with each branch comprising InF diodes in	series	1
	13.	A zener diode		L]
		(a) has a sharp breakdown	age rating		
		(c) is useful as an amplifier			
		(d) has a negative resistance	e		
	14.	A tunnel- diode is	~	ſ	1
	(2	a) a very heavily-doped PN junc	tion diode	L	L
	(ł	b) a high resistivity PN junction	diode		
	(c) a slow switching device			
	(d) used with reverse bias			
	15.	The light-emitting diode (LED)		[]
	(8	a) is usually made from silicon			
	(1	b) uses a reverse-biased junction			
	((c) gives a light output which inc	reases with the increase in temperature		
16	((1 E	1) depends on the recombination D^2	of holes and electrons	г	1
10.	LE	D s do not require	(b) warm up time	l]
	(a)	Both (a) and (b) above	(d) non of above		
17	The	\mathbf{D} sensitivity of a photodiode dependence	ends upon	Г	1
. / .	()	a) light intensity and depletion	region width	L	Ţ
	(1	b) depletion region width and	excess carrier life time		
	(c) Excess carrier life time and	forward bias current.		
	(d) Forward bias current and lig	ght intensity.		

)
18. LEDs are commonly fabricated from gallium compounds like gallium a because they	arsenide and []	≷ gallium phosphid
(a) Are cheap (b) are easily available		
(c) Emit more heat (d) emit more light.		
19. A LED is basically a P-N junction.	[]
(a) forward-biased (b) reverse-biased		
(c) lightly-doped (d) heavily-doped		
20. As compared to a LED display, the distinct advantage of an LCD display is t	that it requires	8
	r î	
(a) No illumination (b) extremely-bias		
(c) No forward-bias (d) a solid crystal		
21. Before illuminating a P-N junction photodiode, it has to be	ſ	1
(a) Reverse-biased (b) forward-biased	L	1
(c) Switched ON (d) switched OFF		
22 A LED emits visible light when its	г	1
(a) P-N junction is reverse-biased (b) depletion region widens	L	1
(a) Heles and electrons recombine (d) B N junction becomes hot		
(c) Holes and electrons recombine (d) F-N junction becomes not.	г	1
25. In LED, fight is enflued because	L	J
(a) Recombination of charge carriers takes place		
(b) Diode gets heated up		
(c) Light failing on the diode gets amplified		
(d) Light gets reflected due to lens action.	-	
24. GaAs, LEDs emit radiation in the	l]
(a) Ultraviolet region (b) violet - blue green range of the visible region		
(c) Visible region (d) infra-red region		
IINIT_II		
1 The "out in" voltage of a giligen small signal transistor is	r	1
1. The cut-fit voltage of a sincon small-signal transistor is (a) OV (b) O V (c) O SV (d) O SV	L]
(a) 0° (b) 0.2° (c) 0.5° (d) 0.8°		· · · · · · · · · · · · · · · · · · ·
2. When the collector junction in transistors is blased in the reverse directio	n and the em	litter junction in th
forward direction, the transistor is said to be in the		
(a) Active region (b) cut-off region		
(c) Saturation region (d) none of them.		
3. The transistor is said to be in saturation region when	[]
a. both collector and emitter junctions are forward biased		
b. both collector and emitter junctions are reversed biased ·		
c. emitter junction is forward biased, but the collector junction is reverse biase	ed (
d. emitter junction is reverse biased, but the collector junction is forward biase	d	
4. For a silicon transistor in the common emitter configuration the cut-off of	condition is a	chieved by applyin
a minimum reverse voltage across the emitter junction of the order of		
[]		
(a) 0V (b) 0.7 V (c) 1.5V (d) 5V		
5. A transistor connected in common base configuration has]	1
(a) a high input resistance and a low output resistance	L	1
(b) a low input resistance and high output resistance		
(c) a low input resistance and a low output resistance		
(d) a high input resistance and a high output resistance		
6 Which of the following is not a time varying quantity?	Г	1
(a) V_{ac} (b) V_{ac} (c) V_{ac} (d) V_{ac}	L	1
7 In the Ebbers-Model of a bipolar transistor, the parameter is the	г	1
7. In the Eucles-Would of a Dipolar transition, the parameter is the	L]
a. Forward transmission from emitter to collector		

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b. Reverse transmission from collector to emitter c. Common base current gain d. Both (a) and (c) above 8. The value of trans-conductance of a bipolar transistor for a collector current of 1.5 mA is (a) 0.05Ω (b) 0.05 x 10 ³ Ω(c) 37.5 Ω (d) None of the above 9. The resistance T_{00} in the low frequency hybrid- π model of a bipolar transistor represents 1. Base spreading resistance b. A.C. resistance for forward biased emitter-base junction c. The effect of feedback between the emitter-base junction and collector-base junction due to Early effect 10. The capacitance C_0 in the high frequency hybrid- π model of a bipolar transistor represents the [] (a) Depletion region capacitance (b) Emitter diffusion capacitance (c) Emitter-base junction capacitance (b) Sum of the (b) and (c) above 11. For a common emitter amplifier having a small un bypassed emitter resistance (R_0) the input resistance is approximately equal to (a) R_{e} (b) h_{e} (c) $h_{e} R_{e}$ (d) R_{e} / h_{e} . 12. The voltage gain of a common base amplifier is (a) zero (b) less than unity (c) unity (d) greater than unity 13. For a common base transistor amplifier having input resistance (R_1) and output resistance (R_0), which of the following statements holds good []] (a) R_{e} is low, R_{e} is high (b) R_{e} is low (c) R_{e} and R_{e} are both medium (d) None of these 14. The current gain of an emitter follower is (a) common-base (b) common-collector (c) common-base (b) common-collector (c) common-collector (c) common-base (c) common-collector (c) common-base (d) analler the current gain. (d) smaller the circuit voltage gain. 17. The main use of an emitter follower is as (a) power amplifier, larger the internal resistance of the as signal source (c) common-base (c) common-base (d) context the input impedance (e) now-input impedance incurit (d) follower of base signal. 18. An ideal amplifer is one which (a) has antifier to output od a resistance of signal source is increased (c) mit			
b. Reverse transmission from collector to emitter c. Common base current gain d. Both (a) and (c) above 8. The value of trans-conductance of a bipolar transistor for a collector current of 1.5 mA is [] (a) 0.05Ω (b) $0.05 \times 10^3 \Omega(c) 37.5 \Omega$ (d) None of the above 9. The resistance r_{sw} in the low frequency hybrid- π model of a bipolar transistor represents [] a. Base spreading resistance b. A.C. resistance of forward biased emitter-base junction c. The effect of feedback between the emitter-base junction and collector-base junction due to Early effect d. None of the above 10. The capacitance C _s in the high frequency hybrid- π model of a bipolar transistor represents the [] (a) Depletion region capacitance (b) Emitter diffusion capacitance (c) Emitter-base junction capacitance (c) Emitter-base gain of a common base amplifier is 12. The voltage gain of a common base amplifier is (a) zero (b) less than unity (c) less than unity (d) greater than unity (e) R ₁ and R ₀ are both medium 15. Mich of the following transistor amplifiers has the highest voltage gain? 16. In an a camplifier, larger the internal resistance of the as signal source (c) convinent than outer follower is as (a) zero (b) creater the overall voltage gain (b) greater the input impedance (c) Banal et the current gain 1			>
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22. The h-parameters are called hybrid parameters because they [] (a) are different from y- and z - parameters. [] (b) are mixed with other parameters. [] (c) apply to circuits contained in a box [] (d) are defined by using both open-circuit and short-circuit terminations 23. Which of the following statement is not correct regarding the h-parameters of a transistor (a) The values of h-parameters can be obtained from transistor characteristics. (b) their values depend on operating point (d) they are four in number 24. Which of the following four h-parameters of a transistor has a greatest value [] (a) h. (b) h. (c) hn (d) hr 27. The typical value he is is [] (a) h. (b) h. (c) hn (d) hr 28. The h-parameters of a transistor depend on its [] (a) 0 (b) $\frac{1}{\sqrt{p}}$ (c) Temperature (d) all of the above 29. The output admittance h ₀ of an ideal transistor connected is common-base configuration (c) $\frac{1}{p_{R_{R_{R_{R}}}}}$ (d) 10 mA (d) 0.5 mA (e) 10 mA (f) 0.5 mA (g) 10 mA (h) 0.5 mA			
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(d) Both (a) and (c) above	(c) N-channel devices have higher packing density than D-channel devices		
	(d) Both (a) and (c) above		

 6. As compared to N-channel MOS switch, the P-channel MOS switch has [(a) Same ON resistance (b) Less ON resistance]
 (a) More ON resistance (d) either (a) or (b) 7. Thermal runway is not possible in FET because as the temperature of the FET increases[(a) the mobility decreases (b) the trans-conductance increases (c) the drain current increases (d) either (a) or (b)]
8. (1217)8 is equivalent to []
(A) (1217)16 (B) (028F)16 (C) (2297)10 (D) (0B17)16	
9. The smallest integer than can be represented by an 8-bit number in 2's complement form is []
(A) 256 (B) -128 (C) -127 (D) 0	
10. P is a 16-bit signed integer. The 2's complement representation of P is (F87B)16. The 2	2's comple
representation of 8*P is []	
(A) C3D8 (B) 187B (C) F878 (D) 987B.	
11. Convert (101101.1101) binary number to decimal number []
a). 45.8125 b) 44.8125 c) 45.8215 d) 44.8215	
12. Express the number 107 into 1's compliment form. []
a).10010100 b)10010101 c) 10000100 b)10000101	
13. BCD addition for decimal number 113 & 101 is []
a) 214 b) 241 c)142 d)124	
14. convert 101011 to gray code number []
a). 111110 b) 110110 c)101110 d)111011.	
15. What is the minimum number of gates required to implement the Boolean	
function (AB+C) if we have to use only 2-input NOR gates? [$(A) = 2 (B) = 2 (C) = 4 (D) = 5$]
(A) 2 (B) 3 (C) 4 (D) 5 16. convert 011001 to gray code number [1
a). 111110 b) 110110 c)101110 d)NONE	-
17. BCD addition for decimal number 143 & 167 is .	1
a) 214 b) 241 c)142 d)NONE	-
18. Any negative number is recognized by its .	1
a) MSB b) LSB c) Bits d) Nibble	
	1
19. The base or radix of binary number system is]
20. The quantity of double word is []
UNIT-IV	
1. What is the minimum number of gates required to implement the Boolean	
 tunction (AB+C) if we have to use only 2-input NOR gates? (A) 2 (B) 3 (C) 4 (D) 5 2. A bulb in a staircase has two switches, one switch being at the ground floor 	



and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles (A)an AND gate (B) an OR gate (C) an XOR gate (D) a NAND

3. Match the logic ga5tes in Column A with their equivalents in Column B.



4. For the output F to be 1 in the logic circuit shown, the input combination should be



5) Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate?

6) Which of the following Boolean Expression correctly represents the relation between P, Q, R and M1?

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- 9) The output Y in the circuit below is always '1' when
- (A) two or more of the inputs P,Q,R are '0'
- (B) two or more of the inputs P,Q,R are '1'
- (C) any odd number of the inputs P,Q,R is '0'
- (D) any odd number of the inputs P,Q,R is '1'

- 10. What is the minimum number of gates required to implement the Boolean
- function (AB+CD) if we have to use only 2-input NAND gates?

(A) 2 (B) 3 (C) 4 (D) NONE

1. The Boolean function realized by the logic circuit shown is []

2. The Boolean expression for the output f of the multiplexer shown below is []

3. For the circuit shown in the following figure IO-I3 are inputs to the 4:1 multiplexer R(MSB) and S are control bits [1]

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	A MARK		
	Z		
The output Z can be represented by (A) PQ + PQS + QRS (B) PQ + PQR + PQS (C) PQR + PQRS + QRS (D) PQR + PQRS + QRS			
 4).How can Parallel data be taken out of shift register simultaneously a) Use Q output of the first F.F b) Use Q output of the last F.F c) Tie all Q outputs together d) Use Q output of each F.F 	[]	
5) In a 16-bit Johnson Counter sequence there re totally how many bit patterns a) 2 b) 6 c) 12 d) 24.	[]	
6).A 122-ring counter requires a minimum of a) 10 F.F b) 12 F.F c) 6 F.F d) 2-F.F	[]	
7). A mod-16 counter, holding the count 1001. What will be count after 31 clock [cycles]	s?	
 a) 1000 b) 1010 c) 1011 d) 1101 8) A sequential circuit does not use clock pulse is a) Asynchronous sequential circuit b) Asynchronous sequential circuit 		[]
 c) Counter d) Shift register 9).In a 8- bit ring counter initial state 10111110, what is state after 4th clock pluse c) 11101011 b) 00010111 c) 11110000 d) 00000000 	[]	
10).With 200Hz clock frequency 8 bits can be serially entered into shift register in a) 4 μ s b) 40 μ s c) 400 μ s d) 40 ms	n	[]
UNIT-V 1).If all the flip-flops were reset to 0 at power on, what is the total number of			
distinct outputs (states) represented by PQR generated by the counter? (A) 3 (B) 4 (C) 5 (D) 6	[]	
2. If at some instance prior to the occurrence of the clock edge, P. Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge (A) 000 (B) 001 (C) 010 (D) 011	ı ?[]	
2.For each of the positive edge-triggered J-K flip flop used in the following figure the propagation delay is T	е,	[]
$\begin{array}{cccccccccccccccccccccccccccccccccccc$			

3. Which of the following waveforms correctly represents the output at Q1? []

ALISTIC

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(A)

4.Two D flip-flops are connected as a synchronous counter that goes through the following QBQA sequence $00 \square 11 \square 01 \square 10 \square 00 \square ...$

The combination to the inputs DA and DB are $\frac{1}{2}$

(A)
$$D_A = Q_B$$
; $D_B = Q_A$
(B) $D_A = \overline{Q_A}$; $D_B = \overline{Q_B}$
(C) $D_A = (Q_A \overline{Q_B} + \overline{Q_A} Q_B)$; $D_B = \overline{Q_A}$
(D) $D_A = (Q_A Q_B + \overline{Q_A} Q_B)$; $D_B = \overline{Q_B}$

5.Assuming that flip-flops are in reset condition initially, the count sequence observed at QA in the circuit shown is

(A) 0010111... (B) 0001011... (C) 0101111... (D) 0110100...
6. Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration

7. The minimum number of D flip-flops needed to design a mod-258 counter is [] (A) 9 (B) 8 (C) 512 (D) 258

8. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles []

A) AND gate (B) OR gate (C) XOR gate (D) NAND

9. The minimum number of D flip-flops needed to design a mod-128 counter is [

10. The minimum number of T flip-flops needed to design a mod-32 counter is [] (A) 4 (B) 8 (C) 16 (D) 32 (E) NONE

XII. WEBSITES:

- 1. http://www.onsemi.com
- 2. http://www.kpsec.freeuk.com/symbol.htm
- 3. http://buildinggadgets.com/index_circuitlinks.htm
- 4. http://www.guidecircuit.com
- 5. www.mathsisfun.com/binary-number-system.html
- 6. www.allaboutcircuits.com
- 7. www.electronics-tutorials.ws

XIII. EXPERT DETAILS:

- 1. Mr. S. Srinivasan, Professor, Indian Institute of Technology, Madras
- 2. Dr. P. V. D. Somasekhar Rao (JNTUH)
- 3. Dr. T.Satya Savithri (JNTUH)
- 4. Mrs N Mangala Gouri (JNTUH)
- 5. Dr.D.Rama Krishna (O.U)
- 6. Dr.K.Chandra Bhushana Rao (JNTUK)
- 7. Dr. V. Sumalatha (JNTUA)
- 8. Dr. M.N Giriprasad (JNTUA)

XIV. JOURNALS:

INTERNATIONAL

- 1. IEEE Transaction on Electronic Devices
- 2. International Journal of Micro and Nano Electronics, Circuits and Systems
- 3. Active and Passive Electronic Components (ISSN: 0882-7516)
- 4. International Journal Of Circuits And Architecture Design (IJCAD)

NATIONAL

- 1. Journal of Active and Passive Electronic Devices
- 2. Journal of Electronic Testing
- 3. IETE Journal of Research
- 4. Journal of Electrical Engineering and Electronic Technology
- 5. IET Computers & Digital Techniques

XV. LIST OF TOPICS FOR STUDENT SEMINARS:

- 1. Formation of depletion layer in PN junction diode
- 2. Zener diode as voltage regulator
- 3. Common Collector Configuration
- 4. Need for biasing
- 5. Thermal runaway, thermal stability
- 6. Design of CE amplifier
- 7. MOSFET Characteristics in Enhancement and Depletion Mode

8. Binary adders9. Encoder & Decoder10. Multiplexer11. Flip-flops and latches12. ROM,RAM,PLA,PAL

XVII. CASE STUDIES / SMALL PROJECTS:

- 1. Voltage regulator
- 2. Regulated power supply
- 3. Single stage amplifier
- 4. SCR acts as fastest switch
- 5. FET act as a variable resistor

Half adder using universal Gates.

Simple 2- bit ripple counter.

Basic 8- bit static Memory(RAM) device.