



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**M.Tech. (VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN)**

**COURSE STRUCTURE AND SYLLABUS**

**I Year – I Semester**

Category	Course Title	Int. marks	Ext. marks	L	P	C
Core Course I	VLSI Technology	25	75	4	--	4
Core Course II	CMOS Analog Integrated Circuit Design	25	75	4	--	4
Core Course III	CMOS Digital Integrated Circuit Design	25	75	4	--	4
Core Elective I	Digital System Design Hardware Software Co-Design CPLD and FPGA Architectures and Applications	25	75	4	--	4
Core Elective II	Algorithms for VLSI Design Automation Embedded System Design Device Modeling	25	75	4	--	4
Open Elective I	Soft Computing Techniques Image and Video processing Software Defined Radio	25	75	4	--	4
Laboratory I	VLSI Laboratory – I	25	75	--	4	2
Seminar I	Seminar	50	--	--	4	2
<b>Total Credits</b>				<b>24</b>	<b>8</b>	<b>28</b>

**I Year – II Semester**

Category	Course Title	Int. marks	Ext. marks	L	P	C
Core Course IV	Low Power VLSI Design	25	75	4	--	4
Core Course V	Design for Testability	25	75	4	--	4
Core Course VI	CMOS Mixed Signal Circuit Design	25	75	4	--	4
Core Elective III	VLSI and DSP Architectures Full custom IC Design Hardware Description Language	25	75	4	--	4
Core Elective IV	Optimization Techniques in VLSI Design System On Chip Architecture Semiconductor Memory Design and Testing	25	75	4	--	4
Open Elective II	Scripting Languages Coding Theory and Techniques Adhoc Wireless Networks	25	75	4	--	4
Laboratory II	VLSI Laboratory – II	25	75	--	4	2
Seminar II	Seminar	50	--	--	4	2
<b>Total Credits</b>				<b>24</b>	<b>8</b>	<b>28</b>

**II Year - I Semester**

Course Title	Int. marks	Ext. marks	L	P	C
Comprehensive Viva-Voce	--	100	--	--	4
Project work Review I	50	--	--	24	12
<b>Total Credits</b>			--	24	16

**II Year - II Semester**

Course Title	Int. marks	Ext. marks	L	P	C
Project work Review II	50	--	--	8	4
Project Evaluation (Viva-Voce)	--	150	--	16	12
<b>Total Credits</b>			--	24	16



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)**

**VLSI TECHNOLOGY**

**UNIT –I:**

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits:  $I_{ds} - V_{ds}$  relationships, Threshold Voltage  $V_T$ ,  $G_m$ ,  $G_{ds}$  and  $\omega_o$ , Pass Transistor, MOS, CMOS & BiCMOS Inverters,  $Z_{pu}/Z_{pd}$ , MOS Transistor circuit model, Latch-up in CMOS circuits.

**UNIT –II:**

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

**UNIT –III:**

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

**UNIT –IV**

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

**UNIT –V**

Design rules and Scaling, BiCMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors,

Packaging: Chip characteristics, package functions, package operations

**TEXT BOOKS:**

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

**REFERENCE BOOKS:**

1. Micro Electronics circuits Analysis and Design 2<sup>nd</sup> Edition, Muhammad H Rashid, CENAGE Learning 2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994



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**CMOS ANALOG INTEGRATED CIRCUIT DESIGN**

**UNIT -I:**

**MOS Devices and Modeling**

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

**UNIT -II:**

**Analog CMOS Sub-Circuits:**

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

**UNIT -III**

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

**UNIT -IV**

CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

**UNIT -V**

Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

**TEXT BOOKS:**

CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

**REFERENCE BOOKS:**

Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.

Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.



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**CMOS DIGITAL INTEGRATED CIRCUIT DESIGN**

**UNIT –I:**

**MOS Design:**

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

**UNIT –II:**

**Combinational MOS Logic Circuits:**

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

**UNIT –III:**

**Sequential MOS Logic Circuits:**

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

**UNIT –IV:**

**Dynamic Logic Circuits:**

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

**UNIT –V:**

**Semiconductor Memories:**

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

**TEXT BOOKS:**

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3<sup>rd</sup> Ed., 2011.

**REFERENCE BOOKS:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2<sup>nd</sup> Ed., PHI.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)**

**DIGITAL SYSTEM DESIGN**  
(Core Elective –I)

**UNIT -I:**

**Minimization and Transformation of Sequential Machines:**

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

**UNIT -II:**

**Digital Design:**

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

**UNIT -III:**

**SM Charts:**

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

**UNIT -IV:**

**Fault Modeling & Test Pattern Generation:**

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

**UNIT -V:**

**Fault Diagnosis in Sequential Circuits:**

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

**TEXT BOOKS:**

1. Fundamentals of Logic Design – Charles H. Roth, 5<sup>th</sup> Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

**REFERENCE BOOKS:**

1. Switching and Finite Automata Theory – Z. Kohavi , 2<sup>nd</sup> Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4<sup>th</sup> Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI



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**HARDWARE - SOFTWARE CO-DESIGN**  
(Core Elective –I)

**UNIT –I:**

**Co- Design Issues:**

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

**Co- Synthesis Algorithms:**

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

**UNIT –II:**

**Prototyping and Emulation:**

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

**Target Architectures:**

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

**UNIT –III:**

**Compilation Techniques and Tools for Embedded Processor Architectures:**

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

**UNIT –IV:**

**Design Specification and Verification:**

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

**UNIT –V:**

**Languages for System – Level Specification and Design-I:**

System – level specification, design representation for system level synthesis, system level specification languages,

**Languages for System – Level Specification and Design-II:**

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

**TEXT BOOKS:**

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - [Giovanni De Micheli](#), [Mariagiovanna Sami](#), 2002, Kluwer Academic Publishers

**REFERENCE BOOKS:**

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer



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**CPLD AND FPGA ARCHITECTURES AND APPLICATIONS**  
(Core Elective –I)

**UNIT-I:**

**Introduction to Programmable Logic Devices:**

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

**UNIT-II:**

**Field Programmable Gate Arrays:**

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

**UNIT -III:**

**SRAM Programmable FPGAs:**

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

**UNIT -IV:**

**Anti-Fuse Programmed FPGAs:**

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

**UNIT -V:**

**Design Applications:**

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

**TEXT BOOKS:**

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

**REFERENCE BOOKS:**

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.





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**ALGORITHMS FOR VLSI DESIGN AUTOMATION**  
(Core Elective –II)

**UNIT I**

**PRELIMINARIES**

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

**UNIT II**

**GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION**

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

**UNIT III**

**LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING**

Problems, Concepts and Algorithms.

**MODELLING AND SIMULATION**

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

**UNIT IV**

**LOGIC SYNTHESIS AND VERIFICATION**

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

**HIGH-LEVEL SYNTHESIS**

Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

**UNIT V**

**PHYSICAL DESIGN AUTOMATION OF FPGAs**

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

**PHYSICAL DESIGN AUTOMATION OF MCMs**

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

**TEXT BOOKS**

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3<sup>rd</sup> Ed., 2005, Springer International Edition.

**REFERENCE BOOKS**

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2<sup>nd</sup> ed., 1998, Pearson Education Asia.





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**EMBEDDED SYSTEMS DESIGN**  
(Core Elective –II)

**UNIT -I:**

**Introduction to Embedded Systems**

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

**UNIT -II:**

**Typical Embedded System:**

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

**UNIT -III:**

**Embedded Firmware:**

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

**UNIT -IV:**

**RTOS Based Embedded System Design:**

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

**UNIT -V:**

**Task Communication:** Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

**TEXT BOOKS:**

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

**REFERENCE BOOKS:**

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.



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**DEVICE MODELLING**  
(Core Elective –II)

**UNIT -I:**

**Introduction to Semiconductor Physics:**

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

**Integrated Passive Devices:**

Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

**UNIT -II:**

**Integrated Diodes:**

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

**Integrated Bipolar Transistor:**

Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gummel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

**UNIT -III:**

**Integrated MOS Transistor:**

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

**UNIT -IV:**

**VLSI Fabrication Techniques:** An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

**UNIT -V:**

**Modeling of Hetero Junction Devices:** Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

**TEXT BOOKS:**

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

**REFERENCE BOOKS:**

1. Physics of Semiconductor Devices – Sze S. M, 2<sup>nd</sup> Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011



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**SOFT COMPUTING TECHNIQUES**  
**(Open Elective - I)**

**UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks**

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

**UNIT – II: Associative Memories & ART Neural Networks**

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

**UNIT – III: Fuzzy Logic & Systems**

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

**UNIT – IV: Genetic Algorithms**

Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

**UNIT – V: Hybrid Systems**

Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

**TEXT BOOKS:**

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications -S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

**REFERENCE BOOKS:**

1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.



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**IMAGE AND VIDEO PROCESSING**  
**(OPEN ELECTIVE-I)**

**UNIT –I:**

**Fundamentals of Image Processing and Image Transforms:** Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

**Image Segmentation:** Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

**UNIT –II:**

**Image Enhancement:** Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

**UNIT –III:**

**Image Compression:** Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

**UNIT -IV:**

**Basic Steps of Video Processing:** Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

**UNIT –V:**

**2-D Motion Estimation:** Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

**TEXT BOOKS:**

1. Digital Image Processing – Gonzalez and Woods, 3<sup>rd</sup> Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya-quin Zhang. 1<sup>st</sup> Ed., PH Int.

**REFERENCE BOOKS:**

1. Digital Image Processing using MATLAB– Gonzalez and Woods, 2<sup>nd</sup> ed., Mc Graw Hill Education, 2010
2. Image Processing Analysis , and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE, 2008
3. Digital Video Processing – A Murat Tekalp, PERSON, 2010
4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009



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**SOFTWARE DEFINED RADIO**  
**(Open Elective-I)**

**UNIT -I:**

**Introduction:** The Need for Software Radios, What is Software Radio, Characteristics and benefits of software radio- Design Principles of Software Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front-End Topologies- Enhanced Flexibility of the RF Chain with Software Radios- Importance of the Components to Overall Performance- Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

**UNIT -II:**

**Profile and Radio Resource Management :** Communication Profiles- Introduction, Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data

**UNIT -III:**

**Radio Resource Management in Heterogeneous Networks**

Introduction, Definition of Radio Resource Management, Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks, Measuring Gain in the Upper Bound Due to JRRM, Circuit-Switched System, Packet-Switched System, Functions and Principles of JRRM, General Architecture of JRRM, Detailed RRM Functions in Sub-Networks and Overall Systems

**UNIT -IV:**

**Reconfiguration of the Network Elements :** Introduction, Reconfiguration of Base Stations and Mobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration Based on Comparison, Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

**UNIT -V:**

**Object – Oriented Representation of Radios and Network Resources:**

Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.

**Case Studies in Software Radio Design:** Introduction and Historical Perspective, SPEAK easy-JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT.

**TEXT BOOKS:**

1. Software Defined Radio Architecture System and Functions- Markus Dillinger, Kambiz Madani, WILEY 2003
2. Software Defined Radio: Enabling Technologies- Walter Tuttle Bee, 2002, Wiley Publications.

**REFERENCE BOOKS:**

1. Software Radio: A Modern Approach to Radio Engineering - Jeffrey H. Reed, 2002, PEA Publication.
2. Software Defined Radio for 3G - Paul Burns, 2002, Artech House.
3. Software Defined Radio: Architectures, Systems and Functions - Markus Dillinger, Kambiz Madani, Nancy Alonistioti, 2003, Wiley.
4. Software Radio Architecture: Object Oriented Approaches to wireless System Engineering – Joseph Mitola, III, 2000, John Wiley & Sons.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)**

**VLSI LABORATORY – I**

**Note:**

- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

**Part –I: VLSI Front End Design programs:**

Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters ( synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

**Part –II: VLSI Back End Design programs:**

Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
  - Basic logic gates
  - CMOS inverter
  - CMOS NOR/ NAND gates
  - CMOS XOR and MUX gates
  - CMOS 1-bit full adder
  - Static / Dynamic logic circuit (register cell)
  - Latch
  - Pass transistor

Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech. (VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN)

COURSE STRUCTURE AND SYLLABUS

I Year – II Semester

Category	Course Title	Int. marks	Ext. marks	L	P	C
Core Course IV	Low Power VLSI Design	25	75	4	--	4
Core Course V	Design for Testability	25	75	4	--	4
Core Course VI	CMOS Mixed Signal Circuit Design	25	75	4	--	4
Core Elective III	VLSI and DSP Architectures Full custom Design Hardware Description Language	25	75	4	--	4
Core Elective IV	Optimization Techniques in VLSI Design System On Chip Architecture Semiconductor Memory Design and Testing	25	75	4	--	4
Open Elective II	Scripting Languages Coding Theory and Techniques Adhoc Wireless Networks	25	75	4	--	4
Laboratory II	VLSI Laboratory – II	25	75	--	4	2
Seminar II	Seminar	50	--	--	4	2
<b>Total Credits</b>				<b>24</b>	<b>8</b>	<b>28</b>





**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**LOW POWER VLSI DESIGN**

**UNIT –I:**

**Fundamentals:**

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

**UNIT –II:**

**Low-Power Design Approaches:**

**Low-Power Design through Voltage Scaling** – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

**Switched Capacitance Minimization Approaches:**

System Level Measures, Circuit Level Measures, Mask level Measures.

**UNIT –III:**

**Low-Voltage Low-Power Adders:**

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

**UNIT –IV:**

**Low-Voltage Low-Power Multipliers:**

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

**UNIT –V:**

**Low-Voltage Low-Power Memories:**

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

**TEXT BOOKS:**

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

**REFERENCE BOOKS:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**DESIGN FOR TESTABILITY**

**UNIT -I:**

**Introduction to Testing:**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

**UNIT -II:**

**Logic and Fault Simulation:**

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

**UNIT -III:**

**Testability Measures:**

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

**UNIT -IV:**

**Built-In Self-Test:**

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

**UNIT -V:**

**Boundary Scan Standard:**

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BSDL Description Components, Pin Descriptions.

**TEXT BOOK:**

1 Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.

**REFERENCE BOOKS:**

1. Digital Systems and Testable Design - M. Abramovici, M.A. Breuer and A.D. Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**CMOS MIXED SIGNAL CIRCUIT DESIGN**

**UNIT -I:**

**Switched Capacitor Circuits:**

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

**UNIT -II:**

**Phased Lock Loop (PLL):**

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

**UNIT -III:**

**Data Converter Fundamentals:**

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

**UNIT -IV:**

**Nyquist Rate A/D Converters:**

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

**UNIT -V:**

**Oversampling Converters:**

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

**TEXT BOOKS:**

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

**REFERENCE BOOKS:**

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**VLSI AND DSP ARCHITECTURES**  
(Core Elective –III)

**UNIT I**

Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

**UNIT II**

**Data Path and Control:** Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

**UNIT III**

**Enhancing performance with pipeline:** An overview of pipelining, a pipe lined data path. Pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

**UNIT IV**

**Computational Accuracy in DSP implementations:** Introduction, number formats for signals and coefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors

**UNIT V**

**Architectures for programmable digital signal processing devices:** introduction, basic architectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

**TEXT BOOKS:**

1. Computer Organization and Design: Hard ware/ Software Interface-D.A, Patterson and J.L Hennessy, 4<sup>th</sup> ed., Elsevier, 2011
2. Structural Computer organization, A.S Tannenbaum, 4<sup>th</sup> ed., Prentice-Hall, 1999

**REFERENCE BOOKS:**

1. W. Wolf, Modern VLSI Design: System on Silicon, 2<sup>nd</sup> Ed., Person Education, 1998
2. Keshab Parhi, VLSI Digital Signal Processing system design and implementations, Wiley 1999
3. Avatar sign, Srinivasan S, Digital Signal Processing implementations using DSP microprocessors with examples, Thomson 4<sup>th</sup> reprint, 2004.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**FULL CUSTOM DESIGN**  
(Core Elective –III)

**UNIT I**

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

**UNIT II**

Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals and

**UNIT III**

Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

**UNIT IV**

Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

**UNIT V**

Proper layout CAD tools for layout, Planning tools, Layout generation tools, Support tools.

**TEXT BOOKS:**

1. CMOS IC Layout Concepts Methodologies and Tools, Dan Clein, Newnes, 2000.
2. The Art of Analog Layout, 2nd Edition, Ray Alan Hastings, Prentice Hall, 2006



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**HARDWARE DESCRIPTION LANGUAGE**  
(Core Elective –III)

**UNIT I**

Introduction: About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading

**UNIT II**

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

**UNIT III**

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot

**UNIT IV**

Introduction to Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling.

**UNIT V**

Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior

**TEXT BOOKS**

1. Circuit Design and Simulation with VHDL, Volnei A. Pedroni, 2nd Edition, MIT Press, 2010.
2. Designers Guide to Verilog AMS, Kenneth S Kundert, Olaf Zinke, Springer, 2004



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**OPTIMIZATION TECHNIQUES IN VLSI DESIGN**  
(Core Elective –IV)

**UNIT –I:**

**Statistical Modeling:**

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

**UNIT –II:**

**Statistical Performance, Power and Yield Analysis**

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

**UNIT –III:**

**Convex Optimization:**

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

**UNIT –IV:**

**Genetic Algorithm:**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

**UNIT –V:**

**GA Routing Procedures and Power Estimation:**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

**TEXT BOOKS / REFERENCE BOOKS:**

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall, 1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.





**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**SYSTEM ON CHIP ARCHITECTURE**  
(Core Elective –IV)

**UNIT –I:**

**Introduction to the System Approach:**

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

**UNIT –II:**

**Processors:**

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

**UNIT –III:**

**Memory Design for SOC:**

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

**UNIT -IV:**

**Interconnect Customization and Configuration:**

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

**UNIT –V:**

**Application Studies / Case Studies:**

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

**TEXT BOOKS:**

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2<sup>nd</sup> Ed., 2000, Addison Wesley Professional.

**REFERENCE BOOKS:**

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1<sup>st</sup> Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**SEMICONDUCTOR MEMORY DESIGN AND TESTING**  
(Core Elective –IV)

**UNIT -I:**

**Random Access Memory Technologies:**

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

**UNIT -II:**

**Non-volatile Memories:**

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

**UNIT -III:**

**Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance:** RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

**UNIT -IV:**

**Semiconductor Memory Reliability and Radiation Effects:**

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

**UNIT -V:**

**Advanced Memory Technologies and High-density Memory Packing Technologies:** Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

**TEXT BOOKS:**

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1<sup>st</sup> Ed., Prentice Hall.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**SCRIPTING LANGUAGES**  
**(Open Elective-II)**

**UNIT -I:**

**Introduction to Scripts and Scripting:**

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

**UNIT -II:**

**Advanced PERL:**

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

**UNIT -III:**

**TCL:**

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

**UNIT -IV:**

**Advanced TCL:**

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

**UNIT -V:**

**TK and JavaScript:**

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.

**Object Oriented Programming Concepts (Qualitative Concepts Only):** Objects, Classes, Encapsulation, Data Hierarchy.

**TEXT BOOKS:**

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7<sup>th</sup> Edition, TMH.

**REFERENCE BOOKS:**

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann Series.
2. Tcl and the Tk Toolkit- John Ousterhout, 2<sup>nd</sup> Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**CODING THEORY AND TECHNIQUES**  
**(Open Elective-II)**

**UNIT – I:**

**Coding for Reliable Digital Transmission and storage**

Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

**Linear Block Codes:** Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

**UNIT - II:**

**Cyclic Codes** : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

**UNIT – III:**

**Convolutional Codes** : Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

**UNIT – IV:**

**Turbo Codes**

LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

**UNIT - V:**

**Space-Time Codes**

Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

**TEXT BOOKS:**

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice Hall, Inc.
2. Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill

**REFERENCE BOOKS:**

1. Error Correcting Coding Theory-Man Young Rhee-1989,McGraw – Hill Publishing,19
2. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
3. Digital Communications- John G. Proakis, 5<sup>th</sup> ed., 2008, TMH.
4. Introduction to Error Control Codes-Salvatore Gravano-oxford
5. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley India.
6. Information Theory, Coding and Cryptography – Ranjan Bose, 2<sup>nd</sup> Edition, 2009, TMH.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**AD-HOC WIRELESS NETWORKS**  
**(Open Elective-II)**

**UNIT - I:**

**Wireless Local Area Networks**

Introduction, wireless LAN Topologies, Wireless LAN Requirements, Physical Layer- Infrared Physical Layer, Microwave based Physical Layer Alternatives, Medium Access Control Layer- HIPERLAN 1 Sublayer, IEEE 802.11 MAC Sublayer and Latest Developments-802.11a, 802.11b, 802.11g  
Personal Area Networks: Introduction to PAN technology and Applications, Bluetooth -specifications, Radio Channel, Piconets and Scatternets, Inquiry, Paging and Link Establishment, Packet Format, Link Types, Power Management, Security, Home RF -Physical and MAC Layer

**UNIT - II:**

**MAC Protocols**

Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

**UNIT - III:**

**Routing Protocols**

Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

**UNIT – IV:**

**Transport Layer Protocols**

Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

**UNIT – V:**

**Quality of Service in Ad Hoc Wireless Networks:**

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

**TEXT BOOKS:**

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Networks -P Nicopolitidis and M S Obaidat, Wiley India Edition 2003.

**REFERENCE BOOKS**

1. Wireless Communication Technology- Roy Blake, CENGAGE,2012
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**  
**M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)**

**VLSI LABORATORY - II**

**Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.**

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

***VLSI Back End Design programs:***

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
  - CMOS inverter
  - CMOS NOR/ NAND gates
  - CMOS XOR and MUX gates
  - CMOS half adder and full adder
  - Static / Dynamic logic circuits (register cell)
  - Latch
  - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL