VLSI DESIGN

Subject Code: **(EC702PC)**

Regulations : R16 JNTUH

Class :IV Year B.Tech ECE I Semester-I

Department of Electronics and communication Engineering

BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

Ibrahimpatnam -501 510, Hyderabad

VLSI DESIGN (EC702PC)

COURSE PLANNER

I. Course Over-View

This course provides an introduction to the design and implementation of VLSI circuits for complex digital systems. The focus is on CMOS technology. Issues to be covered include deep submicron design, clocking, power dissipation, CAD tools and algorithms, simulation, verification, testing, and design methodology. The course includes a computer lab component in which you will design and layout different combinational and sequential digital circuits.

II. Pre requisites :

Requires knowledge of physics concepts, basics of electronic devices and circuits, and digital design.

III. Course Objectives:

The objectives of the course are to:

1	Give exposure to different steps involved in the fabrication of ICs using MOS transistor, CMOS/BICMOS transistors, and passive components.
2	Explain electrical properties of MOS and BiCMOS devices to analyze the behavior of inverters designed with various loads.
3	Give exposure to the design rules to be followed to draw the layout of any logic circuit.
4	Provide concept to design different types of logic gates using CMOS inverter and analyze their transfer characteristics.
5	Provide design concepts to design building blocks of data path of any system using gates.
6	Understand basic programmable logic devices and testing of CMOS circuits.

IV. Course Outcomes:

Upon successfully completing the course, the student should be able to:

S.No.	Description	Bloom's Taxonomy Level
1	Acquire qualitative knowledge about the fabrication process of integrated circuit using MOS transistors.	Knowledge, Understand (Level1, Level2)
2	Choose an appropriate inverter depending on specifications required for a circuit	Apply, Create (Level 3, Level 6)

3	Draw the layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Analyze (Level 4)
4	Design different types of logic gates using CMOS inverter and analyze their transfer characteristics	Analyze (Level 4)
5	Provide design concepts required to design building blocks of data path using gates.	Knowledge, Understand (Level1, Level2)
6	Design simple memories using MOS transistors and can understand design of large memories.	Knowledge, Understand (Level1, Level2)
7	Design simple logic circuit using PLA, PAL, FPGA and CPLD.	Analyze (Level 4)
8	Understand different types of faults that can occur in a system and learn the concept of testing and adding extra hardware to improve testability of system	Analyze (Level 4) Analyze (Level 4)

S.No.	Description	Bloom's Taxonomy Level
1	Acquire qualitative knowledge about the fabrication process of integrated circuit using MOS transistors.	Knowledge, Understand (Level1, Level2)
2	Choose an appropriate inverter depending on specifications required for a circuit	Apply, Create (Level 3, Level 6)
3	Draw the layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Analyze (Level 4)
4	Design different types of logic gates using CMOS inverter and analyze their transfer characteristics	Analyze (Level 4)
5	Provide design concepts required to design building blocks of data path using gates.	Knowledge, Understand (Level1, Level2)
6	Design simple memories using MOS transistors and can understand design of large memories.	Knowledge, Understand (Level1, Level2)
7	Design simple logic circuit using PLA, PAL, FPGA and CPLD.	Analyze (Level 4)
8	Understand different types of faults that can occur in a system and learn the concept of testing and adding extra hardware to improve testability of system	Analyze (Level 4) Analyze (Level 4)

V. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Level	Proficiency assessed by
PO1:	**Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems related to Electronics & Communication and Engineering.	2	Assignments, Exercises
PO2:	**Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems related to Electronics & Communication Engineering and reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.	3	Assignments

PO3:	**Design/ Development of Solutions:** Design solutions for complex engineering problems related to Electronics & Communication Engineering and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Assignments, Exercises
PO4:	**Conduct Investigations of Complex Problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Assignments
PO5:	**Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	3	Assignments, Seminars
PO6:	**The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the Electronics & Communication Engineering professional engineering practice.	3	Seminars
PO7:	**Environment and Sustainability:** Understand the impact of the Electronics & Communication Engineering professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	-	-
PO8:	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	-	-
PO9:	**Individual and Team Work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	2	Oral Discussions
PO10:	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	-	-
PO11:	**Project Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	-	-
PO12:	**Life-Long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	-	-

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VI. HOW VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Level	Proficiency assessed by
PSO1:	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	2	Lectures, Assignments
PSO2:	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	2	Tutorials
PSO3:	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	2	Seminars, Projects

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

Bloom's taxonomy Levels
L1. Remember – recalling relevant terminology, specific facts, or different procedures related to information and/or course topics. At this level, a student can remember something, but may not really understand it.
L2. Understand – the ability to grasp the meaning of information (facts, definitions, concepts, etc.) that has been presented.
L3. Apply – being able to use previously learned information in different situations or in problem solving.
L4. Analyze – the ability to break information down into its component parts. Analysis also refers to the process of examining information in order to make conclusions regarding cause and effect, interpreting motives, making inferences, or finding evidence to support statements/arguments.
L5. Evaluate – being able to judge the value of information and/or sources of information based on personal values or opinions.
L6. Create – the ability to creatively or uniquely apply prior knowledge and/or skills to produce new and original thoughts, ideas, processes, etc. At this level, students are involved in creating their own thoughts and ideas.

Course	CO. No	Course Outcomes (CO)	Knowledge Level (Blooms Level)
	CO1	CO-1: Able to analysis the fabricating procedures of different MOS transistors and behavior electrical properties	**L-1**

	CO2	CO-2: An ability to extract the analog parasitic elements from the layout and Analyze the circuit timing using a logic simulator and an analog simulator	**L-2**
	CO3	CO-3: An ability to design elementary data paths for logic circuits, including moderate-speed adders, subracters, and multipliers	**L-3,4**
	CO4	CO-4: Provide design concepts required to design building blocks of data path using gates.	**L-4,6**
	CO5	CO-5: Design simple memories using MOS transistors and can understand design of large memories	**L-4,6**
	CO6	CO-6: Design simple logic circuit using PLA, PAL, FPGA and CPLD And Understand different types of faults that can occur in a system	**L-2,4,6** **L-2,4,6**

Bloom's taxonomy Levels
L1. Remember – recalling relevant terminology, specific facts, or different procedures related to information and/or course topics. At this level, a student can remember something, but may not really understand it.
L2. Understand – the ability to grasp the meaning of information (facts, definitions, concepts, etc.) that has been presented.
L3. Apply – being able to use previously learned information in different situations or in problem solving.
L4. Analyze – the ability to break information down into its component parts. Analysis also refers to the process of examining information in order to make conclusions regarding cause and effect, interpreting motives, making inferences, or finding evidence to support statements/arguments.
L5. Evaluate – being able to judge the value of information and/or sources of information based on personal values or opinions.
L6. Create – the ability to creatively or uniquely apply prior knowledge and/or skills to produce new and original thoughts, ideas, processes, etc. At this level, students are involved in creating their own thoughts and ideas.

Course	CO. No	Course Outcomes (CO)	Knowledge Level (Blooms Level)
COURSE: VLSI DESIGN	CO1	CO-1: Able to analysis the fabricating procedures of different MOS transistors and behavior electrical properties	**L-1**
	CO2	CO-2: An ability to extract the analog parasitic elements from the layout and Analyze the circuit timing using a logic simulator and an analog simulator	**L-2**
	CO3	CO-3: An ability to design elementary data paths for logic circuits, including moderate-speed adders, subracters, and multipliers	**L-3,4**
	CO4	CO-4: Provide design concepts required to design building blocks of data path using gates.	**L-4,6**
	CO5	CO-5: Design simple memories using MOS transistors and can understand design of large memories	**L-4,6**
	CO6	CO-6: Design simple logic circuit using PLA, PAL, FPGA and CPLD And Understand different types of faults that can occur in a system	**L-2,4,6** **L-2,4,6**

VII. SYLLABUS:

UNIT – I

Introduction: Introduction to IC Technology – MOS, PMOS, NMOS, CMOS & BiCMOS

Basic Electrical Properties: Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships, MOS transistor threshold Voltage, gm, gds, Figure of merit ωo; Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS

Inverters.

UNIT - II

VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, 2 μm CMOS Design rules for wires, Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits.

UNIT – III

Gate Level Design: Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Time delays, Driving large capacitive loads, Wiring capacitance, Fan – in, Fan – out, Choice of layers.

UNIT - IV

Data Path Subsystems: Subsystem Design, Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Zero/One Detectors, Counters.

Array Subsystems: SRAM, DRAM, ROM, Serial Access Memories.

UNIT - V

Programmable Logic Devices: PLAs, FPGAs, CPLDs, Standard Cells, Programmable Array Logic, Design Approach, Parameters influencing low power design.

CMOS Testing: CMOS Testing, Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques.

TEXT BOOKS:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition
2. CMOS VLSI Design – A Circuits and Systems Perspective, Neil H. E Weste, David Harris, Ayan Banerjee, 3rd Ed, Pearson, 2009.

REFERENCE BOOKS:

1. CMOS logic circuit Design - John .P. Uyemura, Springer, 2007.
2. Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.

VIII. COURSE PLAN (WEEK-WISE):

The course will proceed as follows for all sections. Please note that the week and the classes in each week are relative to each section.

Lecture	Week	Topic	Course Learning Outcomes	Teaching Methodology	Reference
UNIT – 1					
1	1	Introduction to IC Technology – MOS	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	T1,T2,R1
2		Introduction to IC Technology – MOS	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
3		Introduction to IC Technology – MOS	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
4		PMOS, NMOS	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
5	2	CMOS	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
6		CMOS	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
7		BiCMOS Technologies	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
8		BiCMOS Technologies	**Knowledge** :About the fabrication process of MOS transistors.	Chalk and Talk	
9	3	Basic Electrical Properties : Basic electrical properties of MOS and BiCMOS circuits	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	T1,T2,R1
10		Ids – Vds relationships	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
11		MOS transistor threshold voltage	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
12		gm, gds, Figure of merit wo	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
13	4	Pass transistor, NMOS Inverter	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
14		Various pull ups	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	

15		CMOS inverter analysis and design	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
16		Bi-CMOS inverters	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
UNIT -2					
17	5	VLSI Circuit Design Process : VLSI design flow	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	**T1,T2,R1**
18		MOS layers, Stick diagrams	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
19		Design rules and layout	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
20		2um CMOS design rules for wires	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
21	6	Contacts and Transistors layout diagrams for NMOS and CMOS inverters and Gates	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
22		Contacts and Transistors layout diagrams for NMOS and CMOS inverters and Gates	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
23		Scaling of MOS circuits	**Understanding:** layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit	Chalk and Talk	
24		**MOCK TEST-1**			
UNIT-3					
25	7	Gate Level design : logic Gates and other complex gates	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	**T1,T2,R1**
26		Switch logic	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
27		Alternative gate circuits	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
28		**BRIDGE**			
29		Time delays	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	

30	8	Driving large capacitive loads	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
31		Wiring capacitance	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
32		**BRIDGE**			
33	9	**Mid 1 Exams**			
UNIT- 4					
34	10	Choice of layers	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	**T1,T2,R1**
35		Fan-in, Fan-out	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
36		**(UNIT-04)** Data Path Subsystems : Subsystem Design	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
37		Shifters	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
38	11	Adders	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
39		Adders	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
40		ALUs	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
41		**BRIDGE**			
42	12	Multipliers	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	**T1,T2,R1**
43		Multipliers	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
44		Parity generators, Comparators	**Analyzing & Design**: different types of logic gates using CMOS inverter and their transfer characteristics	Chalk and Talk	
45		**BRIDGE**			
46		Array Subsystems : SRAM	**Design:** Simple memories using MOS transistors and understand design of large memories.	Chalk and Talk	

47	13	DRAM	**Design:** Simple memories using MOS transistors and understand design of large memories.	Chalk and Talk	
48		ROM	**Design:** Simple memories using MOS transistors and understand design of large memories.	Chalk and Talk	
49		Serial Access Memories,Content Addressable Memory	**Design:** Simple memories using MOS transistors and understand design of large memories.	Chalk and Talk	
UNIT-5					
50	14	Semiconductor Integrated Circuit Design : PLAs	**Design:S**imple logic circuit using PLA, PAL, FPGA and CPLD	Chalk and Talk	**T1,T2,R1**
51		FPGAs,	**Design:S**imple logic circuit using PLA, PAL, FPGA and CPLD	Chalk and Talk	
52		CPLDs,Standard cells	**Design:S**imple logic circuit using PLA, PAL, FPGA and CPLD	Chalk and Talk	
53		**MOCK TEST-2**			
54	15	Programmable Array Logic	**Design:S**imple logic circuit using PLA, PAL, FPGA and CPLD	Chalk and Talk	
55		Design Approach	**Design:S**imple logic circuit using PLA, PAL, FPGA and CPLD	Chalk and Talk	
56		Parameters influencing low power design	**Design:S**imple logic circuit using PLA, PAL, FPGA and CPLD	Chalk and Talk	
57		**BRIDGE**			
58	16	CMOS Testing : CMOS testing	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	**T1,T2,R1**
59		Need for Testing	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	
60		Test principles	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	
61		Design Strategies for test	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	
62	17	Chip level test techniques	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	
63		System level test techniques	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	
64		Layout design for improved testability	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	
65		Layout design for improved testability	**Understand:** Different types of faults that can occur in a system and learn the concept of testing	Chalk and Talk	

66		**Mid 2 Exams(week 18)**			

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

CO-PO Matrix	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
Course Outcomes (COs)	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO-1:	2	-	3	-	2	-	-	-	-	-	-	-	-	3	1
CO-2:	1	3	3	-	-	-	-	-	-	-	-	-	2	2	2
CO-3:	3	3	3	3	-	2	-	-	-	-	-	-	3	2	2
CO-4:	1	-	3	3	2	3	-	-	2	-	-	-	2	2	2
CO-5:	1	2	3	2	3	-	-	-	-	-	-	-	1	1	3
CO-6:	1	2	3	3	3	-	-	-	-	-	-	-	1	2	3
Average	1.5	2.5	3	2.75	2.5	2.5	-	-	2	-	-	-	1.8	2	2.17

X.JNTU & IMPORTANT Exam Questions

S. No	Questions	Blooms Taxonomy Level	Course Outcome
	UNIT-I **INTRODUCTION AND BASIC ELECTRICAL PROPPERTIES**		
	PART-A (SHORT ANSWER QUESTIONS)		
1	What are the advantages of IC technology	Remember	1
2	What is Moore's law? Explain its relevance with respect to evolution of IC technology.	Understand	1
3	With a neat sketch explain CMOS fabrication using n-well process.	Understand	1
4	Elaborate steps in nMOS fabrication process with suitable sketch.	Understand	1
5	Explain steps in pMOS fabrication	Understand	1
6	Explain steps in p-well process of CMOS fabrication.	Understand	1
7	Explain steps in n-well process of CMOS fabrication.	Understand	1
8	What is meant by twin-tub process and explain where it is used.	Understand	1
9	With a neat sketch explain BiCMOS fabrication in p-well process.	Understand	1
10	What are advantages of BiCMOS process over CMOS technology	Remember	1
	PART-B (LONG ANSWER QUESTIONS)		
1	Draw a neat sketch of CMOS inverter fabricated using n-well process.	Understand	1

2	What is Moore's law? Explain its relevance with respect to evolution of IC Technology.	Understand	1
3	With neat sketches necessary, explain the oxidation process in the IC fabrication process.	Understand	1
4	Explain clearly the fabrication of nMOS ICs with neat sketches.	Understand	1
5	Explain clearly the fabrication of BiCMOS ICs with neat sketches.	Understand	1
6	Explain an enhancement mode & depletion mode transistor operation with relevant diagrams.	Understand	1
7	An nMOS transistor is operated in the triode region with the following parameters $V_{GS} = 4V$; $V_{tn} = 1V$; $V_{DS} = 2V$; $W/L = 100$; $\mu_n C_{ox} = 90A/V^2$. Find its drain current and drain source resistance.	Analyze, Understand	1
8	An pMOS transistor is operated in the active region with the following parameters $V_{GS} = -4.5V$; $V_{tp} = -1V$; $V_{DS} = 2V$; $W/L = 95$; $\mu_n C_{ox} = 95\ A/V^2$. Find its drain current and drain source resistance.	Analyze, Understand	1
9	Derive an equation for Transconductance of an n-channel enhancement MOSFET operating in Active region.	Understand	1

UNIT-II
VLSI CIRCUIT DESIGN PROCESSES

PART-A (SHORT ANSWER QUESTIONS)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Explain VLSI design flow.	Understand	2
2	Describe Stick Diagram.	Remember	2
3	List the uses of Stick diagram.	Remember	2
4	List the various types of color coding used in stick diagram.	Remember	2
5	Explain different MOS layers.	Understand	2
6	Sketch a stick diagram for 2 input nMOS NAND gate.	Remember	2
7	List the types of design rules.	Remember	2
8	Sketch a Transistor related design rules (Orbit 2 μm CMOS) minimum sizes and overlaps.	Remember	2
9	Sketch the aspects of λ-based design rules for contacts, including some factors contributing to higher yield/reliability.	Remember	2
10	Sketch the stick diagram for 2 input nMOS nor gate.	Remember	2
11	Describe Scaling.	Remember	2
12	Explain about transistor design rules for Nmos.	Understand	2
13	Describe layout diagram.	Remember	2
14	Sketch stick diagram for nMOS inverter.	Analyze	2

PART-B (LONG ANSWER QUESTIONS)

1	Explain clearly the nMOS Design style with neat sketches.	Understand	2
2	Explain clearly the CMOS Design style with neat sketches.	Understand	2

3	(a) What is a stick diagram? Sketch the stick diagram and layout for a CMOS inverter. (b) What are design rules? Why is metal- metal spacing larger than poly– poly spacing.	Understand	2 2
4	Sketch the stick diagram for the NMOS implemented of the Boolean expression Y=AB+C.	Remember	2
5	Sketch a Schematic and Cell Layout with neat diagrams. Explain λ-based design rules for contact cuts and vias with neat diagram.	Remember	2
6	Draw the circuit schematic and stick diagram of CMOS 2-Input NAND Gate.	Remember	2
7	Sketch the transistor level diagram for the expression Y=AB+CD and also get the corresponding Stick diagram representation using CMOS logic.	Analyze	2
8	Define Scaling. What are the factors to be considered for transistor scaling?	Remember	2
9	Define constant voltage scaling and give necessary equations.	Remember	2
10	Explain with suitable examples how to design the layout of a gate to maximize performance and minimize area.	Remember	2
11	Sketch a stick diagram for a CMOS gate computing Y=A+B+C+D and estimate the cell width and height.	Understand	2
12	Design a layout diagram for the CMOS logic given Y =A B·C .	Analyze	2
13	Design a stick diagram for the CMOS logic given Y= A B C.	Analyze	2
14	Design a stick diagram for two input pMOS NAND and NOR gates.	Analyze	2
15	Design a stick diagram for the CMOS logic for AB CD.	Analyze	2
16	Design a layout diagram for the pMOS logic Y A(B C.)	Analyze	2
17	Design a layout diagram for two input nMOS NAND gate.	Analyze	2
18	Design a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers.	Analyze	2
19	Draw the stick diagram and mask layout for a CMOS two input NOR gate.	Remember	2

UNIT-III
GATE LEVEL DESIGN

PART-A (SHORT ANSWER QUESTIONS)

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Give the different symbols for transmission gate representation.	Remember	3
2	What is pass transistor?	Understand	3
3	What is sheet resistance?	Remember	3
4	Define Rise time.	Understand	3
5	Define Fall time.	Remember	3
6	Define Delay time.	Remember	3
7	What are the other forms of CMOS logic?	Understand	4
8	Draw AND gate with pass transistors.	Remember	4

9	Explain why D latch is called level sensitive latch.	Understand	4
PART-B (LONG ANSWER QUESTIONS)			
1	Draw the CMOS implementation of 4-to-1 MUX using transmission gates.	Remember	3
2	Explain the VLSI design flow with a neat diagram.	Understand	3
3	Explain the Transmission gate and tri state inverter briefly.	Understand	3
4	Clearly explain the AOI implementation using CMOS design style with neat diagrams.	Understand	4
5	Design a 2-input multiplexer using CMOS transmission gates.	Analyze	4
6	Explain clocked CMOS logic and n-p CMOS logic. Mention their advantages and disadvantages.	Understand	4
7	Explain dynamic CMOS logic and give its advantages and disadvantages.	Understand	4
8	Explain CMOS domino logic and give its advantages and disadvantages.	Understand	4
9	Explain PSEUDO nMOS Logic give with advantages and disadvantages.	Understand	4
PART-C (ANALYTICAL QUESTIONS)			
1	Realize the function f=AB+CD using pseudo-nMOS logic.	Remember	3
2	Realize the function f =A+BC using pseudo –nMOS logic.	Remember	3
3	Derive the expression for rise and fall time of CMOS inverter. Comment on the expression derived.	Understand	4
4	Realize the function f=ABD+BCD using pseudo-nMOS logic.	Remember	4
5	Realize the function f =AB+CD using CMOS static logic.	Remember	4
6	Explain D latch using MUX and transmission gate.	Understand	3
7	Calculate ON resistance from VDD to GND for the given inverter, if n- channel sheet resistance is $2x10_4\Omega$/square.	Understand	3
8	Explain 4:1MUX using transmission gate.	Understand	3
UNIT-IV DATA PAT SUB SYSTEMS			
PART-A (SHORT ANSWER QUESTIONS)			
S. No	**Questions**	**Blooms Taxonomy Level**	**Course Outcome**
1	What is a data path subsystem?	Remember	5
2	What is a shifter?	Remember	5
3	What is the difference between shifter and barrel shifter?	Remember	5
4	Write the truth table for 1-bit full adder.	Remember	5
5	Draw the circuit of one detector with AND gates.	Remember	5
6	Draw the circuit of zero detector with AND gates.	Understand	5
7	What is comparator?	Remember	5
8	Draw the circuit of comparator.	Remember	5
9	What is parity generator?	Remember	5
10	What is the difference between synchronous and asynchronous counter.	Remember	5

11	Write categories of memory arrays.	Remember	5
12	What is RAM.	Understand	5
13	What is ROM.	Understand	5
14	What is Serial access memory.	Understand	5
15	What is Content Addressable Memory.	Understand	5
16	Draw the 6-Transistor SRAM cell.	Remember	5
17	Draw the 1-Transistor DRAM cell.	Remember	5
18	What are the different types of serial access memories.	Remember	5
19	What is flash memory?	Remember	5
20	What are the different types of ROMs?	Remember	5
21	Explain the principle of SRAM.	Understand	5
22	Discuss the advantages of SRAM.	Understand	5
23	Explain the principle of DRAM.	Understand	5
24	Discuss the advantages of Flash memory.	Understand	5
PART-B (LONG ANSWER QUESTIONS)			
1	Describe half adder and Full adder.	Understand	5
2	Draw the logic diagram of zero/one detector and explain its operation with the help of stick diagram.	Remember	5
3	Draw the schematic of Array Multiplier. Explain its principle and operation.	Remember	5
4	Explain the carry look ahead Adder.	Understand	5
5	Explain the design hierarchies and bring out which kind of approach is better to adopt for system design.	Remember	5
6	Describe briefly n-bit parallel adder.	Understand	5
7	Draw the structure of barrel shifter and explain its operation.	Remember	5
8	How Boolean functions are performed using MUX. Discuss 1-bit CMOS implementation of ALU.	Understand	5
9	Sketch the schematic of serial parallel multiplier and explain its operation.	Remember	5
10	Discuss synchronous and asynchronous counters.	Remember	5
11	Discuss in detail about classification of memory arrays.	Understand	5
12	Explain the memory cell read and write operation of 6T SRAM with neat sketches.	Understand	5
13	Explain the principles of SRAM and DRAM.	Understand	5
14	What are the advantages of SRAM and DRAM? Distinguish each property.	Remember	5
15	Explain the read and write operations of 1T DRAM memory cell.	Remember	5
16	Explain the read and write operations of 3T DRAM memory cell.	Remember	5
17	Explain about NAND based ROM design.	Remember	5
18	Explain about NOR based ROM design.	Remember	5
19	Discuss about different types of ROMs.	Remember	5
20	Explain various types of serial access memories with sketches.	Understand	5
21	What is content addressable memory and give any one application of it?	Understand	5

PART-C (ANALYTICAL QUESTIONS)			
1	Draw circuit diagram of one transistor with capacitor dynamic RAM and also draw its layout.	Remember	5
2	Draw the circuit diagram for 4X4 barrel sifter using complementary transmission gates and explain its shifting operation.	Remember	5
3	Design an Incrementer circuit using counter.	Analyze	5
4	Design ripple structure for one-zero detector circuit.	Analyze	5
5	Design a comparator using XNOR gates.	Analyze	5
6	Design sum and carry expressions of carry look ahead adder using Nmos Logic.	Analyze	5
7	Design a 4-bit array multiplier and implement using basic gates.	Analyze	5
8	Implement JK flip-flop using PROM.	Understand	5
9	Implement 2-bit comparator using PAL logic.	Understand	5
10	Draw and explain the antifuse structure for programming the PAL device.	Remember	5
11	Implement Y =A.C+AB +ACD using programmable logic array (PLA).	Understand	5
12	Implement Y =A.C+AB +ACD using programmable array logic (PAL).	Understand	5
13	Implement Y =A.C+AB +ACD using programmable logic read only memory (PROM).	Understand	5
14	Design a 1-bit full adder and implement the sum and carry expressions using PLA.	Analyze	5

UNIT-V
SEMICONDUCTOR INTEGRATD CIRCUIT DESIGN AND CMOS TESTING

PART-A (SHORT ANSWER QUESTIONS)			
S. No	Questions	**Blooms Taxonomy Level**	**Course Outcome**
1	Name the different types of ASICs.	Remember	6
2	Analyze full custom ASIC design.	Understand	6
3	Analyze the standard cell-based ASIC design.	Understand	6
4	Differentiate between channeled and channel less gate array.	Remember	6
5	Explain about FPGA.	Understand	6
6	Explain about Antifuse technology.	Understand	6
7	Explain about Programmable Interconnects.	Understand	6
8	List the steps in ASIC design flow.	Remember	6
9	Discuss the parameters influencing low power design.	Understand	6
10	Explain about CPLD.	Understand	6
11	State the levels at which testing of a chip can be done.	Remember	6
12	Discuss the categories of testing.	Understand	6
13	Explain functionality tests.	Understand	6
14	Explain manufacturing tests.	Understand	6
15	Discuss the defects that occur in a chip.	Understand	6
16	Explain about fault models.	Understand	6
17	Analyze Stuck–At fault.	Understand	6

18	Explain fault models with relevant examples.	Understand	6
19	Discuss about Observability.	Understand	6
20	Discuss about Controllability.	Understand	6
21	Explain various approaches in design for testability.	Understand	6
22	Mention the common techniques involved in ad hoc testing.	Remember	6
23	Analyze the scan-based test techniques.	Understand	6
24	Analyze the self-test techniques.	Understand	6
25	Discuss the applications of chip level test techniques.	Understand	6
26	Explain boundary scan.	Understand	6
27	Analyze Test access port.	Understand	6
28	Explain about Boundary scan register.	Understand	6
PART-B (LONG ANSWER QUESTIONS)			
1	Discuss the different methods of programming of PALs.	Understand	6
2	Distinguish PLAs, PALs, CPLDs, FPGAs, and standard cells in all respects.	Remember	6
3	Explain about the principle and operation of FPGAs. What are its applications?	Understand	6
4	Draw the schematic of PLA and explain its principle of operation.	Remember	6
5	What are the advantages of PLAs?	Understand	6
6	Draw the schematic and examine how Full Adder can be implemented using PLAs.	Remember	6
7	Explain about configurable FPGA based I/O blocks.	Understand	6
8	Design JK Flip flop circuit using PLA.	Analyze	6
9	Explain semicustom design approach of an IC.	Understand	6
10	Compare semicustom and full custom designs of an IC.	Remember	6
11	Explain the various DFT techniques.	Understand	6
12	Explain system-level test techniques.	Remember	6
13	Explain about memory-self test with the help of a schematic.	Understand	6
14	Analyze the issues to be considered while implementing BIST and explain each.	Remember	6
15	Explain how layout design can be done for improving testability.	Remember	6
16	Explain about different fault models in VLSI testing with examples.	Remember	6

XI. JNTU Objective questions

UNIT- 1

1. Starting material for CMOS Technology is
a) <100> b) <101> c) <110> d) <111> [ ]

2. Decomposing of BJT in CMOS Technique results -- latch up
Prevention b) Formation [ ]
c) PNPN structure function b) Formation of BJT

3. _____is used as gate material
Polysilicon b) Si c) Cu d) Al [ ]

4. Boron used to adjust the
a. Threshold voltage b) Current c) Power d) Inductance [ ]

5. Which MOS transistor passes strong logic '1' [ ]
a. pMOS b) nMOS c) (a) & (b) d) None

6. . Pinchoff occurs in---------- region [ ]
a) Non saturation b) Saturation c) cutoff d) linear

7. The drain current flow in ideally independent of drain –source voltage when the channel is [ ]
a. strongly depleted b) weakly depleted c) strongly inverted d) weakly inverted

8. process is used to transfer the layout pattern from masks to wafer. [ ]
a. Diffusion b) Isolation c) photolithographic d) metallization

9. According to Moore's law, the number of transistors that could be manufactured on a chip [ ]
linearly decreases b) grows exponentially c) grows linearly d) decreases exponentially

10. The transistor threshold voltage, V_T is---------- for P type transistor.
Positive b) negative c) zero d) Infinity [ ]

UNIT-2

1. Pick out the advantageof IC [ ]
a) Smaller physical size b) Low power consumption c) Reduced cost d) All

2. In the MOSFET, as width of channel increases I_d [ ]
a) Increases b) decreases c) Constant d) none

3. Latch – up is caused by [ ]
a) Parasitic R b) Parasitic BJT's c) (a) & (b) d) Parasitic C

4. Pick up latch-up resistant CMOS process [ ]
a) n well b) p well c) silicon on Insulator d) all

5. Cascaded inverters are used to drive large_____loads [ ]
a) Capacitive b) resistive c) inductive d) all

6. In which process (CMOS) pFETs are embedded in n well [ ]
a) p well b) n well c) SOI d) all

7. In the Pseudo-nMOS logic ---------- transistor is used as pull-up resistor [ ]
a)pMOS b) nMOS c) Bipolar d) Unijunction

8. Latch structure is used in---------- Logic [ ]

a)Pseudo-nMOS b) DCVS c) Domino d) all

9. Routing channel is spacing between [ ]

a)cell rows b) cells c) wires d) None

10. Feed throughs are used during [ ]

a)Placement b) Routing c) Floor planning d) Synthesis

11. For n-type transistor threshold voltage is _____ [ ]

a) Positive b) negative c) zero d) none

12. In the twin tub process_____wafer is used [ ]

a) p-doped b) n-doped c) undoped d) none

UNIT- 3

1. The smallest feature size of a transistor is [ ]

a) 4λ x 4λ b) 2λ x 2λ c) 8λ x 8λ d) 1λ x 1λ

2. The inverter pair delay for inverter having 4:1 ratio is [ ]

a) 4τ b) 1τ c) 2 τ d) 5τ

3. Metal to metal contact is called ---------- [ ]

a) Buried contact b) Butting contact c) Via d) contact out

4. The capacitance that is caused by the edges of conductor is ---------- capacitance.

a. Fringing field capacitance b) Diffusion capacitance [ ]

c) Gate to channel capacitance d) Area capacitance.

5. Measure of quality of logic circuit family is [ ]

a).Speed power product b) Voltage c) Days d) Current

6. The following is one of the method for CMOS Technology

a) Twin tub b) Three tub c) Four tub d) Five tub [ ]

7. .In Bi-polar Technology is used to get small diffusion coeffecient

a) Antimony b) Phosphorous c) Gold d) Copper [ ]

8..Base Collector capacitance can be minimized is n epitaxial layer is

a) Lightly doped b) Heavily doped c) Moderate d) no doping [ ]

9. Power Consumption of CMOS circuits depends on [ ]

a. Switching frequency b) load capacitance c) Supply voltages d) all

10. Cascaded inverters are used to drive large loads [ ]

a. Capacitive b) resistive c) inductive d) all

UNIT- 4

1. The carry chain in adder is consist with [ ]
   a. cross-bar swith b. transmission gate c. bus interconncection d. pass transistors
2. The type of switch used in shifters is [ ]
   a. line switch c. crossbar switch
   b. transistor type switch d.gate switch
3. For a four bit word, a one-bit shift right is equivalent to a [ ]
   a. two bit shift left c. one bit shift left
   b. three-bit shift left d.four-bit shift left
4. Structured design begins with the concept of [ ]
   a. Hierarchy b. down-top design
   c. bottom level design d. complex function design
5. To simplify the subsystem design, we generally used the [ ]
   a. interdependence c. regular structures
   b. complex interconnections d.standard cells
6. System design is generally in the manner of [ ]
   a. down-top b.top-down c.bottom level only d.top level only
7. The subsystem design is classified as [ ]
   a. first level c. bottom level
   b. top level d.leaf-cell level
8. The parity information (p_i) passed from one cell to the next is modified when the input line (A_i) is at the state of [ ]
   a. zero b.overline$\{A\}_i$ c.one d.independent of input line state
9. The standard cell for an n-bit parity generator is [ ]
   a. n-1 bit cell c. two bit cell
   b. one bit cell d.n+1 bit cell
10. To fast an arithmetic operations, the multipliers and dividers is to use architecture of [ ]
   a. parallel b.serial c. pipelined d.switched

UNIT-5

1. The PLA provides a systematic and regular way of implementing multiple output functions of n variables in [ ]
   a. POS form b.SOP form c.complex form d.simple form
2. A CMOS PLA is realized by [ ]
   a. pseudo nmos NOR gate c.CMOS NOR gate
   b. pseudo nmos NAND gate d.CMOS NAND gate
3. A MOS PLA is realized by using the gate of [ ]
   a. AND b.OR c.AND-OR d.NOR
4. The general arrangement of PLA is [ ]
   a. AND/OR structure
   b. OR/AND structure
   c. NAND/NOR structure
   d. EX-OR/OR structure
5. To realize any finite state machine requirements, the PLA along with [ ]
   a. NOR gate is used
   b. feed back links is used

c. NAND gate is used
d. NOT gate is used

6. To reduce the PLA dimensions, the simplification must be done on a [ ]

a. individual output basis
b. multi-output basis
c. individual product term
d. individual input basis

7. The advantage of fuse-based FPGAS compared to other FPGAs is [ ]

a. allows large number of interconnections b. complex fabrication process
b. larger in size d. modified without changing hardware

8. Generally the system is partitioned for testing because [ ]
]

a. reducing the chip area
b. reducing the no. of pads
c. reducing the number of test vectors
d. reduce the required power

9. The logic cells in FPGA contains [ ]

a. only combinational circuits
b. only sequential circuits
c. both combinational & sequential circuits
d. only Flip-Flop circuits

10. The individual cells of FPGA are interconnected by [ ]

a. AND gates and switches
b. matrix of wires and programmable switches
c. OR gates and non programmable switches
d. AND & OR gates

XII. WEBSITES:

www.asic-world.com
www.edaboard.com
www.synopsys.com
www.cadence.com
www.mentor.com
www.xilinx.com

XIII. List of Journals

INTERNATIONAL:

1. IEEE Transactions on VLSI systems

2. Solid-state circuits Magazine IEEE

3. Electron Devices Magazine IEEE

4. Nano Technology IEEE

NATIONAL:

1. IETE Journal of Research
2. Journal of VLSI Design
3. IETE Journal on Technical Review

XIV. EXPERT DETAILS:

1. Dr. N.S. Murthy Head ECE,
   Dept. NIT. Warangal
   email:nsm@nitw.ernet.in
2. Dr. K.S.R. Krishna Prasad.
   Prof. ECE. Dept. NIT. Warangal
   email:krish@nitw.ernet.in
3. Mr.R.V.G. Anjaneyulu
   Engr/SC-D NRSA,
   Balanagar Hyderabad

XV. LIST OF TOPICS FOR STUDENT SEMINARS:

1. Latest trends in FPGA architecture
2. VLSI Design tools
3. DFT techniques
4. Comparision on SRAM,DRAM memories
5. Comparision of vlsi design technologies
6. GaAs technology.
7. Xilinx FPGA family
8. Altera FPGA families
9. Actel FPGA families

XVI. CASE STUDIES / SMALL PROJECTS:

1. Serial Transmitter / Receiver (UART)
2. Hamming code correction for SRAM
3. 16-bit RISC CPU