DIGITAL ELECTRONICS

Subject Code : EE403PC
Regulations : R18 - JNTUH
Class : II Year B.Tech EEE II Semester

Department of Electrical and Electronics and Engineering

BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

Ibrahimpatnam - 501 510, Hyderabad

DIGITAL ELECTRONICS (EE403PC)
COURSE PLANNER

I. COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors. In this course IC applications acquaints the students with general analog principles and design methodologies using practical devices and applications. It focuses on process of learning about signal condition, signal generation, instrumentation, timing and control using various IC circuitry.This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. PREREQUISITS:

1. The Pre-requisites for this Course is Analog Electronics.

III. COURSE OBJECTIVES:

1.	To learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
2.	To understand common forms of number representation in digital electronic circuits and to be able to convert between different representations.
3.	To implement simple logical operations using combinational logic circuits.
4.	To design combinational logic circuits, sequential logic circuits.
5.	To impart to student the concepts of sequential circuits, enabling them to analyze sequential systems in terms of state machines.
6.	To implement synchronous state machines using flip-flops.

IV. COURSE OUTCOMES:

S.No.	Description	Bloom's Taxonomy Level
1.	***Understand*** working of logic families and logic gates.	Knowledge, Understand (Level 1, Level 2)
2.	***Design*** and implement Combinational and Sequential logic circuits.	Knowledge, Understand, Apply, Analyze (Level 1, Level 2, Level 3, Level 4)
3.	***Understand*** the process of Analog to Digital conversion and Digital to Analog conversion.	Knowledge, Understand, Apply, Analyze (Level 1, Level 2, Level 3,

		Level 4)
4.	Be able to ***Apply*** PLDs to implement the given logical problem.	Knowledge, Understand, Apply, Analyze (Level 1, Level 2, Level 3, Level 4)

V. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (PO)		Level	Proficiency assessed by
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems related to Electronics & Communication and Engineering.	3	Lectures, Assignments, Exercises
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems related to Electronics & Communication Engineering and reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	3	Handson Practice Sessions
PO3	**Design/development of solutions**: Design solutions for complex engineering problems related to Electronics & Communication Engineering and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Design Exercises, Projects
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Labsessions, Exams
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	3	Design Exercises,Oral discussions
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the Electronics & Communication Engineering professional engineering practice.	2	Discuss, Exams

Program Outcomes (PO)		Level	Proficiency assessed by
PO7	**Environment and sustainability**: Understand the impact of the Electronics & Communication Engineering professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	-	--
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	-	--
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	3	Seminars Discussions
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	2	Seminars, Paper Presentations
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	-	--
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	2	Development of Mini Projects

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO 1	Talented to analyze, design, and implement electrical & electronics systems and deal with the rapid pace of industrial innovations and developments.	2	Lectures, Assignments.
PSO 2	Skillful to use application and control techniques for research and advanced studies in Electrical & Electronics Engineering domain.	3	Participate events, seminars & symposiums

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VII. SYLLABUS:

Course syllabus: (JNTUH)

UNIT - I Fundamentals of Digital Systems and Logic Families: Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations, Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic, one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital lCs, digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.

UNIT - II Combinational Digital Circuits: Standard representation for logic functions, K-map representation, and simplification of logic functions using K-map, minimization of logical functions. Don't care conditions, Multiplexer, De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial ladder, ALU, elementary ALU design, popular MSI chips, digital comparator, parity checker/generator, code converters, priority encoders, decoders/drivers for display devices, Q-M method of function realization.

UNIT - III Sequential Circuits and Systems: A 1-bit memory, the circuit properties of Bi-stable latch, the clocked SR flip flop, J, K, T and D types flip-flops, applications of flip-flops, shift registers, applications of shift registers, serial to parallel converter, parallel to serial converter, ring counter, sequence generator, ripple (Asynchronous) counters, synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.

UNIT - IV A/D and D/A Converters: Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter, specifications for D/A converters, examples of D/A converter lCs, sample and hold circuit, analog to digital converters: quantization and encoding, parallel comparator A/D converter, successive approximation A/D converter, counting A/D converter, dual slope A/D converter, A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters, example of A/D converter ICs

UNIT - V Semiconductor Memories and Programmable Logic Devices: Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).

TEXT BOOKS:

1. R. P. Jain, "Modern Digital Electronics", McGraw Hill Education, 2009.
2. M. M. Mano, "Digital logic and Computer design", Pearson Education India, 2016.

REFERENCE BOOKS:

1. A. Kumar, "Fundamentals of Digital Circuits", Prentice Hall India, 2016.

NPTEL Web Course: Digital Circuits
NPTEL Video Course: Digital Circuits

GATE Syllabus: Digital Circuits, Number systems; Combinatorial circuits: Boolean algebra, minimization of functions using Boolean identities and Karnaugh map, logic gates and their static CMOS implementations, arithmetic circuits,code converters, multiplexers, decoders and PLAs; Sequential circuits: latches and flip-flops,

counters, shift-registers and finite state machines; Sample and hold circuits, ADCs, DACs. Semiconductor memories. Microprocessor (8085): architecture, programming, memory and I/O interfacing.

IES Syllabus:Digital Circuits (Section:6)Boolean Algebra& uses; Logic gates, Digital IC families, Combinatorial/sequential circuits; Basics of multiplexers, counters/registers/ memories /microprocessors, design& applications. IC Logic gates and their characteristics; IC logic families : DTL, TTL, ECL, NMOS, PMOS and CMOS gates and their comparison; A/D and D/A converters. Semiconductor memories.

VIII. COURSE PLAN (WEEK-WISE):

Lecture	Week	Topic	Course Learning Outcome	Teaching Methodology	Reference
UNIT 1					
1	Week – 1	Introduction	-	Chalk & Board	T1,T2
2		Review of number systems, Complements of Numbers	**Understand** the arithmetic operations carried by digital systems.	Chalk & Board	
3		Codes- Binary Codes, Binary Coded Decimal Code and its Properties	**Understand** the different code representations in digital systems.	Chalk & Board	
4		Unit Distance Codes, Error Detecting and Correcting Codes,*problems on mantissa & exponent	**Understand** the different code representations in digital systems.	Chalk & Board	
5		Boolean Algebra: Basic Theorems and Properties,*problems on tautology & Fallacy	**Learn** Boolean algebra and logical operations in Boolean algebra.	Chalk & Board	
6	Week – 2	Switching Functions, Canonical and Standard Form,	**Learn** Boolean algebra and logical operations in Boolean algebra.	Chalk & Board	
7		Algebraic Simplification of Digital Logic Gates	**Apply** different logic gates to functions and simplify them.	Chalk & Board	
8		Properties of XOR Gates, Universal Gates, Multilevel NAND/NOR realizations	**Apply** different logic gates to functions and simplify them.	Chalk & Board	

9	Week – 3	Digital integrated circuits and classification	To **understand** the basics of digital integrated circuits and classification	Chalk & Board	
10		comparison of various logic families	To **understand** the comparison of various logic families	Chalk & Board	
11		TTL, Schottky TTL	To **know** TTL logic levels	Chalk & Board	
12		CMOS logic	To **know** CMOS logic levels	Chalk & Board	
13		Interfacing CMOS and TTL	To **analyze** the interface between CMOS and TTL	Chalk & Board	
14		Tri-state logic	To **understand** the tri state logic	Chalk & Board	
MOCK TEST- I					
UNIT 2					
15	Week – 4	Introduction	-	Chalk & Board	T1,T2
16		The Minimization of switching function using theorem	**Apply** different logic gates to functions and simplify them.	Chalk & Board	
17		The Karnaugh Map Method-Up to Five Variable Maps	**Analyze** the redundant terms and minimize the expression using K-maps	Chalk & Board	
18		The Karnaugh Map Method-Up to Five Variable Maps	**Analyze** the redundant terms and minimize the expression using K-maps	Chalk & Board	
19		Don't Care Map Entries	**Analyze** the redundant terms and minimize the expression using K-maps	Chalk & Board	
20		Tabular Method	**Identify** the redundant terms and minimize the expression using tabular method	Chalk & Board	
21	Week – 5	Design of Combinational Logic: Adders, Subtractors,	**Apply** the logic gates and design of combinational circuits	Chalk & Board	

22		comparators	**Apply** the logic gates and design of combinational circuits	Chalk & Board	
23		Multiplexers, Demultiplexers	**Apply** the logic gates and design of combinational circuits	Chalk & Board	T1,T2
24		Decoders, Encoders	**Apply** the logic gates and design of combinational circuits	Chalk & Board	
25		Code converters	**Design** of different combinational logic circuits	Chalk & Board	
26		Hazards and Hazard Free Relations	**Design** of different combinational logic circuits	Chalk & Board	
27	Week – 6	BCD arithmetic, carry look ahead adder, serial ladder	**Design** of different combinational logic circuits	Chalk & Board	
28		ALU, elementary ALU design	**Design** of different combinational logic circuits	Chalk & Board	
29		popular MSI chips	**Design** of different combinational logic circuits	Chalk & Board	
30		parity checker/generator	**Design** of different combinational logic circuits	Chalk & Board	
31		Q-M method of function realization	To understand Realization of the method.		
UNIT 3					
32	Week -7	Introduction: Basic Architectural Distinctions between Combinational and Sequential circuits	**Understand** the clock dependent circuits and identify the differences between clocked and clock less circuits	Chalk & Board	T1,T2
33		The Binary Cell, Fundamentals of Sequential Machine Operation	**Understand** the clock dependent circuits and identifythe differences between clocked and clock	Chalk & Board	

			less circuits		
34		Latches, Flip Flops: SR	**Apply** and design clock dependent circuits.	Chalk & Board	
35		JK, Race Around Condition in JK	**Apply** and design clock dependent circuits.	Chalk & Board	
36	Week -8	JK Master Slave	**Apply** and design clock dependent circuits.	Chalk & Board	
37		D and T Type Flip Flops	**Apply** and design clock dependent circuits.	Chalk & Board	
38		Excitation Table of all Flip Flops	**Apply** and design clock dependent circuits.	Chalk & Board	
39		Design of a Clocked Flip-Flop, Timing and Triggering Consideration, Clock Skew	**Understand** how the flip-flops are synchronized.	Chalk & Board	
40		Conversion from one type of Flip-Flop to another	**Apply** and design clock dependent circuits.	Chalk & Board	
41	Week -9	Registers and Counters: Shift Registers	**Apply** the sequential circuits and design the different memory devices and counting circuits.	Chalk & Board,ppt's	T1,T2
42		Data Transmission in Shift Registers, Operation of Shift Registers	**Apply** the sequential circuits and design the different memory devices and counting circuits.	Chalk & Board, ppt's	
43		Shift Register Configuration	**Apply** the sequential circuits and design the different memory devices and counting circuits.	Chalk & Board, ppt's	T1,T2
44		Bidirectional Shift Registers, Applications of Shift Registers	**Apply** the sequential circuits and design the different memory devices and counting circuits.	Chalk & Board, ppt's	
45	Week -10	Design and Operation of Ring and Twisted Ring	**Apply** the sequential circuits and design	Chalk & Board	T1,T2

		Counter	the different memory devices and counting circuits.		
46		Operation Of Asynchronous And Synchronous Counters	**Apply** and design clock dependent circuits.	Chalk & Board	
47		Synthesis of Synchronous Sequential Circuits	**Understand** how synchronous sequential circuit works.	Chalk & Board	
48	Week – 11	Sequence Detector	**Understand** how synchronous sequential circuit works.	Chalk & Board	T 1,T2
49		Parity-bit Generator	**Understand** how synchronous sequential circuit works.	Chalk & Board	
50		Design of Asynchronous Counters	**Understand** how Asynchronous sequential circuit works.	Chalk & Board	
51		Design of Synchronous Modulo N Counters	**Understand** how Asynchronous sequential circuit works.	Chalk & Board	
UNIT 4					
52	Week – 12	Introduction to data converters	To understand the basics of data converter	Chalk & Board	T1,T2
53		Introduction, basic DAC techniques - weighted resistor DAC	To understand the basics of DAC's,and the operation of weighted resistor DAC	Chalk & Board	
54		R-2R ladder DAC, inverted R-2R DAC	To know the disadvantage of weighted resistor DAC, and the operation of R-2R ladder DAC and	Chalk & Board	

			Inverted Ladder DAC		
55	Week – 13	A to D converters - parallel comparator type ADC, counter type ADC	To know the basics of ADC's, and the operation of Parallel type and Counter type ADC	Chalk & Board	
56		Successive approximation ADC , Dual slope ADC	To understand the Operation of Successive Approximation type ADC and Dual slope ADC	Chalk & Board	
57		DAC and ADC Specifications	To study the specifications of DAC's and ADC's	Chalk & Board	
58	Week – 14	A/D converter using voltage to frequency and voltage to time conversion	To study the A/D converter using voltage to frequency and voltage to time conversion	Chalk & Board	
59		specifications of A/D converters	To study the specifications of A/D converters	Chalk & Board	T1,T2
60		example of A/D converter ICs	To analyze the example of A/D converter ICs	Chalk & Board	
MOCK TEST-II					
UNIT 5					
61	Week – 15	Memory organization and operation, expanding memory size.	To Understand Memory organization and operation.	Chalk & Board	T1,T2

62		classification and characteristics of memories.	To Understand the classification and characteristics of memories.	Chalk & Board	
63		sequential memory, read only memory (ROM), read and write memory(RAM)	To Understand the RAM,ROM.	Chalk & Board	
64	Week – 16	content addressable memory (CAM), charge de coupled device memory (CCD).	To Understand the Memory devices.	Chalk & Board	
65		commonly used memory chips, ROM as a PLD.	To Understand the commonly used memory chips, ROM as a PLD	Chalk & Board	
66		Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	To Understand the different types of Programmable logic arrays	Chalk & Board	

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes	
	PO 1	PO2	PO3	PO 4	PO 5	PO6	PO 7	PO 8	PO9	PO1 0	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	2	2	-	-	2	1	-	1	2	2
CO2	3	2	2	2	2	2	-	-	2	1	-	2	1	2
CO3	3	3	2	3	3	1	2	-	2	2	2	2	1	2
CO4	3	2	3	3	3	2	2	-	3	3	3	3	2	3
Average	3	2.25	2.25	2.5	2.5	1.75	1	0	2.25	1.75	1.25	2	1.5	2.25

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

X. QUESTION BANK (JNTUH) :

UNIT - I

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	A)Convert the given Gray code number to equivalent binary 001001011110010. B) Convert (A0F9.0EBA98.0DC)16 to decimal, binary, octal.	Apply	1
2.	A)Simplify the following Boolean expressions using the Boolean theorems. i) (A+B+C)(B'+C)+(A+D)(A'+C) ii)(A+B)(A'+B)(A+B') B) Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates.	Apply	1
3.	A)Encode the message bits (1110)2 into 7-bit even parity hamming code. B) Perform the following arithmetic using 2's complement method. i) 101111-100110 ii) 111001-011010	Apply	1
4.	A)Convert the following expression into sum of products and product of sums. X'+X(X+Y')(Y+Z') B) Implement the following Boolean function with NAND gates only. F(X, Y, Z) = ∑m (1, 2, 3, 4, 5, 7)	Apply	1
5.	Obtain dual of the following Boolean expressions (i) AB+A(B+C)+B'(B+D) ii)A+B+A'B'C b) Obtain the compliment of the following Boolean expressions i)A'BA'BC'+A'BCD+A'BC'D'E ii)ABEF+ABE'F'+A'B'EF.	Apply	1
6.	a)Convert the number$(1222)_3$and$(4413)_5$ into decimal and hexadecimal number system. b)Add and multiply the numbers $(23)_5$ and $(345)_6$ without converting to decimal. c) Consider a function 'F'.Show that F.F'=0 and F+F'=1.	Apply	1
7.	a)Find the 9's complement of the numbers 12345678,87654321. b)Express the function B'D+A'D+BD in sum of minterms and product of maxterms.	Apply	1
8.	a)Given 2 binary numbers X=1010100 and Y=1000011 perform i)X-Y ii)Y-X using 2's complement method. b)Prove that the Gray Code is the reflecting code.	Apply	1
9.	a)Find the complement of the following function in sum of minterms.F(A,B,C,D)= ∑(3,5,9,11,15) b)obtain the dual of the following function. F=A'B+A'BC'+A'BCD+A'B(CDE)'.	Apply	1
10.	a)Explain the operation and use a TTL gate with an	Understand	1

	open-collector output. b) Discuss the logic levels and noise margin with reference to TTL family		
11.	a)Explain the operation of the CMOS gate with open drain output. b) Draw a standard two input TTL NAND gate and explain the operation.	Understand	1
12.	Explain how CMOS-TTL interfacing can be achieved. Give the input and output levels of voltages and explain the same.	Understand	1
13.	a)Write short notes on tristate TTL b) Classify ICs based on application, device used and chip complexity.	Understand	1
14.	What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw the interface circuit and explain the operation?	Understand	1

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	AB+A′B+BC=A′C+AB represents which theorem?	Apply	1
2.	How do you obtain dual of an expression?	Understand	1
3.	Convert the following to the required form. i) $(101001.001)_2$= ( )$_{10}$ ii) $(1264)_8$ = ( )$_{10}$ iii)$(A3B)_{16}$=( )$_{10}$	Apply	1
4.	Show that the dual of the Exclusive–OR is equal to its complement.	Apply	1
5.	What is Gray code?	Remember	1
6.	Define Binary coded decimal code.	Remember	1
7.	Draw the logic diagram of NAND gate and explain.	Understand	1
8.	Add and Subtract the following in binary. i)1111 and 1010 ii)100100 and 10110	Apply	1
9.	Give the characteristics of TTL family.	Understand	1
10.	Draw a CMOS tri state buffer and explain.	Understand	1
11.	Draw the interfacing circuit of CMOS driving TTL gate	Understand	1
12.	Define Linear and Digital ICs	Understand	1
13	Why Integrated circuits are needed?	Understand	1
14.	Classify the ICs	Understand	1

15.	a)List the parameters which are used to compare logic families. b) Draw the diagram of basic gate of 2 input TTL gate.	Understand	1
16.	a)Realize EX-OR gate with CMOS circuit. b) Mention the reasons why open loop is not preferred for linear applications	Understand	1

UNIT - II

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	A combinational circuit has 4 inputs (A,B,C,D) and three outputs (X,Y,Z). XYZ represents a binary number whose value equals the number of 1's at the input i. Find the minterm expansion for the X,Y, Z ii. Find the maxterm expansion for the Y and Z.	Evaluate	2
2.	A combinational circuit has four inputs (A, B, C ,D), which represent a binary-coded-decimal digit. The circuit has two groups of four outputs- S,T, U, V (MSB digit) and W, X,Y,Z (LSB digit). Each group represents a BCD digit. The output digits represent a decimal number which is five times the input number. Write down the minimum expression for all the outputs.	Evaluate	2
3.	Simplify the following Boolean expressions using K-map and implement them using NOR gates: (a) F (A, B, C D) = AB'C'+ AC +A'CD' (b)F (W, X, Y,Z)= W' X' Y' Z'+ WXY'Z'+ W'X'YZ+WXYZ	Analyze	2
4.	Design BCD to Gray code converter and realize using logic gates.	Analyze	2
5.	Design 2*4 decoder using NAND gates.	Analyze	2
6.	Reduce the following expression using K-map (BA+A'B+AB')	Apply	2
7.	Design a circuit with three inputs (A, B, C) and two outputs (X,Y) where the outputs are the binary count of the number of "ON" (HIGH) inputs	Analyze	2
8.	Design a three input majority function such that the output is 1 if the input has even number of 1's otherwise the output is 0.	Analyze	2
9.	Design a combinational circuit with the three inputs and one output.the output is equal to logic-1 when the binary value of the input is less than 4 otherwise the output is logic-0.	Analyze	2
10.	a)Minimize the following expression using K-map and realize using NAND Gates,	Apply	2

	F(A,B,C,D)=∑m(0,1,2,9,11) +d(8,10,14,15). b) Minimize the following expression using K-map and realize using NOR Gates. f =πM(0,4,6,7,8,12,13,14,15)		

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define K-map?	Remember	2
2.	Write the block diagram of 2-4 and 3-8 decoders?	Understand	2
3.	Define magnitude comparator?	Remember	2
4.	What do you mean by look-ahead carry?	Remember	2
5.	Simplify the Boolean function using K-Map F(X,Y,Z)= ∑m(0,2,4,5,6).	Apply	2
6.	Write a short notes on multiplexers.	Understand	2
7.	What are the IC components used to design combinatorial circuits with MSI and LSI?	Understand	2
8.	Define the importance of prime implications	Understand	2
9.	Locate the minters in a three variable map for f=∑m(0,1,5,7)	Apply	2
10.	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z without using K-map	Apply	2
11.	What are don't cares? What is minterms?	Understand	2
12.	a)Compare combinational and sequential circuits. b) Explain about binary cell.	Understand	2
13.	Realize a full adder using 2 half adders and explain the truth table.	Analyze	2
14.	Explain the wired logic.	Understand	2
15.	What is a Decoder? Construct a 4×16 decoder with two 3×8 Decoders.	Analyze	2
16.	Realize a full adder using 2 half adders and explain the truth table.	Analyze	2

UNIT - III

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.	Evaluate	2
2.	Draw and explain the circuit diagram of positive edge triggered J-K flip-flop using NOR gates with its truth table. How race around conditions are eliminated?	Evaluate	2

3.	a) Discuss about synchronous and ripple counters. Compare their merits and demerits. b) What do you mean by universal shift register? Draw and explain its circuit diagram and operation.	Understand	2
4.	Explain in detail about timing and triggering considerations sequential circuits.	Understand	2
5.	a) What is a shift register? Explain about the following modes of operations in a four bit shift register (i) shift right (ii) shift left (iii) bidirectional. b) Explain the differences between ring and Johnson counters. Design and explain the operation of a decade Johnson counters.	Understand	2
6.	Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits.	Understand	2
7.	a) Design and explain a synchronous MOD-12 down-counter using j-k flipflop. b) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams.		2
8.	Describe about T flip flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip flop.	Understand	2
9.	a) Design a MOD-10 ripple counter. b) Design and construct MOD-5 synchronous counter using JK flip flops.	Apply	2
10.	Differentiate combinational and sequential circuits.	Understand	2
11.	Explain the working principle of JK flip flop in detail.	Understand	2
12.	Derive a JK-flip-flop from SR flip flop.	Create	2
13.	Explain serial transfer in 4-bit shift registers	Understand	2
14.	How many Flip Flops will be complemented in a 10 bit binary ripple counter to reach the next count after counting 1111110011?	Evaluate	2
15.	Explain about Binary Ripple counter.	Understand	2
16.	Define Latch. Explain different types of Latches in detail	Understand	2
17.	Examine with the help of a block diagram, the basic components of a sequential circuit.	Understand	2
18.	Explain the Ripple counter design. Mention its application	Understand	2
19.	a) Explain the design of ring counter using shift registers. b) Draw the logic diagram of a 4-bit binary ripple counter using flip flops that trigger on negative edge transition.	Apply	2
20.	Explain about design of an ALU subsystem in brief.	Understand	2

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Distinguish between a shift register and counter?	Understand	2
2.	What are the applications of shift registers?	Understand	2
3.	What are the applications of Flip-Flops?	Understand	2
4.	Discuss about a bidirectional shift register?	Understand	2
5.	How do you build a latch using universal gates?	Analyze	2
6.	What is the flip-flop memory characteristic?	Understand	2
7.	Distinguish between synchronous and asynchronous latch?	Understand	2
8.	What is meant by clocked flip-flop?	Understand	2
9.	Why a gated D latch is called a transparent latch?	Understand	2
10.	What are the two types of flip-flops?	Understand	2
11.	Write a short notes on Ripple Counter.	Understand	2
12.	Draw a neat diagram of a 3-bit Jhonson Counter and explain its truth table in brief.	Understand	2
13.	Compare latch and flip flop.	Understand	2
14.	What are the drawbacks of ripple counters?	Understand	2
15.	Define Level trigger, Edge trigger, Clock skew.	Understand	2
16.	Explain about Ring counter with a neat diagram.	Understand	2
17.	What are the basic types of shift registers?	Understand	2
18.	Compare asynchronous and synchronous counters.	Understand	2

UNIT - IV

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	a) Explain the operation of Successive approximation ADC. b) Write about the ADC specifications.	Understand	3
2.	a) Discuss about the binary weighted resistor DAC. b) Mention the applications of DAC and ADC.	Understand	3
3.	a) Explain the working of weighted resistor D/A converter and state its features. b) Find the resolution of a 12 bit D/A converter.	Understand	3
4.	a) Explain the working of dual slope A/D converter. b) Draw the IC 1408 DAC pin diagram and explain.	Understand	3
5.	a) Describe Parallel Comparator type ADC operation.	Understand	3

	b) Explain the working of Inverted R-2R ladder D/A converter.		
6.	a) Find out the Step size and Analog output when input is 0011 and 1011. Assume Vref = +5V. b) Explain Successive Approximation ADC with the help of block diagram.	Evaluate	3
7.	Compare the dual slope ADC with successive approximation ADC.	Understand	3
8.	a) Explain the operation of flash ADC using relevant diagrams. b) What are the merits and demerits of counter type ADC? Explain.	Understand	3
9.	a) Obtain an expression for the output voltage of R-2R DAC. b) Explain how Dual Slope A/D converter provides Noise rejection.	Understand	3
10.	a) Find the Resolution of 12-bit D/A Converter. b) An 8-bit Successive Approximation ADC is driven by a 1 MHz clock. Find its Conversion time.	Evaluate	3
11.	a) Discuss the operation of counter type ADC. b) Explain the operation of dual slope ADC	Understand	3
12.	a) For the D/A converter using an R-2R ladder network, determine the size of each step if Rf = 27kΩ and R= 10kΩ and also calculate the output voltage when the inputs b0,b1,b2 and b3 are at 5V. b) Write about the ADC specifications.	Evaluate	3
13.	a) Draw the circuit diagram of Dual slope ADC and explain its working. b) What is the role of DAC in successive approximation ADC?	Understand	3

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Compare R-2R and Weight Resistor types of ADC.	Understand	3
2.	An 8 bit successive approximation type ADC is driven by a 1MHz clock. Find the conversion time.	Understand	3
3.	What are the different sources of errors in DAC?	Understand	3
4.	List the various A/D conversion techniques.	Understand	3
5.	List the draw backs of Binary weighted Resistor technique D/A conversion.	Understand	3
6.	How many resistors are required in a 12-bit weighted resistor DAC? Why?	Understand	3
7.	Explain how Dual-slope ADC provides noise rejection?	Understand	3
8.	Which is the fastest ADC and why?	Understand	3
9.	For a particular 8-bit ADC, the conversion time is 9 μs.	Evaluate	3

	Find the maximum frequency of an input sine wave that can be digitized.		
10.	What is meant by resolution of DAC?	Understand	3
11.	What is the conversion time of counting type ADC and parallel comparator ADC.	Understand	3
12.	What is the advantage of R-2R ladder D/A converter over the one with binary weighted resistors?	Understand	3
13.	What are the different types of ADCs and compare them in terms of speed of operation	Understand	3

UNIT - V

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	a) Draw the structure of a 4×4 static RAM and explain it's operation. b) What is a programmable device? How it differs from ROM?	Understand	4
2.	Discuss any two types of programming technology used in FPGA design.	Understand	4
3.	Explain the detailed logic configurable Block Architecture of FPGA.	Understand	4
4.	Design a PAL to realize a full Adder circuit.	Understand	4
5.	Draw the basic circuit diagram of static RAM and explain its operation.	Understand	4
6.	Compare various programmable devices.	Understand	4
7.	Explain about Serial access memories. Explain Architecture of FPGA in detail.	Understand	4
8.	What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits?	Understand	4
9.	Explain the detailed Architecture of CPLD and its Implementations	Understand	4

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome

1.	What is programmable logic array?	Understand	4
2.	Mention about SRAM and its usage.	Understand	4
3.	Describe about the Serial Access Memories.	Understand	4
4.	Explain the difference between EPROM and EEPROM.	Understand	4
5.	Explain difference between PLA and PAL.	Understand	4
6.	Draw the 1-bit SRAM cell.	Understand	4
7.	What are the various serial access memories?	Understand	4
8.	Implement 2:1 MUX using PAL	Understand	4
9.	Write the Comparison between FPGA and CPLD.	Understand	4

OBJECTIVE QUESTIONS:

UNIT-1

I.Choose the Correct Answer:

1. The fraction $(0.68)_{10}$ is equal to [ ]

a) $(0.010101)_2$ b) $(0.101)_2$ c) $(0.10101)_2$ d) $(0.10111)_2$

2. The Hexadecimal number A0 has the decimal value [ ]

a)80 b) 256 c) 100 d) 160

3. Given two numbers A & B in sign magnitude representation in an eight bit format A=00011110 & B=10011100, A XOR B gives [ ]

a)10000010 b) 00011111 c) 10011101 d) 11100001

4. The value of binary 1111 is [ ]

a) 2^3-1 b) 2^4-1 c) 2^4 d) none of these

5. The minimum number of bits required to represent negative numbers in the range of -1 to -11 using 2's complement arithmetic is [ ]

(a) 2 (b) 3 (c) 4 (d) 5

6. The following code is not a BCD code. [ ]

a) Gray code (b) Xs-3 code (c) 8421 code (d) All of these

7. A 15-bit hamming code requires [ ]

(a) 4 parity bits (b) 5 parity bits (c) 15 parity bits (d) 7 parity bits

8. If=5, thebase (radix) of the number system is [ ]

a) 5 (b) 6 (c) 7 (d) 8

9. The hexadecimal number system is used in digital computers and digital systems to [ ]

(a) Perform arithmetic operations (b) Perform logic operations

(c) Perform arithmetic and logic operations (d) Input binary data into the sys

10. Determine the value of base x if: $(211)_x = (152)_8$ [ ]

(a) 2 (b) 10 (c) 8 (d) 7

11. Determine the value of base x, if $(193)_x = (623)_8$ [ ]

(a) 16 (b) 4 (c) 2 (d) 5

12. Which of the following are called Universal gates [ ]

(a) NAND, NOR (b) AND, OR (c) XOR XNOR (d) OR, XOR

13. Indicate which of the following logic gates can be used to realized all possible

combinational logic functions. **[ ]**

(A) OR gate (B)NAND gates only (C) EX-OR gate (D) NOR & NAND gates

14. Boolean expression for the output of XNOR logic gate with inputs A and B is [ ]

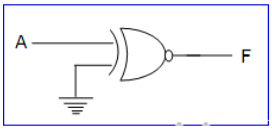
(A) AB' + A'B (B)(A(B)' + AB (C) (A' + (B)(A + B') (D) (A' + B')(A + B)

15. The output of a logic gate is '1' when all its inputs are at logic '0'. The gate is either [ ]

(A)a NAND or an EX-OR gate (B)a NOT or an EX-NOR gate

(C)an OR or an EX-NOR gate (D)an AND or an EX-OR gate

16.The output of the logic gate shown is [ ]



(A) 0 (B) 1 (C) A (D) A'

17. 2's complement representation of a 16 bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is [ ]

(A)0 (B) 1 (C) 32,767 (D) 65,535

18.Two 2's complement numbers having sign bits x and y are added and the sign bit of the result is z. Then, the occurrence of overflow is indicated by the Boolean function. [ ]

A) xyz (B) $\bar{x}\bar{y}\bar{z}$ (C) $\bar{x}\bar{y}z + xy\bar{z}$ (D)xy + yz + zx

19.4 – bit 2's complement representation of a decimal number is 1000. The number is [ ]

(A) +8 (B) 0 (C) -7 (D) -8

20.The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) form is _____. [ ]

(A) 4 (B) 3 (C)2 (D) 8

The short hand notation of min term m_6 is [ ]

(a)A'B'C' (b)A'B'C (c) ABC (d) None of These

II.Fill in the Blanks:

1.. In Boolean algebra A+AB= _____

2. Boolean expression xy+yz+ = _____on reduction.

3. The given expression Y=A+AB+ABC in SOP form is _____

4. Cyclic codes are also called _____codes

5. The basic two types of BCD codes are _____and_____ codes.

6. The distance between code words 10010 & 10101 is _____.

7. Convert the binary code (110110)2 to Gray code _____

8. Conversion of 0.1289062 decimal number to its hexa equivalent is _____

9. In b's complement method, the carry is _____ and in(b-1)'s complement method the carry is _____

10. The MSB of a binary number has a weight of 512, the number consists of _____ bits.

11. _____ are codes which represent letters of the alphabets and decimal numbers as a sequence of 0s and 1s.

12. In b's complement method, the carry is _____and in(b-1)'s complement method the carry _____

13. The MSB of a binary number has a weight of 512,The number consists of _____

14._____ are codes which represent letters of the alphabets and decimal numbers as a sequence of 0s and 1s.

15. The interconnection of gates to perform a variety of logical operations is called_____

16. The NOR gate can function as a NOT gate if _____

UNIT-2

I.Choose the Correct Answer:

The combinational circuits are_____ than sequential circuits [ ]

A)slower B) faster C) same speed D) None

1. In combinational circuits the o/p depends on _____i/p [ ]

A)present B) past C) A & B D) None

2. Full adder circuit adds _____number of bits at a time [ ]

A) 5 B) 2 C) 5 D) 3

3. Half adder circuit adds _____number of bits at a time [ ]

A) 5 B) 2 C) 5 D) 3

4. Serial binary adder is a _____circuit [ ]

A)combinational B) sequential C) A or B D) None

5. A 4 bit parallel adder is designed using _____number of full adders [ ]

A) 2 B) 4 C) 5 D) 3

6. The logic expression for carry of half adder circuit is_____ [ ]

A) A'B B) AB C) AB' D) None

7. The logic expression for sum of half adder circuit is_____ [ ]

A) A'B B) A xor B C) AB' D) None

8. In a half subtractor circuit borrow expression is_____ [ ]

A) A'B B) AB C) AB' D) None

9. The logic expression for difference of half subtractor circuit is_____ [ ]

A) A xor B xor C B) B xor C C) A xor B D) None

10. The logic expression for sum of full adder circuit is_____ [ ]

A) A'BC B) A xor B xor C C) B xor C D) None

11. The logic expression for carry of full adder circuit is_____ [ ]

A) ABC B) A xor B xor C C) B xor C D) None

12. In a full subtractor circuit difference expression is_____ [ ]

A) A xor B xor C B) B xor C C) A xor C D) B xor C

13. In a full subtractor circuit borrow expression is_____ [ ]

A) A xor B xor C B) B xor C C) A xor C D) None

14. The full adder circuit is implemented using _____number of half adder circuits [ ]

A) 3 B) 1 C) 2 D) 4

15. The full subtractor circuit is implemented using _____number of half subtractor circuit [ ]

A) 3 B) 1 C) 2 D) 4

16. Complement of a bit in adder - subtractor circuit is [ ]
A)inverter B) XOR C) AND D)None
17. Carry look ahead adder reduces _____ [ ]
A)carry propagation time B) carry generation time C) sum generation time D) None
18. For an n-bit adder there are _____ gate levels for the carry to propagate from input to output [ ]
A)3n B) 4n C) 2n D) None
19. In carry look ahead adder C_{i+1}=_____ [ ]
A)$G_i+P_iC_i$ B) $G_i+P_{i+1}C_i$ C) $G_{i+1}+P_iC_i$ D)None

II.Fill in the Blanks:

1. The implicants which will definitely occur in the final expression are called_____
2. The prime implicant mode of a bunch of 0s is called a _____
3._____ is a process of converting familiar numbers or symbols into a coded format.
4. A decoder with 64 output lines has _____ select lines.
5. A decimal – to – BCD encoder is a ____ line to _____line encoder.
6. In magnitude comparison of A,B the output of a xor gate if they are equal is ---------
7. n magnitude comparison of A,B the output of a xnor gate if they are equal is --------
8. In magnitude comparison of A,B the output of a xor gate if they are unequal is --------
9. n magnitude comparison of A,B the output of a xnor gate if they are unequal is --------
10. Minimum number of half adders required for 2 bit multiplier is ----------
11. If A=1010 and B=0100 .Then output of a 4 bit parallel adder is_____
12. A decoderwith n input provides _____minterms at the output.
13. A encoder has --------number of inputs and --------number of outputs
14. The number of output lines in 1X4 demultiplexer is_____
15. The number of AND gates required to implement 3 X 8 decoder along with 3 not gates is___
16. To implement full adder ---------size decoder is required
17. A 4X16 decoder can be designed using _____ number of 3x8 decoders
18. An octal to binary encoder is implemented using 3_____ gates
19. The number of select inputs in 32X1 multiplexer is_____
20. The binary variable (A=**B)** is equal to _____ only if all pairs of digits of the two numbers are equal
21. In a 4X2 priority encoder with D3 with highest priority the output XY for input 1111 is_____

UNIT-3

I.Choose the Correct Answer:

1. The output Y of a 2-bit comparator is logic 1 whenever the 2 bit input A is greater than the 2 bit input B. The number of combinations for which the output is logic 1, is
A. 4 B. 6 C. 8 D. 10 [ ]
2. A switch-tail ring counter is made by using a single D flip flop. The resulting circuit is a
A. SR flip flop B. JK flip flop C. D flip flop D. T flip flop
3. An SR latch is a [ ]
A. Combinational circuit B. Synchronous sequential circuit

C. One bit memory element D. One clock delay element

4. The present output Q_n of an edge triggered JK flip-flop is logic '0'. If j = 1, then Q_{n+1} i
   A. Cannot be determined B. Will be logic '0'
   C. Will be logic '1' D. Will race around
5. A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each flip-flop is 50 nsec, the maximum clock frequency that can be used is equal to _____[ ]
   A. 20 MHz B. 10 MHz C. 5 MHz D. 4 MHz
6. Synchronous counters are _____ than the ripple counters. [ ]
   A. Slower B. Faster C. Moderate D. None
7. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then [ ]
   A. R = 10 ns, S = 40 ns B. R = 40 ns, S = 10 ns
   C. R = 10 ns, S = 30 ns D. R = 30 ns, S = 10 ns
8. In sequential Circuits, the output variable depends on _____of the input variable.[ ]
   A. Present State B. Past State C. Both D. None
9. The Serial adder is a _____Circuit. [ ]
   A. Combinational B. Sequential C. Both D. None
10. The outputs of any sequential circuit are always _____to each other. [ ]
    A. Complementary B. Independent C. Pearson D. None
11. In S-R latch, if S=R=1, the present state of the latch is. [ ]
    A. 1 B. 0 C. Undetermined D. None
12. The D- latch sometimes called as _____ Latch. [ ]
    A. Flipflop B. Buffer C. Transparent D. None
13. _____and_____are building blocks of Sequential Circuits. [ ]
    A. Flipflop B. Latches C. Both D. None
14. In _____Triggering, the output of Flipflop responds to the input changes only when its enable input is Low. [ ]
    A. Negative Level B. Positive Level C. Edge D. None
15. If S=0, R=1 and CP = 0 to which Q_n= 0\1, the S-R Flipflop will be in __State. [ ]
    A. No change B. 1 C. 0 D. Undetermined
16. The Basic building block of D- flipflop is ____Flipflop. [ ]
    A. J-K B. Master-Slave C. S-R D. None
17. The output $Q_{n+1}$is delayed by one clock period for an D- Flipflop to which it is called as ____Flipflop. [ ]
    A. J-K B. Master-Slave C.S-R D. Delay
18. For the Inputs J=0, K=0, the output Q will be in ____state. [ ]
    A. Reset B. Undertermined C.Nochange D. Delay
19. In JK flipflop, when J = K = 1, the output the Flipflop will be in ____state. [ ]
    A. Reset B. Undertermined C. Toggling D. Delay
20. _____will not be an clock input of the Master-slave Flipflop. [ ]
    A. Edge Triggered B. Level Triggered C.Both D. None

II.Fill in the Blanks:

1. The ____ Flipflop is a modification of JK Flipflop.
2. If P = C = 0, the flipflop will be in _____ State.
3. For Moore Sequential Circuit, the output depends on____ State.

4. The state reduction technique avoids _____states.
5. The Input and Output of a register can be controlled by connecting ____.
6. The _____ are used to transfer and storage of data in the registers.
7. The acronym of SIPO is_____.
8. The _____ register has capability of both shifts and parallel load.
9. The_____counters are simple in construction for more no. of states.
10. The Major limitation of Ripple counters is_____.

UNIT-IV:

1. Find out the integrating type analog to digital converter?
   a) Flash type converter b) Tracking converter
   c) Counter type converter d) Dual slope ADC
2. Which type of ADC follow the conversion technique of changing the analog input signal to a linear function of frequency?
   a) Direct type ADC b) Integrating type ADC
   c) Both integrating and direct type ADC d) None of the mentioned
3. Which A/D converter is considered to be simplest, fastest and most expensive?
   a) Servo converter b) Counter type ADC c) Flash type ADC d) All of the mentioned
4. The flash type A/D converters are called as
   a) Parallel non-inverting A/D converter b) Parallel counter A/D converter
   c) Parallel inverting A/D converter d) Parallel comparator A/D converter
5. The number of comparator required for flash type A/D converter
   a) Triples for each added bit b) Reduce by half for each added bit
   c) Double for each added bit d) Doubles exponentially for each added bit
6. Drawback of counter type A/D converter
   a) Counter clears automatically b) More complex c) High conversion time d) Low speed
7. Calculate the conversion time of a 12-bit counter type ADC with 1MHz clock frequent to convert a full scale input?
   a) 4.095 μs b) 4.095ms c) 4.095s d) None of the mentioned
8. In a servo tracking A/D converter, the input voltage is greater than the DAC output signal at this condition
   a) The counter count up b) The counter count down
   c) The counter back and forth d) None of the mentioned
9. At what condition error occurs in the servo tracking A/D Converter?
   a) Slow change input b) Rapid change in input
   c) No change in input d) All of the mentioned
10. How many clock pulses do a successive approximation converter requires for obtaining a digital output.
    a) Twelve b) Six c) Eight d) None of the mentioned
11. The Integrating type converters are used in
    a) Digital meter b) Panel meter c) Monitoring system d) All of the mentioned
12. In integrating type ADCs, the
    a) Input voltage is proportional to input averaged over the integration period
    b) Output voltage is proportional to input averaged over the integration period
    c) Output voltage is proportional to sum of input voltage
    d) Input voltage is proportional to sum of input voltage

13. Which type of ADC is chosen for noisy environment?
a) Successive approximation ADC b) Dual slope
c) Charge balancing ADC d) All of the mentioned
14. How to overcome the drawback of the charge balancing ADC?
a) By using precision integrator b) By using Voltage to frequency converter
c) By using voltage comparator d) By using dual slope converter
15. Which among the following has long conversion time?
a) Servo converter b) Dual ramp converter
c) Flash converter d) None of the mentioned
16. In which application dual slop converter are used.
a) Thermocouple b) Digital panel meter c) Weighting scale d) All of the mentioned
17. A dual slope has the following specifications:16bit counter; Clock rate =4 MHz; Input voltage=12v; Output voltage =-7v and Capacitor=0.47µF.If the counters have cycled through 2^n counts, determine the value of resistor in the integrator.
a) 60kΩ b) 50kΩ c) 120kΩ d) 100kΩ
18. A 12 bit dual ramp generation has a maximum output voltage of +12v. Compute the equivalent digital number for the analog signal of +6v.
a) 1000000000 b) 10000000000
c) 1000000000000 d) 100000000000
19. The maximum deviation between actual and ideal converter output after the removal of error is
a) Absolute accuracy b) Relative accuracy
c) Relative /absolute accuracy d) Linearity
20. A monotonic DAC is one whose analog output increases for
a) Decreases in digital input b) An increases in analog input
c) An increases in digital input d) Decreases in analog input

II.Fill in the Blanks:

1. Multiplexing is the process in which _____
2. Multiplexer contains _____
3. Sample and Hold circuit _____
4. In sample mode, the capacitor Two _____
5. Types of converters are _____
6. In D/ A converters V = _____
7. In weighted resistor DAC as the number of bits increase _____
8. In R-2R Ladder Vo = _____
9. If the input voltage is greater than converter reference voltage then_____
10. In A/D converters V = _____

UNIT-V:

I. Choose the Correct answer:

1. ROM consist of _____
a) NOR and OR arrays b) NAND and NOR arrays
c) NAND and OR arrays d) NOR and AND arrays

2. For reprogrammability, PLDs use _____
a) PROM b) EPROM c) CDROM d) PLA
3. Which of the following is a reprogrammable gate array?
a) EPROM b) FPGA c) Both EPROM and FPGA d) ROM
4. The difference between FPGA and PLD is that _____
a) FPGA is slower than PLD b) FPGA has high power dissipation
c) FPGA incorporates logic blocks d) All of the Mentioned
5. PLA is used to implement _____
a) A complex sequential circuit b) A simple sequential circuit
c) A complex combinational circuit d) A simple combinational circuit
6. A PLA is similar to a ROM in concept except that _____
a) It hasn't capability to read only b) It hasn't capability to read or write operation
c) It doesn't provide full decoding to the variables d) It hasn't capability to write only
7.For programmable logic functions, which type of PLD should be used?
a) PLA b) PAL c) CPLD d) SLD
8. The difference between a PAL & a PLA is _____
a) PALs and PLAs are the same thing
b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
d) The PAL has more possible product terms than the PLA
9. A sequential access memory is one in which _____
a) A particular memory location is accessed rapidly b) A particular memory location is accessed sequentially
c) A particular memory location is accessed serially d) A particular memory location is accessed parallel
10. An example of sequential access memory is _____
a) Floppy disk b) Hard disk c) Magnetic tape memory d) RAM
11. A Random Access Memory is one in which _____
a) Any location can be accessed sequentially b) Any location can be accessed randomly
c) Any location can be accessed serially d) Any location can be accessed parallel
12. As the storage capacity of main memory is inadequate, which memory is used to enhance it?
a) Secondary Memory b) Auxiliary Memory c) Static Memory
d) Both Secondary Memory and Auxiliary Memory
13. A dynamic memory is one in which _____
a) Content changes with time b) Content doesn't changes with time
c) Memory is static always d) Memory is dynamic always
14. Static memory holds data as long as _____
a) AC power is applied b) DC power is applied
c) Capacitor is fully charged d) High Conductivity
15. The example of dynamic memory is _____
a) CCD b) Semiconductor dynamic RAM
c) Both CCD and semiconductor dynamic RAM d) Floppy-Disk

16. In dynamic memory, CCD stands for _____
a) Charged Count Devices b) Change Coupled Devices
c) Charge Coupled Devices d) Charged Compact Disk
17. The example of non-volatile memory device is _____
a) Magnetic Core Memory b) Read Only Memory
c) Random Access Memory d) Both Magnetic Core Memory and Read Only Memory
18. By which technology, semiconductor memories are constructed?
a) PLD b) LSI c) VLSI d) Both LSI and VLSI
19. The capacity of a memory unit is _____
a) The number of binary input stored b) The number of words stored
c) The number of bytes stored d) All of the Mentioned
20. In ROM, each bit combination that comes out of the output lines is called _____
a) Memory unit b) Storage class c) Data word d) Address

II.Fill in the Blanks:

1. PLDs with programmable AND and fixed OR arrays are called _____
2. A large memory is compressed into a small one by using _____
3. Data stored in an electronic memory cell can be accessed at random and on demand using ____
4. The evolution of PLD began with_____
5. The inputs in the PLD is given through _____
6. Based on method of access, memory devices are classified into _____ categories.
7. A memory is a collection of _____
8. Each word stored in a memory location is represented by _____
9. MOS ROM is constructed using _____
10. The MOS technology based semiconductor ROMs are classified into _____ categories.
11. If a RAM chip has n address input lines then it can access memory locations upto _____

XIII. WEBSITES:

1. **www.asic-world.com**
2. **www.nptel.ac.in**
3. **www.learnabout-electronics.org**

XIV . MOOCS SWAYAM NPTEL COURSE AS DIGITAL CIRCUITS (onlinecourses.nptel.ac.in/noc18_ee33) – 12week course.

XV. JOURNALS:

INTERNATIONAL

1. International journal of Analog and Digital Electronics
2. International journal of Digital Electronics
3. International journal of Electronic Security and Digital Forensics

XVI. CASE STUDIES / SMALL PROJECTS:

1. Digital Fan speed regulator
2. Traffic controller
3. Adaptive lighting system for automobiles
4. Automatic LED emergency light.