COMPUTER ORGANIZATION AND MICROPROCESSOR

Subject Code : IT304PC
Regulations : R18 - JNTUH
Class : II Year B.Tech I Semester

Department of INFORMATION TECHNOLOGY

BHARAT INSTITUTE OF ENGINEERING AND TECHNOLOGY

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COMPUTER ORGANIZATION AND MICROPROCESSOR (IT304PC)
COURSE PLANNER

I. COURSE OVERVIEW:

The course has been designed to introduce fundamental principles of Computer Organization and Microprocessor. The students completing this course will understand basic of Computer Organization and Microprocessor, including CPU,ALU,Control Unit,Memory hierarchy, Computer performance,pipelining , Instruction Set and addressing modes of 8086 and Assembly programming of 8086 . Finally, students will gain experience in learning concepts of Computer Organization and Programing of 8086 microprocessor

II. PREREQUISITS:

1. Computer and C Programming
2. Basic Electronics

III. COURSE OBJECTIVES:

1.	To understand basic components of computers.
2.	To understand the architecture of 8086 processor.
3.	To understand the instruction sets, instruction formats and various addressing modes of 8086.
4.	To understand the representation of data at the machine level and how computations are performed at machine level.
5.	To understand the memory organization and I/O organization.
6.	To understand the parallelism both in terms of single and multiple processors.

IV. COURSE OUTCOMES:

S.No.	Description	Bloom's Taxonomy Level
1.	Able to understand the basic components and the design of CPU, ALU and Control Unit.	Knowledge, Understand (Level1, Level2)
2.	Ability to understand memory hierarchy and its impact on computer cost/performance.	Apply, Create (Level 3, Level 5)
3.	Ability to understand the advantage of instruction level parallelism and pipelining for high performance Processor design	Analyze (Level 4)
4.	Ability to understand the instruction set, instruction formats and addressing modes of 8086.	Knowledge, Understand (Level3, Level4)
5.	Ability to write assembly language programs to solve problems.	Analyze (Level 4)

V. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (PO)		Level	Proficiency assessed by
PO1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an	3	Assignments

Program Outcomes (PO)		Level	Proficiency assessed by
	engineering specialization to the solution of complex engineering problems.		
PO2	**Problem Analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Examples
PO3	**Design/ Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Assignments, Exercises
PO4	**Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	-	-
PO5	**Modern Tool Usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an Understand of the limitations.	-	-
PO6	**The Engineer and Society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	-	-
PO7	**Environment and Sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	-	-
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	-	-
PO9	**Individual and Team Work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	1	Oral Discussions
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	2	Document Preparation, Presentation
PO11	**Project management and finance**: Demonstrate knowledge and Understand of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in	3	Assignments

Program Outcomes (PO)		Level	Proficiency assessed by
	multidisciplinary environments.		
PO12	**Life-Long Learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	2	Assignments

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO 1	**Foundation of Mathematical Concepts:** To use mathematical methodologies to crack problem using suitable mathematical analysis, data structure and suitable algorithm.	2	Lectures, Assignments
PSO 2	**Foundation of Computer System:** The ability to interpret the fundamental concepts and methodology of computer systems. Students can understand the functionality of hardware and software aspects of computer systems.	1	Tutorials
PSO 3	**Foundations of Software Development:** The ability to grasp the software development life cycle and methodologies of software systems. Possess competent skills and knowledge of software design process. Familiarity and practical proficiency with a broad area of programming concepts and provide new ideas and innovations towards research.	-	-

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VII. SYLLABUS:

UNIT - I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Basic Computer Organization and Design: Instruction codes, Computer Registers, Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt, Complete Computer Description.

Micro Programmed Control: Control memory, Address sequencing, micro program example, design of control unit.

UNIT - II

Central Processing Unit: The 8086 Processor Architecture, Register organization, Physical memory organization, General Bus Operation, I/O Addressing Capability, Special Processor Activities, Minimum and Maximum mode system and timings.

8086 Instruction Set and Assembler Directives-Machine language instruction formats, Addressing
modes, Instruction set of 8086, Assembler directives and operators.

UNIT - III

Assembly Language Programming with 8086- Machine level programs, Machine coding the programs, Programming with an assembler, Assembly Language example programs. Stack

structure
of 8086, Interrupts and Interrupt service routines, Interrupt cycle of 8086, Interrupt programming,
Passing parameters to procedures, Macros, Timings and Delays.

UNIT - IV

Computer Arithmetic: Introduction, Addition and Subtraction, Multiplication Algorithms, Division
Algorithms, Floating - point Arithmetic operations.

Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt, Direct memory Access, Input –Output Processor (IOP),Intel 8089 IOP.

UNIT - V

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory,
Cache Memory.

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction
Pipeline, RISC Pipeline, Vector Processing, Array Processors.

TEXT BOOKS:

1. Computer System Architecture, M. Moris Mano, Third Edition, Pearson. **(UNIST-I , IV , V)**
2. Advanced Microprocessors and Peripherals, K M Bhurchandi, A.K Ray ,3rd edition, McGraw Hill India Education Private Ltd. **(UNITS - II, III).**

REFERENCE BOOKS:

1. Microprocessors and Interfacing, D V Hall, SSSP Rao, 3rd edition, McGraw Hill India Education Private Ltd.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002
3. Computer Organization and Architecture, William Stallings, 9th Edition, Pearson.
4. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.

GATE SYLLABUS: Microprocessor:

Architecture of 8086, Instruction Set and 8086 Programming

VIII. COURSE PLAN (WEEK-WISE):

Session	Week	Unit	Topics	Course Learning Outcomes	Teaching Methodology	Reference
1	1		**Unit-I**: Introduction,Block Diagram Of Digital Computer	**Know** the working of digital computer	Chalk and Talk	**T1, T2**
2			Definition of Computer Organization, Computer Design and Computer	**Understand** computer design and architecture	Chalk and Talk	**T1, T2**

			Architecture.			
3		**1**	**Basic Computer Organization and Design**:	**Know** basics of computer Organization.	Chalk and Talk	**T1, T2**
4			Instruction codes, Computer Registers, Computer instructions	**Understand** concepts instruction codes, Computer Registers, Computer instructions	Chalk and Talk	**T1, T2**
5	2		Timing and Control, Instruction cycle,	**Understand** Timing and Control, Instruction cycle,	Chalk and Talk	**T1, T2**
6			Memory Reference Instructions, Input – Output and Interrupt	**Know** about Memory Reference Instructions, Input – Output and Interrupt	Chalk and Talk	**T1, T2**
7			Complete Computer Description.	**Understand** Complete Computer Description.	Discussion	**T1, T2**
8			Micro Programmed Control: Control memory	**Understand** Control memory.	Chalk and Talk	**T1, T2**
9	3	**2**	Address sequencing	**Understand** Address sequencing	Chalk and Talk	**T1, T2**
10			micro program example, design	**Understand** micro program example, design	Chalk and Talk	**T1, T2**
11			**Unit-II** Central Processing Unit	**Explain** working of CPU	Chalk and Talk, PPTs	**T1, T2**
12			The 8086 Processor Architecture	**Understand** The Architecture of 8086 Architecture.	Chalk and Talk, PPTs	**T1, T2**
13	4		Register organization	**Understand** Register organization of 8086	Chalk and Talk, PPTs	**T1, T2**
14			Physical memory organization	**Understand** Physical memory Organization of 8086	Chalk and Talk, PPTs	**T1, T2**
15			Revesion			
16			**Mock Test-I**			
17	5	**2**	General Bus Operation	**Understand** the basics of General Bus Operation	Chalk and Talk, PPTs	**T1, T2**
18			I/O Addressing Capability	**Study** I/O Addressing Capability	Chalk and Talk, PPTs	**T1, T2**
19			Special Processor Activities	**Learn** Special Processor Activities	Chalk and Talk, PPTs	**T1, T2**
20			Minimum	**Study** Minimum	Chalk and	**T1,**

			and Maximum mode system and timings.	and Maximum mode system and timings.	Talk, PPTs	**T2**
21			Bridge Class			
22			Minimum and Maximum mode system and timings.	Minimum and Maximum mode system and timings.	Chalk and Talk	**T1, T2**
23	6		**8086 Instruction Set and Assembler Directives**-	**Understand 8086 Instruction**	PPTs, discussions	**T1, T2**
24			Machine language	**Study** Machine language	Chalk and Talk	**T1, T2**
25			instruction formats	**Study** instruction formats	Chalk and Talk	**T1, T2, R1**
26	7		Addressing Modes	**Understand** Addressing Modes of 8086	Chalk and Talk, PPTs	**T1, T2, R1**
27			Instruction set of 8086,	**Study** Instruction set of 8086,		
28			Instruction set of 8086,	**Study** Instruction set of 8086,	Chalk and Talk	**T1, T2**
29			Instruction set of 8086,	**Study** Instruction set of 8086,	Chalk and Talk	**T1, T2**
30			Assembler directives and operators.	**Understand** Assembler directives and operators.	Chalk and Talk,	**T1, T2**
31	8		**<u>Unit-III</u>** **Assembly Language Programming with 8086**- Machine level programs	**Learn** Assembly Language Programming with 8086	Chalk and Talk,	**T1, T2**
32			Machine level programs	**Understand** Machine level programs	Chalk and Talk,	
33			Programming with an assembler,	**Understand** Programming with an assembler,	Chalk and Talk, PPTs	**T1, T2**
34	9		Assembly Language example programs.	**Understand** Assembly Language example programs.	Chalk and Talk, PPTs	**T1, T2**
35			Assembly Language example programs	**Understand** Assembly Language example programs	Chalk and Talk, PPTs	**T1, T2**
36			***I Mid Examinations (Week 9)***			

37	10	3	Stack structure of 8086	**Understand** Stack Structure of 8086	Chalk and Talk, PPTs	**T1, T2**
38			Interrupts and Interrupt service routines	**Understand** Interrupts and Interrupt service routines.	Chalk and Talk, PPTs	**T1, T2**
39			Interrupt cycle of 8086	**Understand** Interrupt cycle of 8086.	Chalk and Talk, PPTs	**T1, T2**
40			Interrupt programming	**Understand and Learn** Interrupt programming.	Chalk and Talk, PPTs	**T1, T2**
41	11		Passing parameters to procedures	**Understand** Passing parameters to procedures		
42		4	Macros, Timings and Delays.	**Understand** Macros, Timings and Delays.	Chalk and Talk, PPTs	**T1, T2**
43			**<u>Unit-IV</u>** **Computer Arithmetic:** Introduction	**Understand Computer Arithmetic**	Chalk and Talk, PPTs	**T1, T2**
44			Addition and Subtraction	**Understand** Addition and Subtraction	Chalk and Talk, PPTs	**T1, T2**
45	12		Addition and Subtraction	**Understand** Addition and Subtraction		
46			Multiplication Algorithms	**Understand** Multiplication Algorithms	Chalk and Talk, PPTs	**T1, T2**
47			Division Algorithms	**Understand** Division Algorithms and Floating point arithmetic operations	Chalk and Talk, PPTs	**T1, T2**
48			Floating - point Arithmetic operations		Chalk and Talk, PPTs	**T1, T2**
49	13		**Input-Output Organization**	**Study** Input-Output Organization	Chalk and Talk, PPTs	**T1, T2**
50			Peripheral Devices, Input-Output Interface	**Understand** Peripheral Devices, Input-Output Interface	Chalk and Talk, PPTs	**T1, T2**
51			Asynchronous data transfer	**Understand** Asynchronous data transfer	Chalk and Talk, PPTs	**T1, T2**
52			Modes of Transfer	**Understand** Modes of Transfer	Chalk and Talk, PPTs	
53	14		Priority Interrupt, Direct memory Access,	**Understand** Priority Interrupt, Direct memory Access. **Understand** Input –Output	Chalk and Talk, PPTs	**T1, T2**
54			Input –Output Processor (IOP),Intel 8089 IOP.		Chalk and Talk, PPTs	**T1, T2**

				Processor (IOP),Intel 8089 IOP.		
55			**Unit-V**: **Memory Organization:** Memory Hierarchy, Main Memory	**Study Memory Organization:** Memory Hierarchy, Main Memory	Chalk and Talk, PPTs	**T1, T2**
56			Auxiliary memory, Associate Memory,			
57			Cache Memory.			
58			**Pipeline and Vector Processing**	**Understand Pipeline and Vector Processing**		
59	16		Parallel Processing	**Understand** Parallel Processing	Chalk and Talk, PPTs	**T1, T2**
60			Pipelining, Arithmetic Pipeline	**Understand** Pipelining, Arithmetic Pipeline.	Chalk and Talk, PPTs	**T1, T2**
61		**5**	Instruction Pipeline	**Understand** Instruction Pipeline.	Chalk and Talk, PPTs	**T1, T2**
62	17		RISC Pipeline	**Study** RISC Pipeline	Chalk and Talk, PPTs	**T1, T2**
63			Vector Processing, Array Processors	**Study** Vector Processing, Array Processors		
64			Revision	**Revise** above topics.	PPTs	**T1, T2**
			II Mid Examinations (Week 18)			

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Outcomes	**Program Outcomes**												**Program Specific Outcomes**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO6**	**PO 7**	**PO8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO2**	**PSO3**
CO1	2	1	1	-	-	-	-	-	-	1	-	-	2	1	1
CO2	2	2	1	-	-	-	-	-	-	1	2	1	1	2	2
CO3	3	2	3	-	-	-	-	-	-	1	1	2	1	3	2
CO4	1	1	3	-	-	-	-	-	-	-	2	2	2	3	2
CO5	3	2	3	-	-	-	-	-	-	2	3	-	3	2	3

Average	3	2	2.5	-	-	-	-	-	1	1	2	1	2	2	2
Average (Rounded)	3	2	3	-	-	-	-	-	1	2	3	2	2	1	2

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

X. JUSTIFICATIONS FOR CO-PO MAPPING:

Mapping	Low (1), Medium (2), High(3)	Justification
CO1-PO1	3	Students will be able to Students will be able to understand open circuited P-N junction.
CO1-PO2	2	Students will be able to understand how the diode acts as rectifier and study the characteristics of rectifiers.
CO1-PO3	3	Students will be able to understand the V-I characteristics of P-N junction.
CO1-PO9	1	Students will be able to understand the temperature effects and diode resistance
CO1-PO12	2	Know about drift and diffusion capacitances.
CO1-PSO1	2	Students will be able to understand diode switching times.
CO1-PSO2	2	Students will be able to understand the concept of breakdown in diodes and study the operation and characteristics of Zener diode.
CO2-PO1	3	Students will be able to understand the operation, characteristics and applications of tunnel diode
CO2-PO2	2	Students will be able to understand the operation, characteristics and applications of photo diode and LED.
CO2-PO3	2	To explain clipping circuits and comparators.
CO2-PO12	2	Students will be able to understand how the diode acts as rectifier and study the characteristics of rectifiers.
CO2-PSO1	2	Students will be able to understand the general conditions for filters and study the rectifier with capacitor filter.
CO3-PO1	3	To study the operation of transistor as an amplifier.
CO3-PO2	2	To study the characteristics of CB,CE,CC configurations.
CO3-PO3	3	Compare various configurations of transistors.
CO3-PO10	2	Understand the concept of operating point and purpose of biasing.
CO3-PO11	3	Study about bias compensation, thermal runaway and stability.
CO4-PO1	3	Explain the operation of transistor at low frequencies.
CO4-PO2	2	Explain the operation of CE amplifier, study its frequency response and gain bandwidth product.

CO4-PO3	2	Understand the operation of emitter follower.
CO4-PO10	2	Explain the operation of RC coupled two cascaded CE and multistage CE amplifiers.
CO4-PO11	1	Students will be able to understand the operation, V-I characteristics of JFET.
CO4-PSO1	2	Students will be able to understand the operation, V-I characteristics of MOSFFET.
CO5-PO1	3	Students will be able to understand the operation of low frequency CS and CD amplifiers.
CO5-PO2	2	Students will be able to understand the arithmetic operations carried by digital systems.
CO5-PO3	3	Students will be able to understand the OR, AND, NOT, EX-OR, NAND and NOR DTL gates and modified DTL gates.
CO5-PO9	1	Students will be able to understand the design and analysis of combinational logic circuits.
CO5-PO11	3	Students will be able to analyze the design of decoders, encoders and multiplexers.
CO5-PSO2	1	Students will be able to understand the EX-OR function.
CO6-PO1	3	To design functions using universal gates.
CO6-PO2	2	Students will be able to understand the design and analysis of sequential logic circuits.
CO6-PO3	2	Students will be able to understand construction of latches and flip flops.
CO6-PO11	3	Analyse the clocked sequential circuits and perform state reduction and assignments.
CO6-PO12	2	Students will be able to understand the concept of memory.

XI. QUESTION BANK (JNTUH) :

UNIT - I
Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain the Block Diagram Of Digital Computer.	Understand	1
2.	Define Computer Organization.	Understand	1
3.	With neat sketch explain Computer Architecture	Understand	1
4.	What are Instruction Codes? Explain	Evaluation	1
5.	Explain Computer Registers in Computer Organization ??	Understand	1
6.	Explain Computer Instructions in Computer Organization	Knowledge	1

	? ?		
7.	With neat sketch explain Instruction Cycle of Computer Organization ?	Understand	1
8.	With neat sketch explain timing and control of Computer Organization ?	Understand	1
9.	Explain input output interrupts of Computer Organization ?	Understand	1
10.	Explain control memory for micro programmed control for computer organization ?	Understand	1
11.	With neat sketch explain Address sequencing for CO	Understand	1
12.	Explain the design of Control Unit for Computer Organization	Understand	1
13.	Explain with an example Micro program control for computer organization	Understand	1

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define Computer Organization?	Remember	1
2.	Define Digital Computer ?	Understand	1
3.	Explain Computer Architecture?	Understand	1
4.	What are instruction codes?Explain	Comprehension	1
5.	Explain Computer Registers ?	Comprehension	1
6.	Explain Computer instructions ?	Remember	1
7.	Define Instruction ?	Knowledge	1
8.	Define Instruction Cycle ?	Remember	1
9.	Define Memory Reference Instructions ?	Remember	1
10.	Define Interrupt ?	Remember	1
11.	Define memory ?	Remember	1
12.	Explain Control Memory of Computer Organization ?	Remember	1

13.	Define Address sequencing?	Knowledge	1
15.	Define control unit ?	Remember	1

UNIT - II
Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Draw the block diagram of 8086 microprocessor and explain?	Understand	2
2.	List the addressing modes of 8086?give examples	Remember	2
3.	What is the processing element inside the microprocessor? What process it does ?	Remember	2
4.	What are the signals involved in memory bank selection of 8086 microprocessor	Comprehension	2
5.	Explian Bus generation operation in 8086	Evaluate	2
6.	How many memory locations can be addressed by 8086 microprocessor	Comprehension	2
7.	With neat sketch explain Register organization of 8086?	Understand	2
8.	Explain Physical memory organization of 8086 ?	Understand	2
9.	Explain with neat sketch I/O addressing of 8086 ?	Understand	2
10.	Explain Special Processor Activities in 8086 ?	Understand	2
11.	Explian Instruction set of 8086 ?.	Remember	2
12.	Explain Assembler Directives in 8086 ?	Understand	2
13.	Explain Machine language instruction format in 8086	Remember	2
14.	State the modes in which 8086 operates.	Remember	2
15.	What is the purpose of flag register in 8086? Explain the different bits of flag register in 8086	Analyze	2
16.	Explain the different string manipulation operations of 8086 with a example each ?	Analyze	2

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	What are Macros ?	Remember	2
2.	Define Instruction ?	Remember	2
3.	What is interrupt service routine	Understand	2
4.	What is the maximum memory size that can be addressed by 8086?	Remember	2
5.	What is the function of the signal in 8086	Comprehension	2
6.	What are the predefined interrupts in 8086?	Understand	2
7.	What are the different flag available in status register of 8086?	Knowledge	2
8.	List the various addressing modes present in 8086?	Comprehension	2
9.	How single stepping can be done in 8086	Remember	2
10.	State the significance of LOCK signal in 8086?	Remember	2
11.	What are the functions of bus interface unit (BIU) in 8086?	Remember	2
12.	What is the clock frequency of 8086?	Knowledge	2
13.	What are the two modes of operations present in 8086	Remember	2
14.	What is the purpose of segment registers in 8086?	Remember	2
15.	What is assembler?	Knowledge	2
16.	What is loader?	Remember	2
17.	What are the schemes for establishing priority in order to resolve bus arbitration problem?	Knowledge	2

UNIT - III

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Write the ALP to add two 16bit numbers?	Understand	3
2.	Write an ALP to move 10 blocks of data from one memory to another	Understand	3
3.	With neat sketch explain stack structure of 8086 ?	Understand	3

4.	Explain interrupts of 8086 in detail ?	Understand	3
5.	Draw the small-signal model of common source FET amplifier.	Understand	3
6.	Explain Timing diagram of 8086 ?	Understand	3
7.	Explain Interrupt Service Routine of 8086 ?	Understand	3
8.	Explain Interrupt Cycle of 8086 ?	Understand	
9.	Explain Macros in 8086 ?	Understand	

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	What does ADC instruction does ?	Understand	2
2.	What is the function of ASSUME directive in 8086?	Understand	2
3.	What is the function of ASSUME directive in 8086?	Understand	2
4.	What is the function of DD directive in 8086?	Understand	2
5.	Write an ALP to Add two 8bit numbers?	Analyze	3
6.	Mention Significance of 'O' flag ?	Evaluation	3
7.	Mention Significance of 'T' flag ?	Knowledge	3
8.	What does signal INTL does in 8086		

UNIT - IV

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain addition computer arithmetic Algorithm?	Understand	5
2.	Explain subtraction computer arithmetic Algorithm?	Understand	5
3.	Explain Multiplication computer arithmetic Algorithm?	Understand	5
4.	Explain Floating Point Arithmetic Operations in 8086 ?	Understand	5
5.	Explain Asynchronous data transfer in 8086?	Understand	5
6.	Explain modes of transfer in 8086?	Understand	5
7.	Explain priority interrupt of 8086 ?	Understand	5
8.	Explain Direct Memory Access(DMA) for 8086 ?	Understand	5

9.	Explain 8086 Input Output Processor (IOP)?	Understand	5
10.	Explain Intel 8089 IOP ?	Understand	5

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define peripheral device ?	Knowledge	5
2.	Define synchronous data transfer ?	Understand	5
3.	Define asynchronous data transfer ?	Knowledge	5
4.	Define interrupt ?	Understand	5
5.	Define Priority interrupt ?	Understand	5
6.	Define IOP ?	Understand	5
7.	What is function of Intel 8089 IOP ?	Understand	5

UNIT - V

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain Memory Organization of 8086 in detail ?	Understand	5
2.	Explain Memory hierarchy of 8086 Microprocessor?	Understand	5
3.	Explain Main memory of 8086 Microprocessor?	Understand	5
4.	Explain Auxiliary memory of 8086 Microprocessor?	Knowledge	5
5.	Explain Associate memory of 8086 Microprocessor?	Understand	5
6.	With neat sketch explain Cache Memory of 8086 Microprocessor ?	Understand	5
7.	Explain pipelining ?	Understand	5
8.	Explain Instruction pipeline in detail ?	Understand	5
9.	Explain RISC pipeline in detail ?	Understand	5
10.	Explain Vector Processing in 8086 ?	Understand	5
11.	Explain array processor in detail ?	Understand	5

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define Memory ?	Apply	5
2.	Define Memory Hierarchy ?	Understand	5
3.	Define Main Memory ?	Apply	5
4.	Define Auxiliary Memory ?	Knowledge	5
5.	Define Associate Memory ?	Knowledge	5
6.	Define Cache Memory ?	Understand	5
7.	What is need of Cache Memory ?	Understand	5
8.	Define Pipelining ?	Apply	5
9.	Define Arithmetic Pipelining ?	Understand	5
10.	What do you mean by Instruction pipelining ?	Understand	5
11.	What is RISC pipelining ?	Understand	5

OBJECTIVE QUESTIONS:

UNIT-I

1. A collection of lines that connects several devices is called:

a. peripheral connection wires
b. bus
c. Both a and b
d. Internal wires The cut in voltage (or knee voltage) of a silicon diode is

2. A complete microcomputer system consist of
   a. microprocessor
   b. memory
   c. peripheral equipment
   d. all of the aboveThe resistance of a diode is equal to
3. PC Program Counter is also called
   a. instruction pointer
   b. memory pointer
   c. file pointer
   d. data counter
4. _____ is used to choose between incrementing the PC or performing ALU operations
   a. Conditional codes
   b. Multiplexer
   c. Control unit
   d. None of theseWhen forward biased, a diode

5. The ultimate goal of a compiler is to
   a. Reduce the clock cycles for a programming task.
   b. Reduce the size of the object code.
   c. Be versatile.
   d. Be able to detect even the smallest of errors

6. The decoded instruction is stored in
   a. PC
   b. MDR
   c. Registers
   d. IR

7. CPU does not perform the operation:
   a. data transfer
   b. logic operation
   c. arithmetic operation
   d. all of the above
8. The access time of memory is …… the time required for performing any single CPU operation
   a. Shorter than
   b. Negligible than
   c. Same as
   d. Longer than

9. A microprogram written as string of 0's and 1's is a
(a) symbolic microinstruction
(b) binary microinstruction
(c) binary micro-program
(d) None of TheseA tunnel- diode is
10. Data transfer between **the main memory and the CPU register takes place through two registers namely :**
(a) MAR and Accumulator
(b) general purpose register and MDR
(c) accumulator and program counter
(d) MAR and MDR

11. The register that keeps track of the instructions in the program stored in memory is:
(a) Control register
(b) Program Counter
(c) Status register
(d) Direct register
12. The communication between central system and the outside environment is done by_____
(a) Control system
(b) Logic system
(c) Memory system
(d) I/O subsystemA

13. CISC stands for_____
(a) Compound Instruction Set Computers
(b) Common Instruction Set Computers
(c) Complex Instruction Set Computers
(d) Complex Instruction Set Compilers
14. During the execution of a program which gets initialized first ____?
(a) IR
(b) PC
(c) MAR
(d) None of These
15. The registers,ALU and the interconnection between them are collectively called as:
(a) Data path
(b) information path
(c) Process route
(d) Information trail
16. In LED, light is emitted because
(a) Recombination of charge carriers takes place
(b) Diode gets heated up
(c) Light falling on the diode gets amplified
(d) Light gets reflected due to lens action.
17. GaAs, LEDs emit radiation in the
(a) Ultraviolet region (b) violet - blue green range of the visible region
(c) Visible region (d) infra-red region

UNIT-II

1 The instruction that is used to transfer the data from source operand to destination operand is

(a) data copy (b) branch instruction (c) arithmetic / logic instruction (d) string instruction

2 Which of the following is not a data copy/transfer instruction?

(a) MOV (b) PUSH
(c) DAS (d)POP

3 The instructions that involve various string manipulation operations are

a. branch instructions
b. flag manipulation instructions·
c. shift and rotate instructions
d. string instructions

4 Which of the following instruction is not valid?

(a) MOV AX, BX (b) MOV DS, 5000H (c) MOV AX, 5000H (d) PUSH AX

5In PUSH instruction, after each execution of the instruction, the stack pointer is

(a) incremented by 1
(b) decremented by 1
(c) incremented by 2
(d) decremented by 2

6The instruction that pushes the contents of the specified register/memory location on to the stack is

(a) PUSHF (b) POPF (c) PUSH (d) POP

7In In POP instruction, after each execution of the instruction, the stack pointer is

a. incremented by 1
b. decremented by 1
c. incremented by 2
d. decremented by 2

8A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

(a) Single (b) Multiple (c) Double (d) Triple

9 The intel 8086 microprocessor is a _____ processor

e. 4 bit
f. 8 bit
g. 16bit
h. 12bit

10 In 8086 microprocessor , the address bus is _____ bit wide [ ]

(a) 12bit (b) 10bit (c) 16bit (d)

11. The SF is called as __ [ ]

(a) Service Flag (b) Single Flag (c) Sign Flag (d) Condition Flag

12 The SP is indicated by _____ [ ]

(a) single pointer (b) stack pointer(c) source pointer (d)destination pointer

13. _____ processor is first introduced by the Intel in 1971. [ ]

a) 8080
b) 4004
c) 8008
d) 8085

14. A 16-bits address bus can generate _____addresses.

a) 32767
b) 25652
c) 65536
d) None of the mentioned

15. The register of 8086 are_____ bits in size.

a) 8
b) 12
c) 16
d) 20

16. Which of the following registers are not available in 8086 microprocessor?

a) General data register
b) Segment registers
c) Pointer and Index register

d) All of the mentioned

17. Which of the following is a 16-bit register?
    a) AL
    b) AX
    c) AH
    d) All of the mentioned
18. register is used as a default counter in case of string and loop instructions.
    a) AX
    b) BX
    c) CX
    d) DX
19. The number of address and data lines of 8086_____.
    a) 8 and 8
    b) 16 and 16
    c) 20 and 16
    d) 16 and 20
20. _ is the most important segment and it contains the actual assembly language instructions to be executed by the microprocessor.
    a) Data segment
    b) Code segment
    c) Stack segment
    d) Extra segment

UNIT-III

1. In 8086 the overflow flag is set when_____.
   a) The sum is more than 16 bit
   b) Carry and sign flags are set
   c) Signed numbers go out of their range after an arithmetic operation
   d) During subtraction
2. Direction flag is used with ____
   a) String instructions
   b) Stack Instructions
   c) Arithmetic Instructions
   d) Branch Instructions
3. If_____ flag is set; the processor enters the single step execution mode.
   (a) Direction (b)Trap
   (c) Interrupt d) Zero
4. If segment address = 1005 H, offset address = 5555 H, then the physical address is_____.
   a) 655A H
   b) 155A5 H
   c) 4550 H
   d) 5655
5. If the size of the segment is 64 kb, what will be the starting and ending off set addresses of it
   a) 0000H to 7FFFH
   b) 0000H to FFFFH

c) 8000H to FFFFH
d) 00000H to FFFFFH
6. When one segment starts before the end of another segment then we call them as_____.
a) Non-overlapping segments
b) Overlapping segments
c) Stack area
d) None of these
7.The work of EU is _____
A.encoding B. decoding C. processingD. calculations
8.The 16 bit flag of 8086 microprocessor is responsible to indicate _____
A. the condition of result of ALU operation B. the condition of memory
C. the result of addition D. the result of subtraction
9.The CF is known as _____
A. carry flag B. condition flag C. common flag D. single flag

10. INC destination increments the content of destination by _____
A. 1 B. 2 C. 30 D. 41
11.IMUL source is a signed _____
A. multiplication B. addition C. subtraction D. division
3. _____destination inverts each bit of destination
A.NOT B. NOR C. AND D. NAND
4. The JS is called as _____
A.jump the signed bit B. jump single bit
C. jump simple bit D. jump single bit
5. Instruction providing both segment base and offset address are called ____
A.below type .B. far type C. low type D. high

UNIT-IV

1. The microprocessor determines whether the specified condition exists or not by testing the _____
A. carry flag B. conditional flag C. common flag D. sign flag

2. The LES copies to words from memory to register and _____
A. DS B. CS C. ES D. DS
3. The_____translates a byte from one code to another code
A. XLAT B. XCHNG C. POP D. PUSH
4. The_____contains an offset instead of actual address
A. SP B. IP C. ES D. SS
5. The 8086 fetches instruction one after another from_____of memory
A.code segment B. IP C. ES D. SS
6. The BIU contains FIFO register of size 6 bytes called____.
A.queue B. stack C. segment D. register
7.The_____is required to synchronize the internal operands in the processor CLK Signal
A.UR Signal B. Vcc C. AIE D. Ground

8.The pin of minimum mode AD0-AD15 has_____address
A.16 bit B. 20 bit C. 32 bit D. 4 bit
9.The pin of minimum mode AD0- AD15 has _____data bus
A. 4 bit B. 20 bit C. 16 bit D. 32 bit
10**.** _is used to write into memory
A.RD B. WR C. RD D. CLK
11.The functions of Pins from 24 to 31 depend on the mode in which is operating A. 8085
B. 8086 C. 80835 D. 80845
12.The RD, WR, M/IO is the heart of control for a mode
A.minimum B. maximum C. compatibility mode D. control mode
13.In a minimum mode there is on the system bus
A. single B. double C.multiple D. triple
14.If MN/MX is low the 8086 operates in
A. Minimum B. Maximum C. both (A) and (B) D. medium
15.In max mode, control bus signal So,S1 and S2 are sent out in
A.decoded B. encoded C. shared D. unshared
16.Which bus controller device decodes the signals to produce the control bus signal
A..internal B. data C. externalD. address
17.Which Instruction at the end of interrupt service program takes the execution back to the interrupted program
A.forward B. return C. data D. line
18.The main concerns of the_____are to define a flexible set of commands
B. memory interface B. peripheral interface
C. both (A) and (B) D. control interface
19.Primary function of memory interfacing is that the_____should be able to read from and write into register
A.multiprocessor B. microprocessor C. dual Processor D. coprocessor

UNIT-V

1. IP Stand for
a. Instruction pointer b. Instruction purpose c. Instruction paints d. None of these
2. CS Stand for
a. Code segment b. Coot segment c. Cost segment d. Counter segment
3. DS Stand for
a. Data segment b. Direct segment c. Declare segment d. Divide segment
4. Which are the segment
a. CS: Code segment b. DS: data segment c. SS: Stack segment d. ES:extra segment
5.Which register containing the 8086/8088 flag
a. Status register b. Stack register c. Flag register d. Stand register
6. How many bits the instruction pointer is wide:
a. 16 bit b. 32 bit c. 64 bit d. 128 bit
7.How many type of addressing in memory
a. Logical address b. Physical address c. Both A and B d. None of these
8.The size of each segment in 8086 is
a. 64 kb b. 24 kb c. 50 kb d. 16kb

9. The physical address of memory is
a. 20 bit b. 16 bit c. 32 bit d. 64 bit
10. The _____ address of a memory is a 20 bit address for the 8086 microprocessor
a. Physical b. Logical c. Both d. None of these
11.The pin configuration of 8086 is available in the_____
a. 40 pin b. 50 pin c. 30 pin d. 20 pin
12. DIP stand for
a. Deal inline package b. Dual inline package c. Direct inline package d. Digital inline package
13.The offset of a particular segment varies from _____
a. 000H to FFFH b. 0000H to FFFFH c. 00H to FFH d. 00000H to FFFFFH
14. _____ is usually the first level of memory access by the microprocessor:
a. Cache memory b. Data memory c. Main memory d. All of these
15. which is the small amount of high- speed memory used to work directly with the microprocessor
a. Cache b. Case c. Cost d. Coos
16. The cache usually gets its data from the_____ whenever the instruction or data is required by the CPU
a. Main memory b. Case memory c. Cache memory d. All of these
17. How many type of cache memory
a. 1 b. 2 c. 3 d. 4
18. Which is the type of cache memory
a. Fully associative cache b. Direct-mapped cache c. Set-associative cache d. All of these
19. Which memory is used to holds the address of the data stored in the cache
a. Associative memory b. Case memory c. Ordinary memory d. None of these
20._____ Stores the instruction currently being executed:
a. Instruction register b. Current register c. Both a and b d. None of these
21. In which register instruction is decoded prepared and ultimately executed
a. Instruction register b. Current register c. Both a and b d. None of these
22. The status register is also called the____:
a. Condition code register b. Flag register c. A and B d. None of these

XII. WEBSITES:

1. http://www.onsemi.com
2. http://www.kpsec.freeuk.com/symbol.htm
3. http://buildinggadgets.com/index_circuitlinks.htm
4. http://www.guidecircuit.com
5. www.mathsisfun.com/binary-number-system.html
6. www.allaboutcircuits.com
7. www.electronics-tutorials.ws

NATIONAL

1. Journal of 8086 processor
2. Journal of Programming 8086
3. IETE Journal of Research
4. Journal of Electrical Engineering and Electronic Technology
5. IET Computers & Digital Techniques

V. LIST OF TOPICS FOR STUDENT SEMINARS:

1. Digital Computers
2. Computer Organization
3. Microprocessor 8086
4. Architecture Of 8086
5. Microprocessor 8086 addressing modes
6. Memory organization of 8086
7. Cache Memory

XVII. CASE STUDIES / SMALL PROJECTS:

1. Simple Calculator
2. Notice Board
3. Home Automation